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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	6
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 2x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24123-24si

Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description
AC	alternating current
AI	analog input
API	application programming interface
APOR	analog power on reset
BC	broadcast clock
CMRR	common mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
DNL	differential nonlinearity
DO	digital or data output
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
FB	feedback
FSR	full scale range
GIE	global interrupt enable
GPIO	general purpose IO
ICE	in-circuit emulator
IDE	integrated development environment
ILO	internal low speed oscillator
INL	integral nonlinearity
IO	input/output
IOW	IO write
IPOR	imprecise power on reset
IRA	interrupt request acknowledge
IRQ	interrupt request
ISR	interrupt service routine
ISSP	in-circuit system serial programming
IVR	interrupt vector read
LFSR	linear feedback shift register
LPF	low pass filter
LSB	least-significant bit
LUT	lookup table
MISO	master-in-slave-out
MOSI	master-out-slave-in
MSB	most-significant bit
PC	program counter
PD	power down
PDDSC	power system sleep duty cycle
PGA	programmable gain amplifier
POR	power on reset
PPOR	precision power on reset
PRS	pseudo random sequence
PSoC™	Programmable System-on-Chip
PSRR	power supply rejection ratio
PVT	process voltage temperature
PWM	pulse width modulator
RAM	random access memory
RAS	ROM access strobe
RETI	return from interrupt
RI	row input
RO	row output
ROM	read only memory
SAR	successive approximation register
SC	switched capacitor
SNR	signal-to-noise ratio
SOI	start of instruction
SP	stack pointer
SPD	sequential phase detector
SPI	serial peripheral interconnect
TC	terminal count
VCO	voltage controlled oscillator
WDT	watchdog timer
WDR	watchdog reset

1. Pin Information

This chapter lists, describes, and illustrates the PSoC device pins and pinouts. Table 1-1 presents a summary of the device pins, and the following tables and illustrations detail a representation of the device's pinouts.

1.1 Pin Summary

Table 1-1. PSoC Device Pin Descriptions

Pin Name	Description	Input/Output
SMP	Switch Mode Pump	Power
Vdd	Supply Voltage	Power
Vss	Ground	Power
XRES	External Reset (Active High)	Input
P0[0] – P0[2]	Port 0[0], 0[1], 0[2], Analog Input	Input/Output
P0[3]	Port 0[3], Analog Input/Output	Input/Output
P0[4]	Port 0[4], Analog Input	Input/Output
P0[5]	Port 0[5], Analog Input/Output	Input/Output
P0[6] – P0[7]	Port 0[6], 0[7], Analog Input	Input/Output
P1[0]	Port 1[0], XTALOut/SDATA / I^2C SDA	Input/Output
P1[1]	Port 1[1], XTALIn/SCLK / I^2C SCL	Input/Output
P1[2]	Port 1[2]	Input/Output
P1[3]	Port 1[3]	Input/Output
P1[4]	Port 1[4], EXTCLK	Input/Output
P1[5]	Port 1[5], I^2C SDA	Input/Output
P1[6]	Port 1[6]	Input/Output
P1[7]	Port 1[7], I^2C SCL	Input/Output
P2[0] – P2[3]	Port 2[0], 2[1], 2[2], 2[3], Non-Multiplexed Analog Input (Switched Capacitor)	Input/Output
P2[4]	Port 2[4], External AGND	Input/Output
P2[5]	Port 2[5]	Input/Output
P2[6]	Port 2[6], External VREF	Input/Output
P2[7]	Port 2[7]	Input/Output

2. Packaging Information

This chapter presents and illustrates the packaging specifications for the PSoC device, along with the thermal impedances for each package.

2.1 Packaging Dimensions

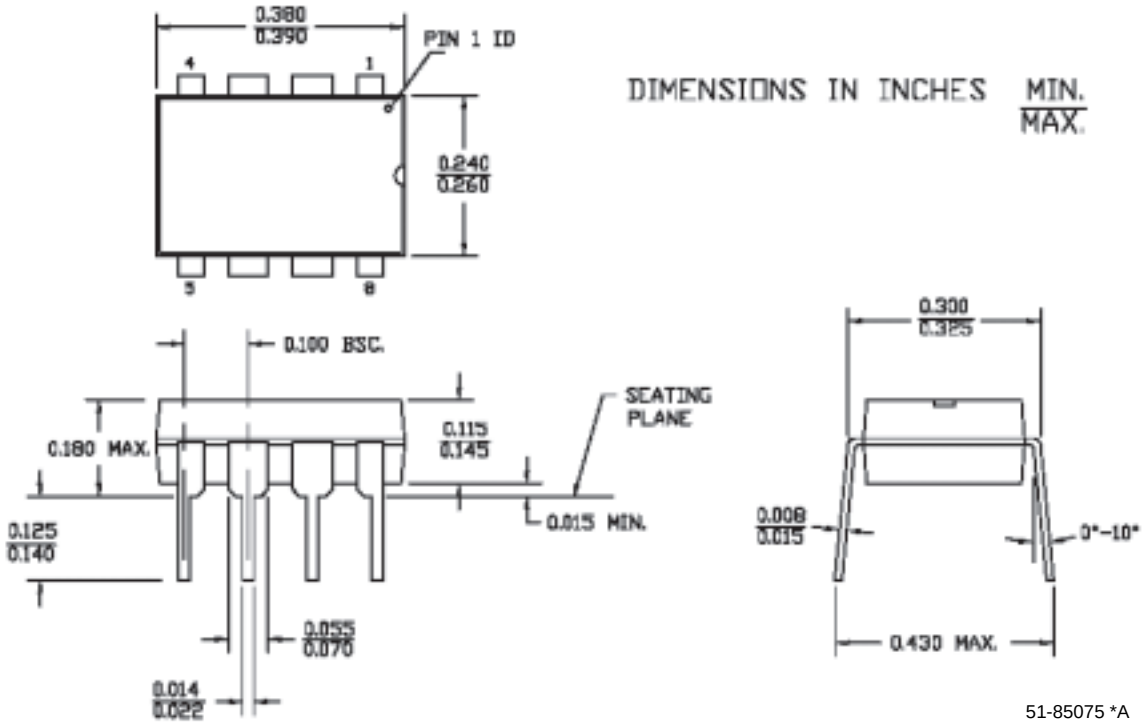


Figure 2-1. 8-Lead (300-Mil) PDIP

3. CPU Core (M8C)

This chapter explains the CPU Core, called M8C, and its associated registers. It covers the internal M8C registers, address spaces, instruction formats, and addressing modes. For additional information concerning the M8C instruction set, reference the *Assembly Language User Guide* available at the Cypress.com web site.

Table 3-1. M8C Registers

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
M8C Register										
x,F7h	CPU_F				XOI		Carry	Zero	GIE	RL : 00
Related Registers										
1,E0h	OSC_CR0	32k Select	PLL Mode	No Buzz	Sleep[1:0]		CPU Speed[2:0]			RW : 00
x,FF	CPU_SCR0	GIES		WDRS	PORS	Sleep			STOP	RW : 17

LEGEND
L: The AND, OR, and XOR flag instructions can be used to modify this register.
x: An “x” before the comma in the address field indicates that this register can be accessed or written to no matter what bank is used.

The M8C is a four MIPS 8-bit Harvard architecture microprocessor. Code selectable processor clock speeds from 93.7 kHz to 24 MHz allow the M8C to be tuned to a particular application’s performance and power requirements. The M8C supports a rich instruction set which allows for efficient low-level language support.

3.1 Internal Registers

The M8C has five internal registers that are used in program execution. The following is a list of these registers.

- Accumulator (A)
- Index (X)
- Program Counter (PC) – internal use only
- Stack Pointer (SP)
- Flags (F)

All of the internal M8C registers are eight bits in width except for the PC which is 16 bits wide. Upon reset, A, X, PC, and SP are reset to 00h. The Flag register (F) is reset to 02h, indicating that the Z flag is set.

With each stack operation, the SP is automatically incremented or decremented so that it always points to the next stack byte in RAM. If the last byte in the stack is at address FFh the Stack Pointer will wrap to RAM address 00h. It is the firmware developer’s responsibility to ensure that the stack does not overlap with user-defined variables in RAM.

With the exception of the F register, the M8C internal registers are not accessible via an explicit register address. The internal M8C registers are accessed using instructions such as:

- `MOV A, expr`
- `MOV X, expr`
- `SWAP A, SP`
- `OR F, expr`
- `JMP LABEL`

The F register may be read by using address F7h in either register bank.

3.2 Address Spaces

The M8C has three address spaces: ROM, RAM, and registers. The ROM address space includes the supervisory ROM (SROM) and the Flash. The ROM address space is accessed via its own address and data bus. Figure 3-1 illustrates the arrangement of the PSoC microcontroller address spaces.

The ROM address space is composed of the Supervisory ROM and the on-chip Flash program store. Flash is organized into 64-byte blocks. The user need not be concerned with program store page boundaries, as the M8C automatically increments the 16-bit PC on every instruction making the block boundaries invisible to user code. Instructions occurring on a 256-byte Flash page boundary (with the

Destination Indirect Post Increment Example:

Source Code	Machine Code	Comments
`MVI [8], A`	`3F 08`	The value in memory at address 8 (the indirect address) points to a memory location in RAM. The Accumulator value is moved into the memory location pointed to by the indirect address. The indirect address in memory, at address 8, is then incremented.

3.6 Register Definitions

3.6.1 CPU_F (Flag) Register

The Flag register has four chip dependent bits (FL[7:4]) and four dedicated bits (FL[3:0]), as shown in Table 3-1.

3.6.1.1 Chip-Dependent Flag Bits

The chip-dependent Flag bits have no effect internally on the M8C. These bits are manipulated by the user with the Flag-Logic opcodes (for example, XOR F, 80h). Bit Definitions for the PSoC Mixed Signal Array family are as follows.

Bits 7, 6, and 5: Reserved.

Bit 4: XOI. IO Bank Select. This bit is used to select between register banks, in order to support more than 256 registers.

3.6.1.2 Dedicated Flag Bits

The dedicated Flag bits are described as follows.

Bit 3: Reserved.

Bit 2: Carry. Carry Flag. This bit is set or cleared in response to the result of several instructions. It may also be manipulated by the Flag-Logic opcodes (for example, OR F, 4). See the *PSoC Designer Assembly Guide User Manual* for more details.

Bit 1: Zero. Zero Flag. This bit is set or cleared in response to the result of several instructions. It may also be manipulated by the Flag-Logic opcodes (for example, OR F, 2). See the *PSoC Designer Assembly Guide User Manual* for more details.

Bit 0: GIE. Global Interrupt Enable. The state of this bit determines whether interrupts (by way of the IRQ) will be recognized by the M8C. This bit is set or cleared by the user, using the Flag-Logic opcodes (e.g., OR F, 1). GIE is also cleared automatically by the interrupt routine, after the flag byte has been stored on the stack.

For GIE=1, the M8C samples the IRQ input for each instruction. For GIE=0, the M8C ignores the IRQ.

For additional information, reference the CPU_F register on page 152.

together as DM[2:0]. Drive modes are shown in Table 6-3.

Table 6-3. Pin Drive Modes

Drive Mode DM[2:0]	Pin State	Description
000b	Resistive pull down	Strong high, resistive low
001b	Strong drive	Strong high, strong low
010b	High impedance	Hi-Z high and low, digital input enabled
011b	Resistive pull up	Resistive high, strong low
100b	Open drain high	Slow strong high, Hi-Z low
101b	Slow strong drive	Slow strong high, slow strong low
110b	High impedance, analog (**reset state**)	Hi-Z high and low, digital input disabled (for zero power) (**reset state**)
111b	Open drain low	Slow strong low, Hi-Z high

For analog IO, the drive mode should be set to one of the Hi-Z modes, either 010b or 110b. The 110b mode has the advantage that the block's digital input buffer is disabled, so no "crowbar" current flows even when the analog input is not close to either power rail. When digital inputs are needed on the same pin as analog inputs, the 010b Drive mode should be used. If the 110b Drive mode is used, the pin will always be read as a zero by the CPU and the pin will not be able to generate a useful interrupt. (It is not strictly required that a Hi-Z mode be selected for analog operation).

For global input modes, the drive mode must be set to 010b.

This GPIO provides a default drive mode of high impedance (Hi-Z). This is achieved by forcing the reset state of all PRTxDM1 and PRTxDM2 registers to FFh.

The resistive drive modes place a resistance in series with the output, for low outputs (mode 000b) or high outputs (mode 011b). Strong drive mode 001b gives the fastest edges at high DC drive strength. Mode 101b gives the same drive strength but with slower edges. The Open drain modes (100b and 111b) also use the slower edge rate drive. These modes enable open drain functions such as I^2C mode 111b (although the slow edge rate is not slow enough to meet the I^2C fast mode specification).

For additional information, reference the PRTxDM2 register on page 91, the PRTxDM0 register on page 155, and the PRTxDM1 register on page 156.

6.2.5 PRTxICx Registers

The interrupt mode for the pin is determined by bits in two registers: PRTxIC1 and PRTxIC0. These are referred to as IM1 and IM0, or together as IM[1:0].

There are four possible interrupt modes for each port pin. Two mode bits are required to select one of these modes and these two bits are spread into two different registers (PRTxIC0 and PRTxIC1). The bit position of the effected port pin (Example: Pin[2] in Port 0) is the same as the bit position of each of the Interrupt Control register bits that control the interrupt mode for that pin (Example: Bit[2] in PRT0IC0 and bit[2] in PRT0IC1). The two bits from the two registers are treated as a group.

The interrupt mode must be set to one of the non-zero modes listed in Table 6-4, in order to get an interrupt from the pin.

Table 6-4. GPIO Interrupt Modes

Interrupt Mode IM[1:0]	Description
00b	Bit interrupt disabled, INTO de-asserted
01b	Assert INTO when PIN = low
10b	Assert INTO when PIN = high
11b	Assert INTO when PIN = change from last read

The GPIO interrupt mode "disabled" (00b) disables interrupts from the pin, even if the GPIO's bit interrupt enable is on (from the PRTxIE register).

Interrupt mode 01b means that the block will assert the interrupt line (INTO) when the pin voltage is low, providing the block's bit interrupt enable line is set (high).

Interrupt mode 10b means that the block will assert the interrupt line (INTO), when the pin voltage is high, providing the block's bit interrupt enable line is set (high).

Interrupt mode 11b means that the block will assert the interrupt line (INTO) when the pin voltage is the opposite of the last state read from the pin (again providing the block's bit interrupt enable line is set high). This mode switches between low mode and high mode, depending on the last value that was read from the port during reads of the data register (PRTxDR). If the last value read from the GPIO was 0, the GPIO will subsequently be in interrupt high mode. If the last value read from the GPIO was 1, the GPIO will then be in interrupt low mode.

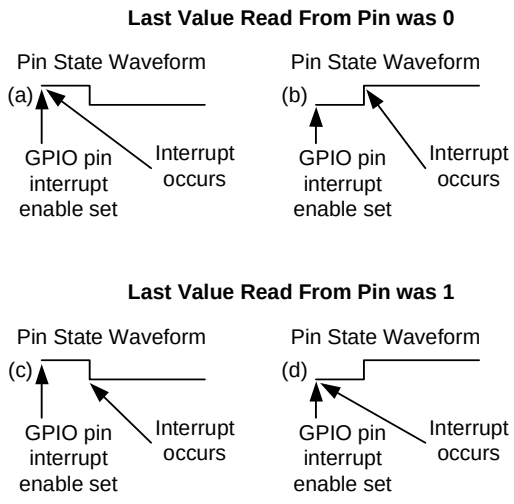


Figure 6-3. GPIO Interrupt Mode 11b

Figure 6-3 assumes that the GIE is set, GPIO interrupt mask is set, and that the GPIO interrupt mode has been set to 11b. The change interrupt mode is different from the other modes, in that it relies on the value of the GPIO's read latch to determine if the pin state has changed. Therefore, the port that contains the GPIO in question must be read during

every interrupt service routine. If the port is not read, the interrupt mode will act as if it is in high mode when the latch value is 0 and low mode when the latch value is 1.

For additional information, reference the PRTxIC0 register on page 157 and the PRTxIC1 register on page 158.

8. Internal Main Oscillator (IMO)

This chapter briefly presents the Internal Main Oscillator (IMO) and its associated register. The IMO produces clock signals of 24 MHz and 48 MHz.

Table 8-1. Internal Main Oscillator Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
1,E8h	IMO_TR	Trim[7:0]								W : 00

8.1 Architectural Description

The Internal Main Oscillator outputs two clocks: a SYSCLK, which can be the internal 24 MHz clock or an external clock, and a SYSCLK2X that is always twice the SYSCLK frequency. In the absence of a high-precision input source from the 32 kHz crystal oscillator, the accuracy of the internal 24 MHz/48 MHz clocks will be +/-2.5% over temperature variation and two voltage ranges (3.3V +/-.3V and 5.0V +/-5%). No external components are required to achieve this level of accuracy.

There is an option to phase lock this oscillator to the External Crystal Oscillator. The choice of crystal and its inherent accuracy will determine the overall accuracy of the oscillator. The External Crystal Oscillator must be stable prior to locking the frequency of the Internal Main Oscillator to this reference source.

The IMO can be disabled when using an external clocking source. Also, the frequency doubler circuit, which produces SYSCLK2X, can be disabled to save power. Note that when using an external clock, if SYSCLK2X is needed, then the IMO can not be disabled. Registers for controlling these operations are found in the Digital Clocks chapter on page 263.

8.2 Register Definitions

8.2.1 IMO_TR Register

The device specific value for 5 volt operation is loaded into the Internal Main Oscillator Trim Register (IMO_TR) at boot time. The Internal Main oscillator will operate within specified tolerance over a voltage range of 4.75V to 5.25V, with no modification of this register. If the device is operated at a lower voltage, user code must modify the contents of this register. For operation in the voltage range of 3.3V +/-.3V, this can be accomplished with a Table Read command to the Supervisor ROM, which will supply a trim value for operation in this range. For operation between these Voltage ranges, user code can interpolate the best value using both available factory trim values.

Bits 7 to 0: Trim. These bits are used to trim the Internal Main Oscillator. A larger value in this register will increase the speed of the oscillator.

For additional information, reference the IMO_TR register on page 181.

13.1.22 ACBxxCR0

Analog Continuous Time Type B Block Control Register 0

Individual Register Names and Addresses

ACB00CR0 : x,71h ACB01CR0 : x,75h

	7	6	5	4	3	2	1	0
Access : POR	RW : 0				RW : 0	RW : 0	RW : 0	
Bit Name	RTapMux[3:0]				Gain	RTopMux	RBotMux[1:0]	

For additional information, reference the “Register Definitions” on page 257 in the Continuous Time Block chapter.

Bit **Name** **Description**

[7:4] **RTapMux[3:0]**

Encoding for selecting one of 18 resistor taps. The four bits of RTapMux[3:0] allow selection of 16 taps. The two additional tap selections are provided using ACBxxCR3 bit 0, EXGAIN. The EXGAIN bit only affects the RTapMux values 0h and 1h.

RTap	EXGAIN	Rf	Ri	Loss	Gain
0h	1	47	1	0.0208	48.000
1h	1	46	2	0.0417	24.000
0h	0	45	3	0.0625	16.000
1h	0	42	6	0.1250	8.000
2h	0	39	9	0.1875	5.333
3h	0	36	12	0.2500	4.000
4h	0	33	15	0.3125	3.200
5h	0	30	18	0.3750	2.667
6h	0	27	21	0.4375	2.286
7h	0	24	24	0.5000	2.000
8h	0	21	27	0.5625	1.778
9h	0	18	30	0.6250	1.600
Ah	0	15	33	0.6875	1.455
Bh	0	12	36	0.7500	1.333
Ch	0	9	39	0.8125	1.231
Dh	0	6	42	0.8750	1.143
Eh	0	3	45	0.9375	1.067
Fh	0	0	48	1.0000	1.000

[3] **Gain**

Select gain or loss configuration for output tap.

0 Loss
1 Gain

[2] **RTopMux**

Encoding for feedback resistor select.

0 Rtop to Vdd
1 Rtop to opamp’s output

[1:0] **RbotMux[1:0]**

Encoding for feedback resistor select. Bits [1:0] are overridden if bit 1 of ACBxxCR3 is set. In that case, the bottom of the resistor string is connected cross columns. Note that available mux inputs vary by individual PSoC block.

	ACB00	ACB01
00b	ACB01	ACB00
01b	AGND	AGND
10b	Vss	Vss
11b	ASC10	ASD11

13.1.25 ASCxxCR0

Analog Switch Cap Type C Block Control Register 0

Individual Register Names and Addresses

ASC10CR0 : x,80h ASC21CR0 : x,94h

	7	6	5	4	3	2	1	0
Access : POR	RW : 0	RW : 0	RW : 0	RW : 00				
Bit Name	FCap	ClockPhase	ASign	ACap[4:0]				

For additional information, reference the “Register Definitions” on page 251 in the Switched Capacitor Block chapter.

Bit	Name	Description
[7]	**FCap**	F Capacitor value selection bit. 0 16 capacitor units 1 32 capacitor units
[6]	**ClockPhase**	The ClockPhase controls the clock phase of the comparator within the switched cap blocks, as well as the clock phase of the switches. 0 Switch phasing is Internal PHI1 = External PHI1. Comparator Capture Point Event is triggered by Falling PHI2 and Comparator Output Point Event is triggered by Rising PHI1. 1 Switch phasing is Internal PHI1 = External PHI2. Comparator Capture Point Event is triggered by Falling PHI1 and Comparator Output Point Event is triggered by Rising PHI2.
[5]	**ASign**	0 Input sampled on Internal PHI1. Reference Input sampled on internal PHI2. Positive gain. 1 Input sampled on Internal PHI2. Reference Input sampled on internal PHI1. Negative gain.
[4:0]	**ACap[4:0]**	Binary encoding for 32 possible capacitor sizes for capacitor ACap.

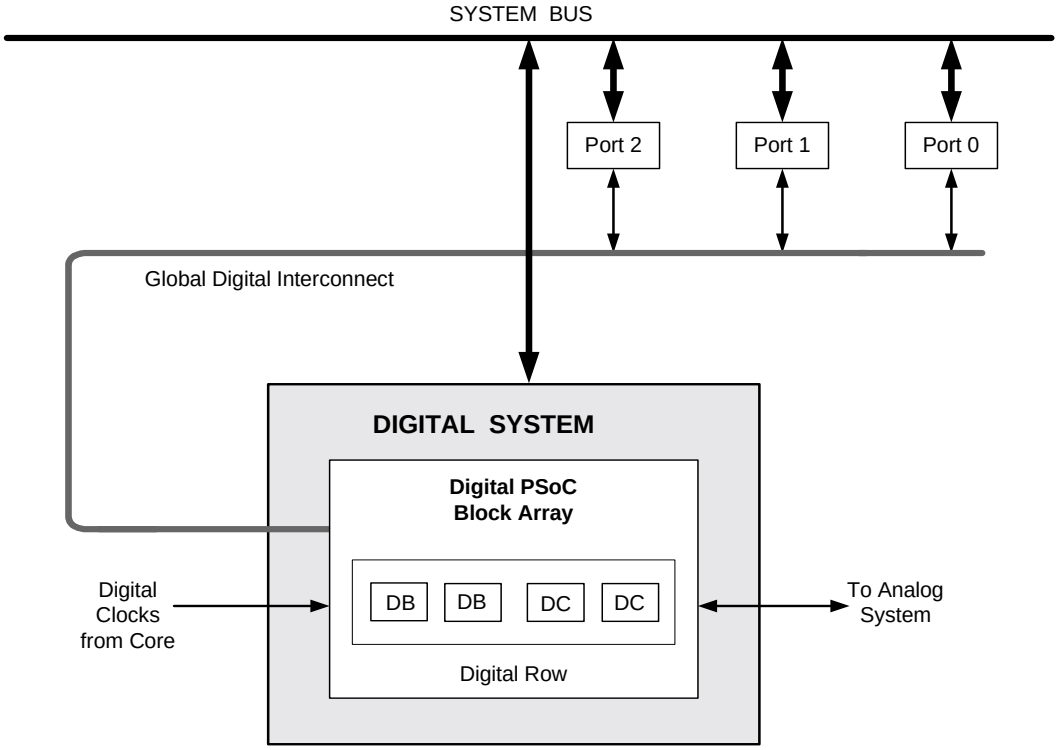
SECTION D DIGITAL SYSTEM

The Digital System section discusses the digital components of the PSoC device and the registers associated with those components. This section encompasses the following chapters:

- Global Digital Interconnect (GDI) on page 187
- Array Digital Interconnect (ADI) on page 191
- Row Digital Interconnect (RDI) on page 193
- Digital Blocks on page 199

Top-Level Digital Architecture

The figure below displays the top-level architecture of the PSoC's digital system. Each component of the figure is discussed at length in this section.



PSoC Digital System Block Diagram

In Figure 15-1, the detailed view of a Digital PSoC block row has been replaced by a box labeled “Digital PSoC Block Row.” The rest of this figure illustrates how all rows are connected to the same globals, clocks, and so on. The figure also illustrates how the broadcast clock nets (BCxxxx) are connected between rows.

20. Analog Input Configuration

This chapter briefly discusses the Analog Input Configuration and its associated registers.

Table 20-1. Analog Input Configuration Registers

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
0,60h	AMX_IN					ACI1[1:0]		ACI0[1:0]		RW : 00
1,62h	ABF_CR0	ACol1Mux		ABUF1EN0		ABUF0EN0		Bypass	PWR	RW : 00

The input multiplexor maps device inputs to analog array columns, based on bit values in the AMX_IN and ABF_CR0 registers. Edge columns are fed by one 4:1 mux; inner columns are fed by 1 of 2 4:1 muxes. The muxes are CMOS switches with typical resistances in the range of 2K ohms. Reference the analog block diagrams, on the following pages, to view the various analog input configurations.

20.1 Register Definitions

20.1.1 AMX_IN Register

Bits 7 to 4: Reserved.

Bits 3 to 0: ACI1[1:0] and ACI0[1:0]. These bits control the analog muxes that feed signals in from port pins into the Analog Column. The analog column can have up to eight port bits connected to its muxed input. ACI1 and ACI0 are used to select among even and odd pins. The AC1Mux bit field controls the bits for those muxes and is located in the Analog Output Buffer Control Register (ABF_CR). There are up to two additional analog inputs that go directly into the Switch Capacitor PSoC blocks.

For additional information, reference the AMX_IN register on page 103.

20.1.2 ABF_CR0 Register

This register controls analog input muxes from Port 0, and the output buffer amplifiers that drive column outputs to device pins.

Bit 7: ACol1MUX. A mux selects the output of column 0 input mux or column 1 input mux. When set, this bit sets the column 1 input to column 0 input mux output.

Bit 6: Reserved.

Bits 5 and 3: ABUFxEN0. These bits enable or disable the column output amplifiers.

Bits 4 and 2: Reserved.

Bit 1: Bypass. Bypass mode connects the amplifier input directly to the output. When this bit is set, all amplifiers controlled by the register will be in bypass mode.

Bit 0: PWR. This bit is used to set the power level of the amplifiers. When this bit is set, all amplifiers controlled by the register will be in a high power state.

For additional information, reference the ABF_CR0 register on page 166.

25.3.6 MAC_Y/ACC_DR0

This register performs two distinct functions; therefore, two names are used to refer to the same address. When the address is written, a multiply operation with accumulation is performed. The multiply accumulate Y (MAC_Y) register is one of the two multiplicand registers for the signed 8-bit multiply with accumulate operation. When this register is written, the product of the written value and the current value of the MAC_X register is calculated, then that product is added to the 32-bit accumulators value. When this address is read, the accumulator's data register 0 is read. This register holds the least significant of four bytes used to hold the accumulator's value.

For additional information, reference the MAC_Y/ACC_DR0 register on page 149.

25.3.7 MAC_CL0/ACC_DR3

This register performs two distinct functions; therefore, two names are used to refer to the same address. When the address is written with any value, all 32-bits of the accumulator are reset to zero. When this address is read, the accumulator's data register 3 is read. This register holds the most significant of four bytes used to hold the accumulator's value.

For additional information, reference the MAC_CL0/ ACC_DR3 register on page 150.

25.3.8 MAC_CL1/ACC_DR2

This register performs two distinct functions; therefore, two names are used to refer to the same address. When the address is written with any value, all 32-bits of the accumulator are reset to zero. When this address is read, the accumulator's data register 2 is read. This register holds the third of four bytes used to hold the accumulator's value. This byte is the least significant of the upper 16 bits of the accumulator's value.

For additional information, reference the MAC_CL1/ ACC_DR2 register on page 151.

27.4.4 Status Timing

Figure 27-8 illustrates the interrupt timing for Byte Complete, which occurs on the positive edge of the ninth clock (byte + ACK/NACK) in Transmit mode and on the positive edge of the eighth clock in Receive mode. There is a maximum of three cycles of latency due to the input synchronizer/filter circuit. As shown, the interrupt occurs on the clock following a valid SCL positive edge input transition (after the synchronizers). The Address bit is set with the same timing, but only after a Slave address has been received. The LRB (Last Received Bit) status is also set with the same timing, but only on the ninth bit after a transmitted byte.

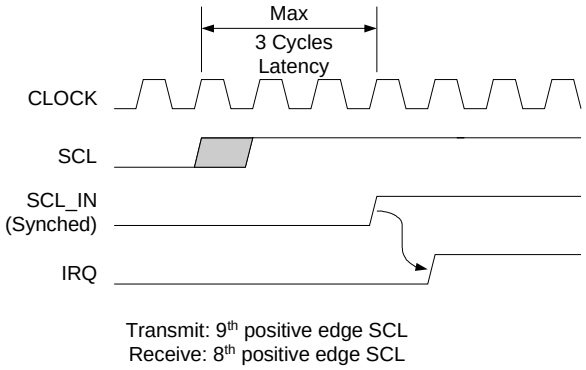


Figure 27-8. Byte Complete, Address, LRB Timing

Figure 27-9 shows the timing for Stop status. This bit is set (and the interrupt occurs) two clocks after the synchronized and filtered SDA line transitions to a '1', when the SCL line is high.

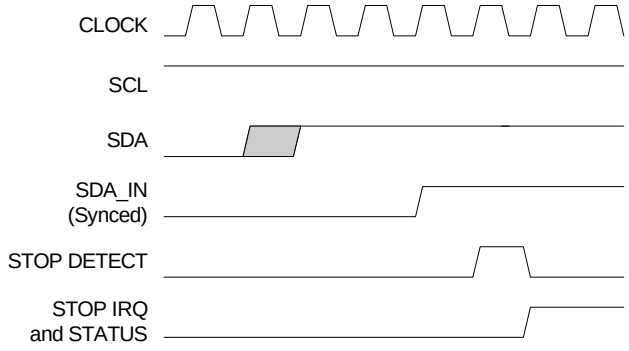


Figure 27-9. Stop Status and Interrupt Timing

Figure 27-10 illustrates the timing for bus error interrupts. Bus Error Status (and interrupt) occurs one cycle after the internal Start or Stop detect (two cycles after the filtered and synced SDA input transition).

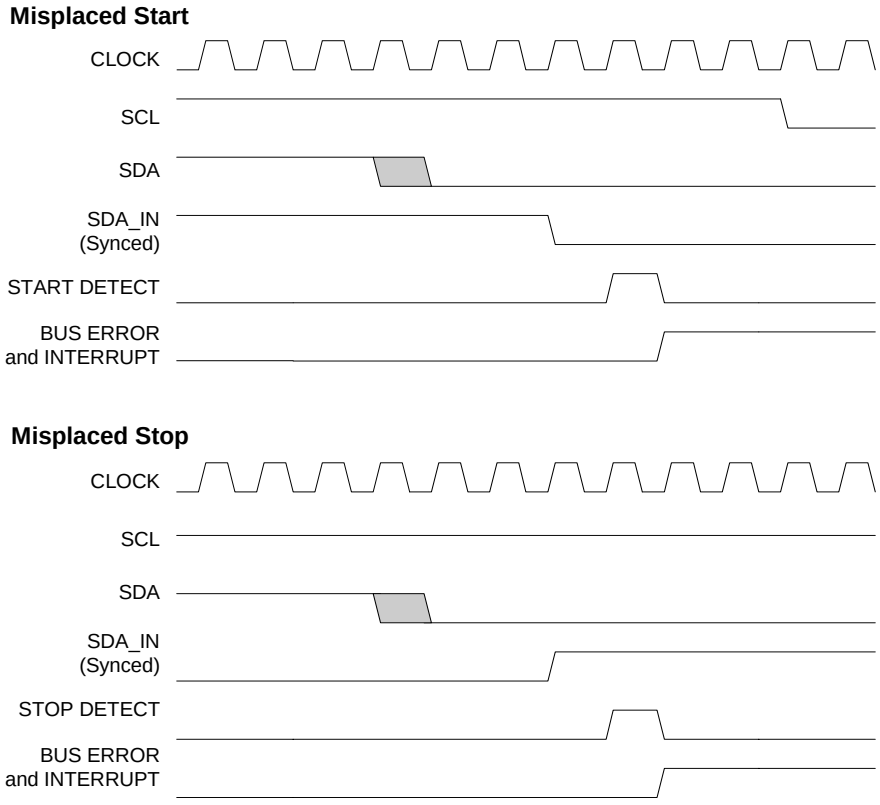


Figure 27-10. Bus Error Interrupt Timing

28. POR and LVD

This chapter briefly discusses the POR and LVD circuits and their associated registers.

Table 28-1. POR and LVD Registers

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
1,E3h	VLT_CR	SMP		PORLEV[1:0]		LVDTBEN	VM[2:0]			RW : 00
1,E4h	VLT_CMP						PUMP	LVD	PPOR	R : 00

28.1 Architectural Description

Power-on-Reset (POR) and Low Voltage Detect (LVD) circuits provide protection against low voltage conditions. The POR function senses Vdd and holds the system in reset, until the magnitude of Vdd will support operation to spec. The LVD function senses Vdd and provides an interrupt to the system when Vdd falls below a selected threshold. Other outputs and status bits are provided to indicate important voltage trip levels.

28.2 Register Definitions

This block contains two registers: VLT_CR and VLT_CMP (read only status bits).

28.2.1 VLT_CR Register

The VLT_CR register is cleared by all resets, which can cause reset-cycling during very slow supply ramps to 5V, when the POR Range is set for the 5V range. This is because the reset will clear the POR range setting back to 3V and a new boot/start-up occurs (possibly many times). The user can manage this with sleep mode and/or reading voltage status bits, if such cycling is an issue.

Bit 7: SMP. SMP low enables the switch mode pump circuit to run, when PUMP is high.

Bit 6: Reserved.

Bits 5 and 4: PORLEV[1:0]. PORLEV[1:0] sets the Vdd level at which PPOR switches.

Bit 3: LVDTBEN. LVDTBEN is AND'ed with LVD to produce a throttle-back signal that reduces CPU clock speed when low voltage conditions are detected.

Bits 2, 1, and 0: VM[2:0]. VM[2:0] sets the Vdd level of the LVD and the Pump Comparator switches.

For additional information, reference the VLT_CR register on page 179.

28.2.2 VLT_CMP Register

Bits 7 to 3: Reserved.

Bit 2: PUMP. PUMP reads the state of the Switch Mode Pump Vdd comparator. The trip points for both LVD and PUMP are set by VM[2:0] in the VLT_CR register.

Bit 1: LVD. LVD reads the state of the low voltage detect comparator. The trip points for both LVD and PUMP are set by VM[2:0] in the VLT_CR register.

Bit 0: PPOR. The PPOR bit reads back the state of the PPOR output. This can only be meaningfully read with PORLEV[1:0] set to disable PPOR. In that case, the PPOR status bit shows the comparator state directly.

For additional information, reference the VLT_CMP register on page 180.

3.3V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
–	AGND = Vdd/2[a] CT Block Power = High	Vdd/2 - 0.037	Vdd/2 - 0.020	Vdd/2 + 0.002	V
–	AGND = 2*BandGap[a] CT Block Power = High	Not Allowed			
–	AGND = P2[4] (P2[4] = Vdd/2) CT Block Power = High	P24 - 0.008	P24 + 0.001	P24 + 0.009	V
–	AGND = BandGap[a] CT Block Power = High	BG - 0.009	BG + 0.005	BG + 0.015	V
–	AGND = 1.6*BandGap[a] CT Block Power = High	1.6*BG - 0.027	1.6*BG - 0.010	1.6*BG + 0.018	V
–	AGND Column to Column Variation (AGND=Vdd/2)[a] CT Block Power = High	-0.034	0.000	0.034	mV
–	REFHI = Vdd/2 + BandGap Ref Control Power = High	Not Allowed			
–	REFHI = 3*BandGap Ref Control Power = High	Not Allowed			
–	REFHI = 2*BandGap + P2[6] (P2[6] = 0.5V) Ref Control Power = High	Not Allowed			
–	REFHI = P2[4] + BandGap (P2[4] = Vdd/2) Ref Control Power = High	Not Allowed			
–	REFHI = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V) Ref Control Power = High	P2[4]+P2[6] - 0.075	P2[4]+P2[6] - 0.009	P2[4]+P2[6]+ 0.057	V
–	REFHI = 3.2*BandGap Ref Control Power = High	Not Allowed			
–	REFLO = Vdd/2 - BandGap Ref Control Power = High	Not Allowed			
–	REFLO = BandGap Ref Control Power = High	Not Allowed			
–	REFLO = 2*BandGap - P2[6] (P2[6] = 0.5V) Ref Control Power = High	Not Allowed			
–	REFLO = P2[4] – BandGap (P2[4] = Vdd/2) Ref Control Power = High	Not Allowed			
–	REFLO = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V) Ref Control Power = High	P2[4]-P2[6] - 0.048	P24-P26 + 0.022	P2[4]-P2[6] + 0.092	V

a. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 2%

DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.24	–	kΩ	
C_{SC}	Capacitor Unit Value (Switch Cap)	–	80	–	fF	