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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	6
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 2x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24123-24sit

Contents

Regardless of the CPU speed bit's setting, if the actual CPU speed is greater than 12 MHz, the 24 MHz operating requirements apply. An example of this scenario is a device that is configured to use an external clock, which is supplying a frequency of 20 MHz. If the CPU speed register's value is 0b011, the CPU clock will be 20 MHz. Therefore, the supply voltage requirements for the device are the same as if the part was operating at 24 MHz off of the internal main oscillator. The operating voltage requirements are not relaxed until the CPU speed is at 12.0 MHz or less.

Table 10-4. OSC_CR0[2:0] Bits: CPU Speed

Bits	Internal Main Oscillator	External Clock
000b	3 MHz	EXTCLK/ 8
001b	6 MHz	EXTCLK/ 4
010b	12 MHz	EXTCLK/ 2
011b	24 MHz	EXTCLK/ 1
100b	1.5 MHz	EXTCLK/ 16
101b	750 kHz	EXTCLK/ 32
110b	187.5 kHz	EXTCLK/ 128
111b	93.7 kHz	EXTCLK/ 256

For additional information, reference the OSC_CR0 register on page 176.

10.2.2 ECO_TR Register

The External Crystal Oscillator Trim register (ECO_TR) sets the adjustment for the External Crystal Oscillator. The device specific value placed in this register at boot time is based on factory testing. This register does not adjust the frequency of the External Crystal Oscillator. It is recommended that the user not alter the bits in this register.

Bits 7 and 6: PSSDC[1:0]. These bits are used to set the sleep duty cycle.

Bits 5 to 0: Reserved.

For additional information, reference the ECO_TR register on page 184.

10.2.3 CPU_SCR1 Register

The CPU_SCR1 register is used to convey status and control of events related to internal resets and watchdog reset.

Bits 7 to 1: Reserved.

Bit 0: IRAMDIS. The Initialize RAM Disable bit is a control bit that is readable and writeable. The default value for this bit is 0, which indicates that the maximum amount of SRAM should be initialized on reset to a value of 00h. When the bit is set, the minimum amount of SRAM is initialized after a watchdog reset. For more information on this bit, see the "SROM Function Descriptions" on page 48.

For additional information, reference the CPU_SCR1 register on page 153.

13.1.4 PRTxDM2

Port Drive Mode Bit 2 Register

Individual Register Names and Addresses

PRT0DM2 : 0,03h PRT1DM2 : 0,07h PRT2DM2 : 0,0Bh

	7	6	5	4	3	2	1	0
Access : POR	RW : FF							
Bit Name	Drive Mode 2[7:0]							

In register PRTxDM2 there are eight possible drive modes for each port pin. Three mode bits are required to select one of these modes, and these three bits are spread into three different registers ("PRTxDM0" on page 155, "PRTxDM1" on page 156, and PRTxDM2). The bit position of the effected port pin (Example: Pin[2] in Port 0) is the same as the bit position of each of the three Drive Mode register bits that control the drive mode for that pin (Example: Bit[2] in PRT0DM0, bit[2] in PRT0DM1 and bit[2] in PRT0DM2). The three bits from the three registers are treated as a group. These are referred to as DM2, DM1, and DM0, or together as DM[2:0].

All Drive Mode bits are shown in the sub-table below ([**2**10] refers to the combination (in order) of bits in a given bit position); however, this register only controls the most significant bit of the drive mode. For additional information, reference the "Register Definitions" on page 60 in the GPIO chapter.

Bit	Name	Description
[7:0]	**Drive Mode 2[7:0]**	Bit 2 of the drive mode, for each of an 8-port pin, for a GPIO port.

[210**]**	**Pin Output High**	**Pin Output Low**	**Notes**
000b	Strong	Resistive	
001b	Strong	Strong	
010b	Hi-z	Hi-z	Digital input enabled.
011b	Resistive	Strong	
100b	Slow + strong	Hi-z	
101b	Slow + strong	Slow + strong	
110b	Hi-z	Hi-z	Digital input disabled for zero power. Reset state.
111b	Hi-z	Slow + strong	I^2C Compatible mode.

13.1.16 AMX_IN

Analog Input Select Register

Individual Register Names and Addresses

AMX_IN: 0,60h

	7	6	5	4	3	2	1	0
Access : POR					RW : 0		RW : 0	
Bit Name					ACI1[1:0]		ACI0[1:0]	

For additional information, reference the “Register Definitions” on page 245 in the Analog Input Configuration chapter.

Bit	Name	Description
[7:4]	**Reserved**	
[3:2]	**ACI1[1:0]**	Selects the Analog Column Mux 1. 00b ACM1 P0[0] 01b ACM1 P0[2] 10b ACM1 P0[4] 11b ACM1 P0[6] **Note** ACol1Mux (ABF_CR, Address = Bank1, 62h) 0 AC1 = ACM1 1 AC1 = ACM0
[1:0]	**ACI0[1:0]**	Selects the Analog Column Mux 0. 00b ACM0 P0[1] 01b ACM0 P0[3] 10b ACM0 P0[5] 11b ACM0 P0[7]

13.1.18 CMP_CR0

Analog Comparator Bus 0 Register

Individual Register Names and Addresses

CMP_CR0: 0,64h

	7	6	5	4	3	2	1	0
Access : POR			R : 0	R : 0			RW : 0	RW : 0
Bit Name			COMP[1]	COMP[0]			AINT[1]	AINT[0]

For additional information, reference the “Register Definitions” on page 238 in the Analog Interface chapter.

Bit	Name	Description
[7:6]	**Reserved**	
[5]	**COMP[1]**	Comparator bus state for column 1. This bit is updated on the rising edge of PHI2, unless the comparator latch disable bits are set. If the comparator latch disable bits are set, then this bit is transparent to the comparator bus in the analog array.
[4]	**COMP[0]**	Comparator bus state for column 0. This bit is updated on the rising edge of PHI2, unless the comparator latch disable bits are set. If the comparator latch disable bits are set, then this bit is transparent to the comparator bus in the analog array.
[3:2]	**Reserved**	
[1]	**AINT[1]**	Controls the selection of the analog comparator interrupt for column 1. 0 The comparator data bit from the column is the input to the interrupt controller. 1 The falling edge of PHI2 for the column is the input to the interrupt controller.
[0]	**AINT[0]**	Controls the selection of the analog comparator interrupt for column 0. 0 The comparator data bit from the column is the input to the interrupt controller. 1 The falling edge of PHI2 for the column is the input to the interrupt controller.

13.1.22 ACBxxCR0

Analog Continuous Time Type B Block Control Register 0

Individual Register Names and Addresses

ACB00CR0 : x,71h ACB01CR0 : x,75h

	7	6	5	4	3	2	1	0
Access : POR	RW : 0				RW : 0	RW : 0	RW : 0	
Bit Name	RTapMux[3:0]				Gain	RTopMux	RBotMux[1:0]	

For additional information, reference the “Register Definitions” on page 257 in the Continuous Time Block chapter.

Bit **Name** **Description**

[7:4] **RTapMux[3:0]**

Encoding for selecting one of 18 resistor taps. The four bits of RTapMux[3:0] allow selection of 16 taps. The two additional tap selections are provided using ACBxxCR3 bit 0, EXGAIN. The EXGAIN bit only affects the RTapMux values 0h and 1h.

RTap	EXGAIN	Rf	Ri	Loss	Gain
0h	1	47	1	0.0208	48.000
1h	1	46	2	0.0417	24.000
0h	0	45	3	0.0625	16.000
1h	0	42	6	0.1250	8.000
2h	0	39	9	0.1875	5.333
3h	0	36	12	0.2500	4.000
4h	0	33	15	0.3125	3.200
5h	0	30	18	0.3750	2.667
6h	0	27	21	0.4375	2.286
7h	0	24	24	0.5000	2.000
8h	0	21	27	0.5625	1.778
9h	0	18	30	0.6250	1.600
Ah	0	15	33	0.6875	1.455
Bh	0	12	36	0.7500	1.333
Ch	0	9	39	0.8125	1.231
Dh	0	6	42	0.8750	1.143
Eh	0	3	45	0.9375	1.067
Fh	0	0	48	1.0000	1.000

[3] **Gain**

Select gain or loss configuration for output tap.

0 Loss
1 Gain

[2] **RTopMux**

Encoding for feedback resistor select.

0 Rtop to Vdd
1 Rtop to opamp’s output

[1:0] **RbotMux[1:0]**

Encoding for feedback resistor select. Bits [1:0] are overridden if bit 1 of ACBxxCR3 is set. In that case, the bottom of the resistor string is connected cross columns. Note that available mux inputs vary by individual PSoC block.

	ACB00	ACB01
00b	ACB01	ACB00
01b	AGND	AGND
10b	Vss	Vss
11b	ASC10	ASD11

13.1.24 ACBxxCR2

Analog Continuous Time Type B Block Control Register 2

Individual Register Names and Addresses

ACB00CR2 : x,73h ACB01CR2 : x,77h

	7	6	5	4	3	2	1	0
Access : POR	RW : 0	RW : 0	RW : 0	RW : 0	RW : 0		RW : 0	
Bit Name	CPhase	CLatch	CompCap	TMUXEN	TestMux[1:0]		PWR[1:0]	

For additional information, reference the “Register Definitions” on page 257 in the Continuous Time Block chapter.

Bit	Name	Description
[7]	**CPhase**	0 Comparator Control latch transparent on PHI1. 1 Comparator Control latch transparent on PHI2.
[6]	**CLatch**	0 Comparator Control latch is always transparent. 1 Comparator Control latch is active.
[5]	**CompCap**	0 Comparator Mode 1 Opamp Mode
[4]	**TMUXEN**	Test mux 0 Disabled 1 Enabled
[3:2]	**TestMux[1:0]**	Select block bypass mode. Note that available mux inputs vary by individual PSoC block and TMUXEN must be set. **ACB00 ACB01** 00b Positive Input to ABUS0 ABUS1 01b AGND to ABUS0 ABUS1 10b REFLO to ABUS0 ABUS1 11b REFHI to ABUS0 ABUS1
[1:0]	**PWR[1:0]**	Encoding for selecting one of four power levels. High Bias mode doubles the power at each of these settings. See bit 6 in the ARF_CR register on page 104. 00b Off 01b Low 10b Medium 11b High

13.1.30 ASDxxCR1

Analog Switch Cap Type D Block Control Register 1

Individual Register Names and Addresses

ASD11CR1 : x,85h ASD20CR1 : x,91h

	7	6	5	4	3	2	1	0
Access : POR	RW : 0			RW : 00				
Bit Name	AMux[2:0]			BCap[4:0]				

For additional information, reference the “Register Definitions” on page 251 in the Switched Capacitor Block chapter.

Bit	Name	Description
[7:5]	**AMux[2:0]**	Encoding for selecting A and C inputs for C Type blocks and A inputs for D Type blocks. (Note that available mux inputs vary by individual PSoC block.)

	ASD20	**ASD11**
000b	ASC10	ACB01
001b	P2[1]	P2[2]
010b	ASC21	ASC10
011b	ABUS0	ASC21
100b	REFHI	REFHI
101b	ASD11	ACB00
110b	Reserved	Reserved
111b	Reserved	Reserved

[4:0]	**BCap[4:0]**	Binary encoding for 32 possible capacitor sizes for capacitor BCap.

13.1.38 RDIxRO0

Row Digital Interconnect Row Output Register 0

Individual Register Names and Addresses

RDI0RO0 : x,B5h

	7	6	5	4	3	2	1	0
Access : POR	RW : 0	RW : 0	RW : 0	RW : 0	RW : 0	RW : 0	RW : 0	RW : 0
Bit Name	GOO5EN	GOO1EN	GOE5EN	GOE1EN	GOO4EN	GOO0EN	GOE4EN	GOE0EN

For additional information, reference the “Register Definitions” on page 196 in the Row Digital Interconnect chapter.

Bit	Name	Description	
[7]	**GOO5EN**	0	Disable LUT output to global output.
		1	Enable LUT output to GOO[5].
[6]	**GOO1EN**	0	Disable LUT output to global output.
		1	Enable LUT output to GOO[1].
[5]	**GOE5EN**	0	Disable LUT output to global output.
		1	Enable LUT output to GOE[5].
[4]	**GOE1EN**	0	Disable LUT output to global output.
		1	Enable LUT output to GOE[1].
[3]	**GOO4EN**	0	Disable LUT output to global output.
		1	Enable LUT output to GOO[4].
[2]	**GOO0EN**	0	Disable LUT output to global output.
		1	Enable LUT output to GOO[0].
[1]	**GOE4EN**	0	Disable LUT output to global output.
		1	Enable LUT output to GOE[4].
[0]	**GOE0EN**	0	Disable LUT output to global output.
		1	Enable LUT output to GOE[0].

13.1.42 I2C_DR

I2C Data Register

Individual Register Names and Addresses

I2C_DR: 0,D8h

	7	6	5	4	3	2	1	0
Access : POR	RW : 00							
Bit Name	Data[7:0]							

This register is read only for received data and write only for transmitted data. For additional information, reference the “Register Definitions” on page 279 in the I^2C chapter.

Bit	Name	Description
[7:0]	**Data**	Read received data or write data to transmit.

13.1.43 I2C_MSCR

I2C Master Status and Control Register

Individual Register Names and Addresses

I2C_MSCR: 0,D9h

	7	6	5	4	3	2	1	0
Access : POR					R : 0	R : 0	RW : 0	RW : 0
Bit Name					Bus Busy	Master Mode	Restart Gen	Start Gen

Bits in this register are held in reset until one of the enable bits in I2C_CFG is set. For additional information, reference the "Register Definitions" on page 279 in the I^2C chapter.

Bit	Name	Description
[7:4]	**Reserved**	
[3]	**Bus Busy**	This bit is set to: 0 When a Stop condition is detected (from any bus master). 1 When a Start condition is detected (from any bus master).
[2]	**Master Mode**	This bit is set/cleared by hardware when the device is operating as a master. 0 Stop condition detected, generated by this device. 1 Start condition detected, generated by this device.
[1]	**Restart Gen**	This bit is cleared by hardware when the Restart generation is complete. 0 Restart generation complete. 1 Generate a Restart condition.
[0]	**Start Gen**	This bit is cleared by hardware when the Start generation is complete. 0 Start generation complete. 1 Generate a Start condition and send a byte (address) to the I2C bus, if bus is not busy.

13.1.53 DEC_DL

Decimator Data Low Register

Individual Register Names and Addresses

DEC_DL: 0,E5h

	7	6	5	4	3	2	1	0
Access : POR	RC : XX							
Bit Name	Data Low Byte[7:0]							

When a hardware reset occurs, the internal state of the Decimator is reset, but the output data registers (DEC_DH and DEC_DL) are not. For additional information, reference the “Register Definitions” on page 273 in the Decimator chapter.

Bit	Name	Description	
[7:0]	**Data Low Byte[7:0]**	Read	Returns the high byte of the decimator.
		Write	Clears the 16-bit accumulator values. Either the DEC_DH or DEC_DL register may be written to clear the accumulators (i.e., it is not necessary to write both).

13.2.24 VLT_CMP

Voltage Monitor Comparators Register

Individual Register Names and Addresses

VLT_CMP: 1,E4h

	7	6	5	4	3	2	1	0
Access : POR						R : 0	R : 0	R : 0
Bit Name						PUMP	LVD	PPOR

For additional information, reference the “Register Definitions” on page 291 in the POR and LVD chapter.

Bit	Name	Description
[7:3]	**Reserved**	
[2]	**PUMP**	Read state of pump comparator. 0 Vdd is above trip point. 1 Vdd is below trip point.
[1]	**LVD**	Reads state of LVD comparator. 0 Vdd is above LVD trip point. 1 Vdd is below LVD trip point.
[0]	**PPOR**	Reads state of Precision POR comparator (only useful with PPOR reset disabled, with PORLEV[1:0] in VLT_CR register set to 11b). 0 Vdd is above PPOR trip voltage. 1 Vdd is below PPOR trip voltage.

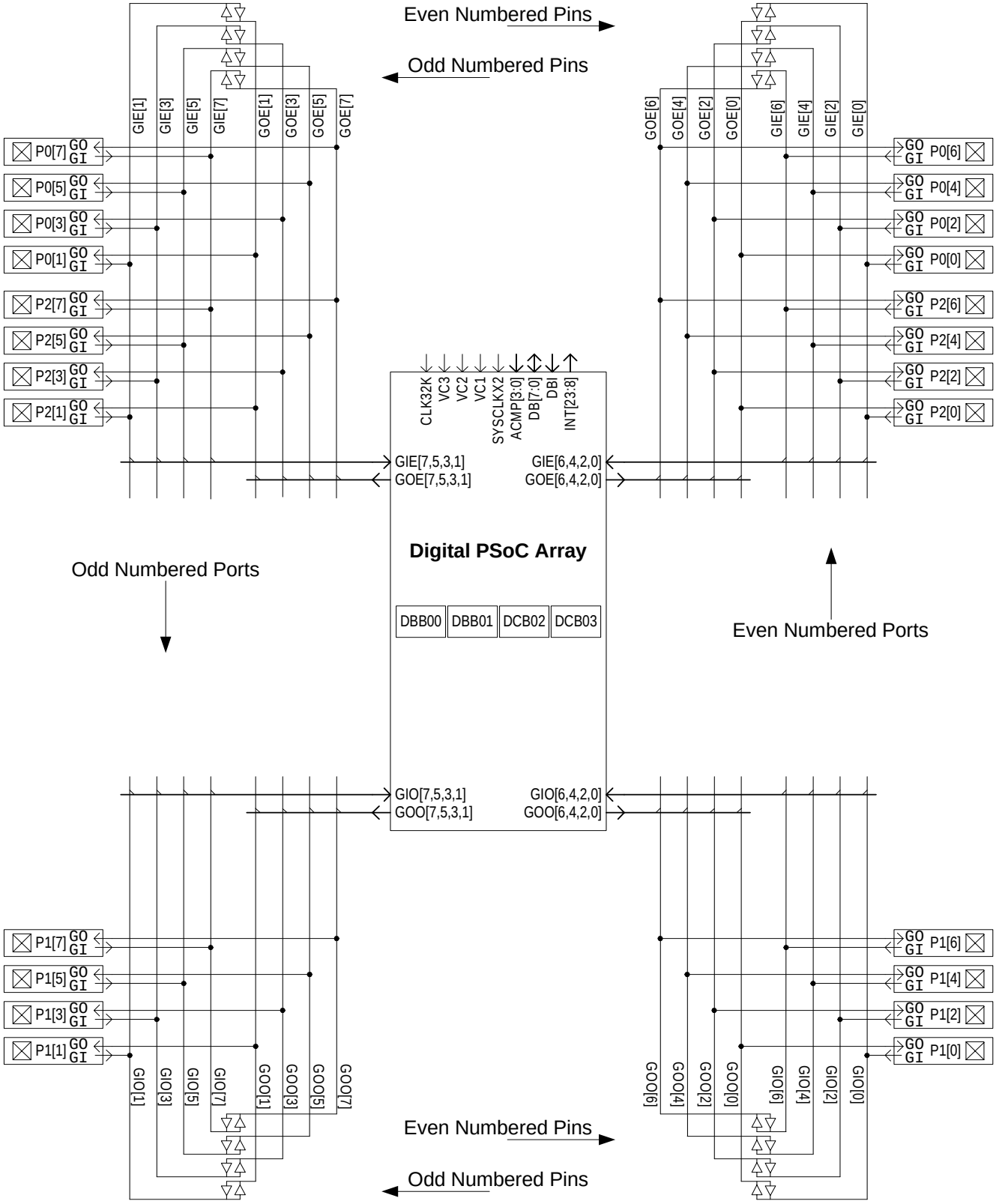

Figure 14-1. Global Interconnect Block Diagram

17.1.12 Asynchronous Transmitter Function

In the Transmitter function, DR0 functions as a shift register, with no input and with the TXD serial data stream output to the primary output F1. DR1 is a TX buffer register and DR2 is unused in this configuration.

Unlike SPI, which has no output latency, the TXD output has one cycle of latency. This is because a multiplexer at the output must select which bits to shift out: the shift register data, framing bits, parity, or mark bits. The output of this multiplexer is registered to unglitch it. When the block is first enabled or when it is idle, a mark bit (logic '1') is output.

The clock generator is a free running divide by eight circuit. Although dividing the clock is not necessary for the Transmitter function, the Receiver function does require a divide by eight for input sampling. It is also done in the Transmitter function, to allow the TX and RX functions to run off the same baud rate generator.

There are two formats supported: A 10-bit frame size including one start bit, eight data bits, and one stop bit or an 11-bit frame size including one start bit, eight data bits, one parity bit, and one stop bit.

The parity generator can be configured to output either even or odd parity on the eight data bits.

A write to the TX Buffer register (DR1) initiates a transmission and an additional byte can be buffered in this register, while transmission is in progress.

An additional feature of the Transmitter function is that a clock, generated with setup and hold time for the data bits only, is output to the auxiliary output. This allows connection to a CRC generator or other digital blocks.

The Transmitter function may not be chained.

17.1.12.1 Block Interrupt

The Transmit block has a selection of two interrupt sources. Interrupt on TX Reg Empty (default) or interrupt on TX Complete. Mode bit 1 in the Function register controls the selection.

If TX Complete is selected as the block interrupt, the Control register must still be read in the interrupt routine so that this status bit is cleared; otherwise, no subsequent interrupts are generated.

17.1.13 Asynchronous Receiver Function

In the Receiver function, DR0 functions as the serial data shift register with RXD input from the DATA input selection. DR2 is an RX buffer register and DR1 is unused in this configuration.

The clock generator and START detection are integrated. The clock generator is a divide by eight which, when the system is idle, is held in reset. When a START bit (logic '0') is detected on the RXD input, the reset is negated and a bit rate clock is generated, subsequently sampling the RXD input at the center of the bit time. Every succeeding START bit resynchronizes the clock generator to the incoming bit rate.

There are two formats supported: A 10-bit frame size including one start bit, eight data bits, and one stop bit. or an 11-bit frame size including one start bit, eight data bits, one parity bit, and one stop bit.

The received data is an input to the parity generator. It is to be compared with a received parity bit, if this feature is enabled. The parity generator can be configured to output either even or odd parity on the eight data bits.

After eight bits of data are received, the byte is transferred from the DR0 shifter to the DR2 RX Buffer register.

An additional feature of the Receiver function is that input data (RXD) and the synchronized clock are passed to the primary output and auxiliary output, respectively. This allows connection to a CRC generator or other digital block.

17.1.13.1 Block Interrupt

The Receiver has one fixed interrupt source, which is the RX Reg Full status.

The RX Buffer register must always be read in the RX interrupt routine, regardless of error status, etc., so that RX Reg Full status bit is cleared; otherwise, no subsequent interrupts are generated.

Table 17-6. Timer Data Register Descriptions *(continued)*

Name	Function	Description
DR1	Period	Write Only Register. Data in this register sets the period of the count. The actual number of clocks counted is Period + 1. In the default one-half cycle terminal count mode, a period value of 00h results in the primary output to be the inversion of the input clock. In the optional full cycle terminal count mode, a period of 00h gives a constant logic high on the primary output. When disabled, a write to this register also transfers the period value directly into DR0. When enabled, if the block frequency is 24 MHz or below, this register may be written to at any time, but the period will only be reloaded into DR0 in the clock following a terminal count. If the block frequency is 48 MHz, the terminal count or compare interrupt should be used to synchronize the new Period register write; otherwise, the counter could be incorrectly loaded.
DR2	Capture/ Compare	Read Write Register (see Exception below). DR2 has multiple functions in a Timer configuration. It is typically used as a Capture register, but it also functions as a Compare register. When enabled and a capture event occurs, the current count in DR0 is synchronously transferred into DR2. When enabled, the compare output is computed using the Compare Type (set in the Function register mode bits) between DR0 and DR2. The result of the Compare is output to the Auxiliary output. When disabled, a read of DR0 will transfer the contents of DR0 into DR2 for the addressed block only. **Exception**: When enabled, DR2 is not writeable.

17.2.1.2 Counter Register Definitions

Bank 0: There are three 8-bit data registers and a 2-bit control register. Table 17-7 explains the meaning of these registers in the context of the Counter operation. Note that the descriptions of the registers are dependant on the enable/disable state of the block. This behavior is only related to the enable bit in the Control register, not the data input that provides the counter gate (unless otherwise noted).

Bank 1: The mode bits in the Function register are block type specific. Other bit fields in this register, as well as the definitions of the Input and Output registers are common to all functions. These mode bits are independent in the Counter block and control the Interrupt Type and the Compare Type (same as the Timer function).

Table 17-7. Counter Data Register Descriptions

Name	Function	Description
DR0	Count Value	Not Directly Readable or Writeable. During normal operation, DR0 stores the current count of a synchronous down counter. When disabled, a write to the DR1 Period register is also simultaneously loaded into DR0 from the data bus. When disabled or the data input (counter gate) is low, a read of DR0 returns 00h to the data bus and transfers the contents of DR0 to DR2. This register should not be read when the counter is enabled and counting.
DR1	Period	Write Only Register. Data in this register sets the period of the count. The actual number of clocks counted is Period + 1. In the default one-half cycle terminal count mode, a period value of 00h will result in the auxiliary output to be the inversion of the input clock. In the optional full cycle terminal count mode, a period of 00h gives a constant logic high on the auxiliary output. When disabled, a write to this register also transfers the period value directly into DR0. When enabled, if the block frequency is 24 MHz or below, this register may be written to at any time, but the period will only be reloaded into DR0 in the clock following a terminal count. If the block frequency is 48 MHz, the terminal count or compare interrupt should be used to synchronize the new Period register write; otherwise, the counter could be incorrectly loaded.
DR2	Compare	Read Write Register. DR2 functions as a Compare register. When enabled, the compare output is computed using the Compare Type (set in the Function register mode bits) between DR0 and DR2. The result of the compare is output to the primary output. When disabled or the data input (counter gate) is low, a read of DR0 will transfer the contents of DR0 into DR2. DR2 may be written to when the function is enabled or disabled.

PSoC blocks are user configurable system resources. On-chip analog PSoC blocks reduce the need for many MCU part types and external peripheral components. Analog PSoC blocks are configured to provide a wide variety of peripheral functions. PSoC Designer Software Integrated Development Environment provides automated configuration of PSoC blocks by selecting the desired functions. PSoC Designer then generates the proper configuration information and prints a device data sheet unique to that configuration.

Each of the analog blocks has many potential inputs and several outputs. The inputs to these blocks include analog signals from external sources, intrinsic analog signals driven from neighboring analog blocks, or various voltage reference sources.

There are three analog PSoC block types: Continuous Time (CT) blocks, and Type C and Type D Switch Capacitor (SC) blocks. CT blocks provide continuous time analog functions. SC blocks provide switched capacitor analog functions. Some available supported analog functions are 12-bit Incremental and 11-bit Delta-Sigma ADC, successive approximation ADCs up to 6 bits, DACs up to 8 bits, programmable gain stages, sample and hold circuits, programmable filters, comparators, and a temperature sensor.

The analog blocks are organized into columns. There are two analog columns in the CY8C24xxx, which contain one Continuous Time Block, one Switch Capacitor (SC) Type C, and one Type D Switch Capacitor (SC). The blocks in a particular column all run off the same clocking source. The blocks in a column also share some output bus resources. Refer to the Analog Interface, on page 233 for additional information.

There are three outputs from each analog block. (There are an additional two discrete outputs in the Continuous Time blocks.)

1. The analog output bus (ABUS) is an analog bus resource that is shared by all of the analog blocks in a column. Only one block in a column can actively drive this bus at any one time and the user has control of this output through register settings. This is the only analog output that can be driven directly to a pin.
2. The comparator bus (CBUS) is a digital bus resource that is shared by all of the analog blocks in a column. Only one block in a column can be actively driving this bus at any one time and the user has control of this output through register settings.
3. The local outputs (OUT, plus GOUT, and LOUT in the Continuous Time blocks) are routed to neighbor blocks. The various input multiplexer connections (NMux, PMux, RBotMux, AMux, BMux, and CMux) all use the output bus from one block as their input.

Six analog PSoC blocks are available separately or combined with the digital PSoC blocks. A precision internal voltage reference provides accurate analog comparisons. A temperature sensor input is provided to the analog PSoC block array, supporting applications such as battery chargers and data acquisition, without requiring external components.

The analog functionality provided is as follows.

- A/D and D/A converters, programmable gain blocks, comparators, and switched capacitor filters.
- Single ended configuration is cost effective for reasonable speed and accuracy, and provides a simple interface to most real-world analog inputs and outputs.
- Support is provided for sensor interfaces, audio codes, embedded modems, and general-purpose opamp circuits.
- Flexible, System on-a-Chip programmability, providing variations in functions.
- For a given function, easily selected trade-offs of accuracy and resolution with speed, resources (number of analog blocks), and power dissipated for that application.
- The analog section is an “Analog Computation Unit,” providing programmed steering of signal flow and selecting functionality through register-based control of analog switches. It also sets coefficients in Switched Capacitor Filters and noise shaping (Delta-Sigma) modulators, as well as program gains or attenuation settings in amplifier configurations.
- The architecture provides continuous time blocks and discrete time (Switched Capacitor) blocks. The continuous time blocks allow selection of precision amplifier or comparator circuitry, using programmable resistors as passive configuration and parameter setting elements. The Switched Capacitor (SC) blocks allow configuration of DACs, Delta Sigma, Incremental or Successive Approximation ADCs, or Switched Capacitor filters with programmable coefficients.

AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
Timer	Capture Pulse Width	50[a]	–	–	ns	
	Maximum Frequency, No Capture	–	–	48	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, With Capture	–	–	24	MHz	
Counter	Enable Pulse Width	50[a]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	48	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, Enable Input	–	–	24	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[a]	–	–	ns	
	Disable Mode	50[a]	–	–	ns	
	Maximum Frequency	–	–	48	MHz	4.75V < Vdd < 5.25V.
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	48	MHz	4.75V < Vdd < 5.25V.
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8	MHz	
SPIS	Maximum Input Clock Frequency	–	–	4	ns	
	Width of SS_ Negated Between Transmissions	50[a]	–	–	ns	
Transmitter	Maximum Input Clock Frequency	–	–	16	MHz	
Receiver	Maximum Input Clock Frequency	–	16	48	MHz	4.75V < Vdd < 5.25V.

a. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).