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Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 2x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
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13. Register Details

This chapter details all the PSoC device registers in offset order for Bank 0 and Bank 1. The registers that are in both banks are incorporated with the Bank 0 registers, designated with at least one ‘x’ in the register name and offset.

Bank 0 registers are listed first and begin on page 88. Bank 1 registers are listed second and begin on page 155. If you need a condensed view of all the registers, reference the “Register Mapping Tables” on page 83. The conventions specific to the registers in this chapter are listed below.

Table 13-1: Register Conventions

Convention	Example	Description
‘x’ in a register name	ACBxxCR1	Multiple instances/address ranges of the same register.
RW	RW : 00	Read and write register or bit(s)
R	R : 00	Read register or bit(s)
W	W : 00	Write register or bit(s)
L	RL : 00	Logical register or bit(s)
C	RC : 00	Clearable register or bit(s)
00	RW : 00	Reset value is 0x00 or 00h
xx	RW : xx	Register is not reset
0,	0,04h	Register is in bank 0
1,	1, 23h	Register is in bank 1
x,	x,F7h	Register exists in register bank 0 and register bank 1
Empty, grayed-out table cell		Reserved bit or group of bits

13.1.6 DxBxxDR1

Digital Basic/Communication Type B Block Data Register 1

Individual Register Names and Addresses

DBB00DR1 : 0,21h DBB01DR1 : 0,25h DCB02DR1 : 0,29h DCB03DR1 : 0,2Dh

	7	6	5	4	3	2	1	0
Access : POR	W : 00							
Bit Name	Data[7:0]							

The function of this register is dependant on the function its block has been configured for (selected in the FN[2:0] bits of the DxBxxFN register on page 159). For additional information, reference the "Register Definitions" on page 208 in the Digital Blocks chapter.

Bit	Name	Description
[7:0]	Data[7:0]	Data for selected function.

Block Function	Register Function
Timer	Period
Counter	Period
Dead Band	Period
CRCPRS	Polynomial
SPIM	TX Buffer
SPIS	TX Buffer
TXUART	TX Buffer
RXUART	Not applicable

13.1.13 DCBxxCR0

(SPIS Control)

Digital Communication Type B Block Control Register 0

Individual Register Names and Addresses

DCB02CR0: 0,2Bh DCB03CR0: 0,2Fh

	7	6	5	4	3	2	1	0
Access : POR	RW : 0	R : 0	R : 0	R : 1	R : 0	RW : 0	RW : 0	RW : 0
Bit Name	LSB First	Overrun	SPI Complete	TX Reg Empty	RX Reg Full	Clock Phase	Clock Polarity	Enable

The LSB First, Clock Phase, and Clock Polarity bit are configuration bits and should never be changed once the block is enabled. They can be set at the same time that the block is enabled. For additional information, reference the "Register Definitions" on page 208 in the Digital Blocks chapter.

Bit	Name	Description
[7]	**LSB First**	This bit should not be changed during an SPI transfer. 0 Data is shifted out MSB first. 1 Data is shifted out LSB first.
[6]	**Overrun**	0 No overrun has occurred. 1 Overrun has occurred. Indicates that a new byte has been received and loaded into the RX Buffer before the previous one could be read. Cleared on read of this (CR0) register.
[5]	**SPI Complete**	0 Indicates that a byte may still be in the process of shifting out or no transmission is active. 1 Indicates that a byte has been shifted out and all associated clocks have been generated. Cleared on read of this (CR0) register. Optional interrupt.
[4]	**TX Reg Empty**	The reset state and the state when the block is disabled is '1'. 0 Indicates that a byte is currently buffered in the TX register. 1 Indicates that a byte can be written to the TX register. Cleared on write of the TX Buffer (DR1) register. Default interrupt. This status will initially be asserted on block enable; however, the TX Reg Empty interrupt will occur only after the first data byte is written and transferred into the shifter.
[3]	**RX Reg Full**	0 RX register is empty. 1 A byte has been received and loaded into the RX register. Cleared on read of the RX Buffer (DR2) register.
[2]	**Clock Phase**	0 Data is latched on the leading edge of the clock. Data changes on the trailing edge. 1 Data changes on the leading edge of the clock. Data is latched on the trailing edge.
[1]	**Clock Polarity**	0 Non-inverted, clock idles low. 1 Inverted, clock idles high.
[0]	**Enable**	0 SPI Slave is not enabled. 1 SPI Slave is enabled.

13.1.23 ACBxxCR1

Analog Continuous Time Type B Block Control Register 1

Individual Register Names and Addresses

ACB00CR1 : x,72h ACB01CR1 : x,76h

	7	6	5	4	3	2	1	0
Access : POR	RW : 0	RW : 0	RW : 0			RW : 0		
Bit Name	AnalogBus	CompBus	NMux[2:0]			PMux[2:0]		

For additional information, reference the “Register Definitions” on page 257 in the Continuous Time Block chapter.

Bit	Name	Description
[7]	**AnalogBus**	Enable output to the analog bus. 0 Disable output to analog column bus. 1 Enable output to analog column bus.
[6]	**CompBus**	Enable output to the comparator bus. 0 Disable output to comparator bus. 1 Enable output to comparator bus.
[5:3]	**NMux[2:0]**	Encoding for negative input select. Note that available mux inputs vary by individual PSoC block. **ACB00 ACB01** 000b ACB01 ACB00 001b AGND AGND 010b REFLO REFLO 011b REFHI REFHI 100b FB# FB# 101b ASC10 ASD11 110b ASD11 ASC10 111b Port Inputs Port Inputs # Feedback point from tap of the feedback resistor as defined by corresponding CR0 bits [7:4] and CR3 bit 0.
[2:0]	**PMux[2:0]**	Encoding for positive input select. Note that available mux inputs vary by individual PSoC block. **ACB00 ACB01** 000b REFLO Vss 001b Port Inputs Port Inputs 010b ACB01 ACB00 011b AGND AGND 100b ASC10 ASD11 101b ASD11 ASC10 110b ABUS0 ABUS1 111b FB# FB# # Feedback point from tap of the feedback resistor as defined by corresponding CR0 bits [7:4] and CR3 bit 0.

13.1.24 ACBxxCR2

Analog Continuous Time Type B Block Control Register 2

Individual Register Names and Addresses

ACB00CR2 : x,73h ACB01CR2 : x,77h

	7	6	5	4	3	2	1	0
Access : POR	RW : 0	RW : 0	RW : 0	RW : 0	RW : 0		RW : 0	
Bit Name	CPhase	CLatch	CompCap	TMUXEN	TestMux[1:0]		PWR[1:0]	

For additional information, reference the “Register Definitions” on page 257 in the Continuous Time Block chapter.

Bit	Name	Description
[7]	**CPhase**	0 Comparator Control latch transparent on PHI1. 1 Comparator Control latch transparent on PHI2.
[6]	**CLatch**	0 Comparator Control latch is always transparent. 1 Comparator Control latch is active.
[5]	**CompCap**	0 Comparator Mode 1 Opamp Mode
[4]	**TMUXEN**	Test mux 0 Disabled 1 Enabled
[3:2]	**TestMux[1:0]**	Select block bypass mode. Note that available mux inputs vary by individual PSoC block and TMUXEN must be set. **ACB00 ACB01** 00b Positive Input to ABUS0 ABUS1 01b AGND to ABUS0 ABUS1 10b REFLO to ABUS0 ABUS1 11b REFHI to ABUS0 ABUS1
[1:0]	**PWR[1:0]**	Encoding for selecting one of four power levels. High Bias mode doubles the power at each of these settings. See bit 6 in the ARF_CR register on page 104. 00b Off 01b Low 10b Medium 11b High

13.1.41 I2C_SCR

I2C Status and Control Register

Individual Register Names and Addresses

I2C_SCR: 0,D7h

	7	6	5	4	3	2	1	0
Access : POR	RC : 0	RC : 0	RC : 0	RW : 0	RC : 0	RW : 0	RC : 0	RC : 0
Bit Name	Bus Error	Lost Arb	Stop Status	ACK	Address	Transmit	LRB	Byte Complete

Bits in this register are held in reset until one of the enable bits in I2C_CFG is set. For additional information, reference the "Register Definitions" on page 279 in the I^2C chapter.

Bit	Name	Description
[7]	**Bus Error**	0 This status bit must be cleared by firmware by writing a '0' to the bit position. It is never cleared by the hardware. 1 A misplaced Start or Stop condition was detected.
[6]	**Lost Arb**	0 This bit is set immediately on lost arbitration; however, it does not cause an interrupt. This status may be checked after the following Byte Complete interrupt. Any Start detect or a write to the Start or Restart generate bits (I2C_MSCR register), when operating in Master mode, will also clear the bit. 1 Lost Arbitration
[5]	**Stop Status**	0 This status bit must be cleared by firmware with write of '0' to the bit position. It is never cleared by the hardware. 1 A Stop condition was detected.
[4]	**ACK**	Acknowledge Out. This bit is automatically cleared by hardware on a Byte Complete event. 0 NACK the last received byte. 1 ACK the last received byte
[3]	**Address**	0 This status bit must be cleared by firmware with write of '0' to the bit position. 1 The received byte is a Slave address.
[2]	**Transmit**	This bit is set by firmware to define the direction of the byte transfer. Any Start detect or a write to the Start or Restart generate bits, when operating in Master mode, will also clear the bit. 0 Receive mode 1 Transmit mode
[1]	**LRB**	Last Received Bit. The value of the 9^{th} bit in a Transmit sequence, which is the acknowledge bit from the receiver. Any Start detect or a write to the Start or Restart generate bits, when operating in Master mode, will also clear the bit. 0 Last transmitted byte was ACKed by the receiver. 1 Last transmitted byte was NACKed by the receiver.
[0]	**Byte Complete**	Transmit/Receive Mode: 0 No completed transmit/receive since last cleared by firmware. Any Start detect or a write to the Start or Restart generate bits, when operating in Master mode, will also clear the bit. Transmit Mode: 1 Eight bits of data have been transmitted and an ACK or NACK has been received. Receive Mode: 1 Eight bits of data have been received.

13.1.49 INT_MSK1

Interrupt Mask Register 1

Individual Register Names and Addresses

INT_MSK1: 0,E1h

	7	6	5	4	3	2	1	0
Access : POR	RW : 0	RW : 0	RW : 0	RW : 0	RW : 0	RW : 0	RW : 0	RW : 0
Bit Name					DCB03	DCB02	DBB01	DBB00

Note that when an interrupt is masked off, the mask bit is '0'. The interrupt will still post in the interrupt controller. Therefore, clearing the mask bit only prevents a posted interrupt from becoming a pending interrupt. For additional information, reference the "Register Definitions" on page 55 in the Interrupt Controller chapter.

Bit	Name	Description	
[7:4]	**Reserved**		
[3]	**DCB03**	0	Mask Digital Communication Block, row 0, position 3 off.
		1	Unmask Digital Communication Block, row 0, position 3.
[2]	**DCB02**	0	Mask Digital Communication Block, row 0, position 2 off.
		1	Unmask Digital Communication Block, row 0, position 2.
[1]	**DBB01**	0	Mask Digital Basic Block, row 0, position 1 off.
		1	Unmask Digital Basic Block, row 0, position 1.
[0]	**DBB00**	0	Mask Digital Basic Block, row 0, position 0 off.
		1	Unmask Digital Basic Block, row 0, position 0.

13.1.51 RES_WDT

Reset Watchdog Timer Register

Individual Register Names and Addresses

RES_WDT: 0,E3h

	7	6	5	4	3	2	1	0
Access : POR	W : 00							
Bit Name	WDSL_Clear[7:0]							

For additional information, reference the “Register Definitions” on page 77 in the Sleep and Watchdog chapter.

Bit	Name	Description
[7:0]	**WDSL_Clear[7:0]**	Any write clears the Watchdog timer. A write of 38h clears both the Watchdog and Sleep timers.

13.1.57 MUL_Y

Multiply Input Y Register

Individual Register Names and Addresses

MUL_Y: 0,E9h

	7	6	5	4	3	2	1	0
Access : POR	W : 00							
Bit Name	Data[7:0]							

For additional information, reference the “Register Definitions” on page 270 in the Multiply Accumulate chapter.

Bit	Name	Description
[7:0]	**Data[7:0]**	Y multiplicand for MAC 8-bit multiplier.

13.1.60 MAC_X/ACC_DR1

Accumulator Data Register 1

Individual Register Names and Addresses

MAC_X/ACC_DR1: 0,ECh

	7	6	5	4	3	2	1	0
Access : POR	RW : 00							
Bit Name	Data[7:0]							

For additional information, reference the “Register Definitions” on page 270 in the Multiply Accumulate chapter.

Bit	Name	Description	
[7:0]	**Data[7:0]**	Read	Low byte of the MAC Accumulator sum. Returns the 2nd byte of the 32-bit accumulated value. The 2nd byte is next to the least significant byte for the accumulated value.
		Write	X multiplicand for the MAC 16-bit multiply and 32-bit accumulator.

13.2.5 DxBxxFN

Digital Basic/Communications Type B Block Function Register

Individual Register Names and Addresses

DBB00FN : 1,20h DBB01FN : 1,24h DCB02FN : 1,28h DCB03FN : 1,2Ch

	7	6	5	4	3	2	1	0
Access : POR	RW : 0	RW : 0	RW : 0	RW : 0		RW : 0		
Bit Name	Data Invert	BCEN	End/Single	Mode[1:0]		Function[2:0]		

Before changing any of the configuration registers (DxBxxFN, DxBxxIN, and DxBxxOU), disable the corresponding digital block by setting bit 0 in the CR0 or DxBxxCR0 register to '0'. The values in the DxBxxFN register should not be changed while the block is enabled. After all configuration changes are made, enable the block by setting bit 0 in the DxBxxCR0 register to '1'.

For additional information, reference the "Register Definitions" on page 208 in the Digital Blocks chapter.

Bit	Name	Description
[7]	**Data Invert**	0 Data input is non-inverted. 1 Data input is inverted.
[6]	**BCEN**	Enable Primary Function Output to drive the broadcast net. 0 Disable 1 Enable
[5]	**End/Single**	0 Block is not the end of a chained function or the function is not chainable. 1 Block is the end of a chained function or a standalone block in a chainable function.
[4:3]	**Mode[1:0]**	(Function Dependent)
	Timer or Counter:	*Mode[0] signifies the interrupt type.* 0 Interrupt on Terminal Count 1 Interrupt on Compare True *Mode[1] signifies the compare type.* 0 Compare on Less Than or Equal 1 Compare on Less Than
	CRCPRS:	*Mode[1:0] are encoded as the Compare Type.* 00b Compare on Equal 01b Compare on Less Than or Equal 10b Reserved 11b Compare on Less Than
	Dead Band:	*Mode[1:0] are encoded as the Kill Type.* 00b Synchronous Restart KILL mode 01b Disable KILL mode 10b Asynchronous KILL mode 11b Reserved

(continued on next page)

13.2.27 BDG_TR

Bandgap Trim Register

Individual Register Names and Addresses

BDG_TR: 1,EAh

	7	6	5	4	3	2	1	0
Access : POR		RW : 0	RW : 1		RW : 8			
Bit Name		AGNDBYP	TC[1:0]		V[3:0]			

For additional information, reference the “Register Definitions” on page 293 in the Internal Voltage Reference chapter.

Bit	Name	Description
[7]	**Reserved**	
[6]	**AGNDBYP**	If set, an external bypass capacitor on AGND may be connected to Port 2[4]. 0 Disable 1 Enable
[5:4]	**TC[1:0]**	The value of these bits is used to trim the temperature coefficient. Their value is set to the best value for the device during boot. ***The value of these bits should not be changed.***
[3:0]	**V[3:0]**	The value of these bits is used to trim the bandgap reference. Their value is set to the best value for the device during boot. ***The value of these its should not be changed.***

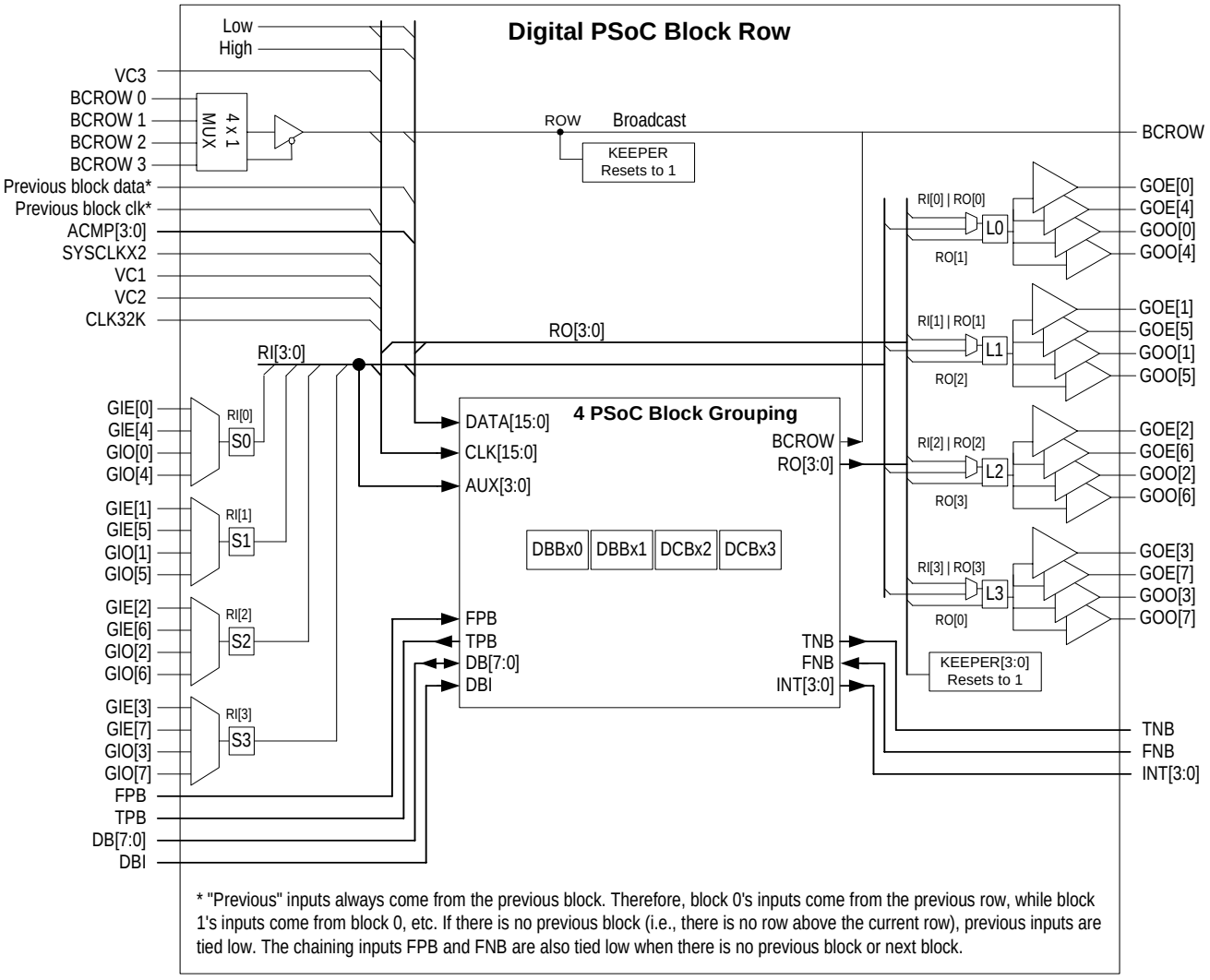

Figure 16-2. Digital PSoC Block Row Structure

plexer are intended to be a selection of GPIO inputs (row inputs).

Note 1 If the input data source for a given block comes from another block, the destination block must be enabled prior to the source block being enabled.

17.1.2 Input Clock Resynchronization

Digital blocks allow a clock selection from one of 16 sources. Possible sources are the system clocks (VC1, VC2, VC3, SYSCLK, and SYSCLKX2), pin inputs, and other digital block outputs. To manage clock skew and ensure that the interfaces between blocks meet timing in all cases, all digital block input clocks must be resynchronized to either SYSCLK or SYSCLKX2, which are the source clocks for all chip clocking. Also, SYSCLK or SYSCLKX2 may be used directly. The AUXCLK bits in the DxBxxOU register are used to specify the input synchronization. The following rules apply to the use of input clock resynchronization.

1. If the clock input is derived (e.g., divided down) from SYSCLK, re-synchronize to SYSCLK at the digital block. Most chip clocks are in this category. For example, VC1 and VC2, and the output of other blocks clocked by VC1 and VC2 or SYSCLK (setting 01 in AUXCLK).
2. If the clock input is derived from SYSCLKX2, re-synchronize to SYSCLKX2. For example, VC3 clocked by SYSCLKX2, or other digital blocks clocked by SYSCLKX2 (setting 10 in AUXCLK).
3. Choose direct SYSCLK (setting 11 in AUXCLK).
4. Choose direct SYSCLKX2 (select SYSCLKX2 in the Clock Input field of the DxBxxIN register).
5. Bypass synchronization. This should be a very rare selection. Because if clocks are not synchronized, they may fail setup to CPU read and write commands. However, it is possible for an external pin to asynchronously clock a digital block. For example, if the user is willing to synchronize CPU interaction through interrupts or other techniques (setting 00 in AUXCLK).

The following notes enumerate configurations that are not allowed, although the hardware does not prevent them. The summary of these notes is that the clock dividers (VC1, VC2, and VC3) may not be configured in such a way as to create an output clock that is equal to SYSCLK or SYSCLKX2.

Note 1 When VC1 is configured to divide by one, choosing an input clock of VC1 is not allowed. This configuration produces a clock frequency that is equal to SYSCLK; therefore, SYSCLK direct should be used by setting the AUXCLK bits in DxBxOU to 11b.

Note 2 When both VC2 and VC1 are configured to divide by one, choosing an input clock of VC2 is not allowed. This configuration produces a clock frequency that is equal to SYSCLK; therefore, SYSCLK direct should be used by setting the AUXCLK bits in DxBxOU to 11b.

Note 3 When VC3 is configured to divide by one with a source clock of SYSCLK, choosing an input clock of VC3 is not allowed. This configuration produces a clock frequency that is equal to SYSCLK. There are two other VC3 configurations to avoid that will result in an output frequency equal to SYSCLK. The first is when VC3 is configured to divide by one with a source clock of VC1 divide by one. The second is when VC3 is configured to divide by one with a source clock of VC2 divide by one and VC1 is also configured to divide by one. All of these configurations result in a VC3 frequency equal to SYSCLK and this is not allowed. When a frequency equal to SYSCLK is desired, SYSCLK direct should be used by setting the AUXCLK bits in DxBxOU to 11b.

Note 4 When VC3 is configured to divide by one with a source clock of SYSCLKX2, choosing an input clock of VC3 is not allowed. This configuration produces a clock frequency that is equal to SYSCLKX2. When a frequency equal to SYSCLKX2 is desired, SYSCLKX2 should be selected by setting the Clock Input bits of the DxBxxIN register to 4h and the AUXCLK bits of DxBxOU to 00b.

All of these issues have been addressed in the actual clock resynchronizer, illustrated in Figure 17-1.

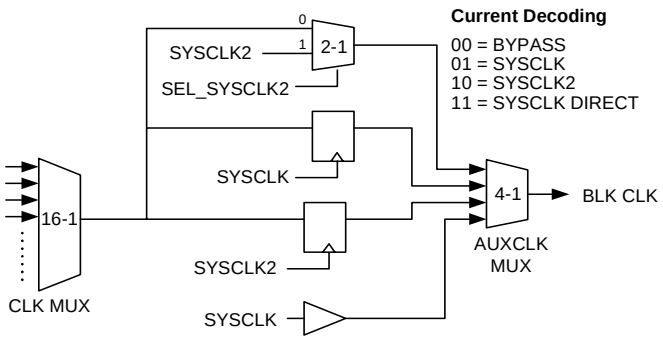

Figure 17-1. Input Clock Resynchronization

Table 17-2: AUXCLK Bit Selections

Code	Description	Usage
00	Bypass	Use this setting only for asynchronous inputs. Also used when SYSCLK2 (48 MHz) is selected.
01	Resync to SYSCLK (24 MHz)	Use this setting for any SYSCLK based clock. VC1, VC2, VC3 driven by SYSCLK, digital blocks with SYSCLK based source clocks, broadcast bus with source based on SYSCLK, row input and row outputs with source based on SYSCLK.
10	Resync to SYSCLK2 (48 MHz)	Use this setting for any SYSCLK2 based clock. VC3 driven by SYSCLK2, digital blocks with SYSCLK2 based source clocks, broadcast bus with source based on SYSCLK2, row input and row outputs with source based on SYSCLK2.
11	SYSCLK Direct	Use this setting to clock the block directly using SYSCLK. Note that this setting is not strictly related to clock resynchronization, but since SYSCLK cannot resync itself, it allows a direct skew controlled SYSCLK source.

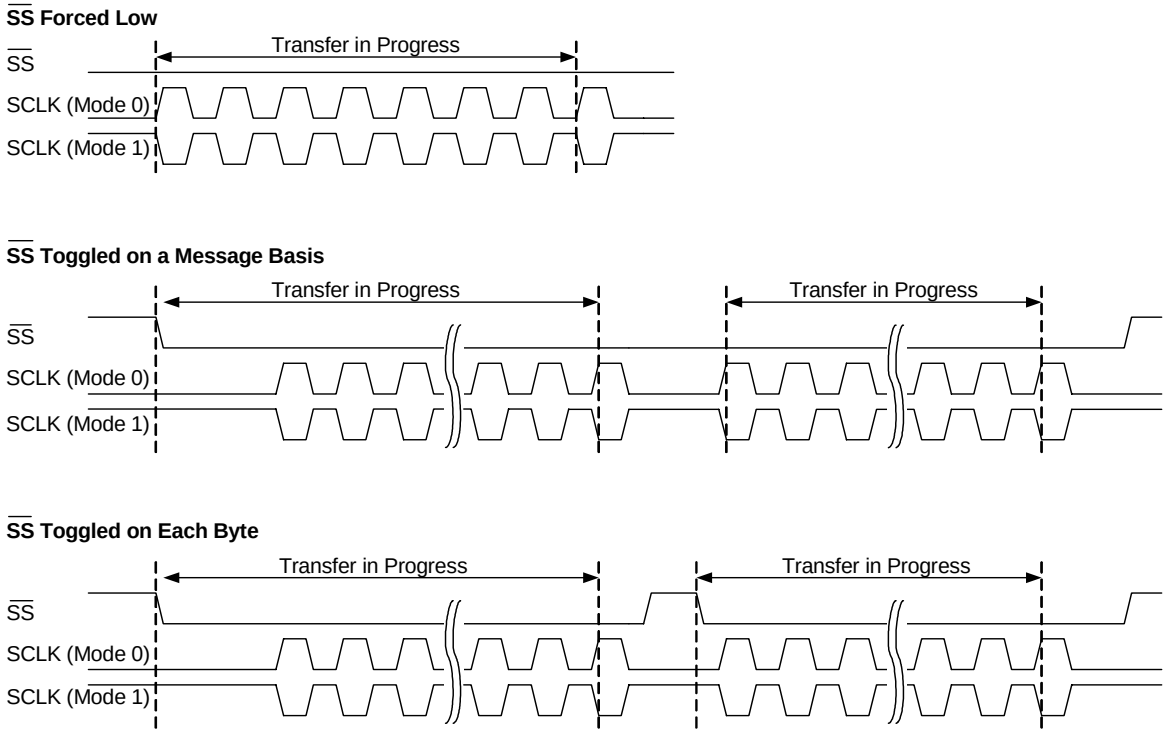

Figure 17-21. Mode 0 and 1 Transfer in Progress

Figure 17-22 illustrates TX data loading in modes 2 and 3. In this case, a transfer in progress is defined to be from the leading edge of the 1st SCLK, to the point at which the RX Buffer register is loaded with the received byte. Loading the shifter by the leading edge of the clock has the effect of providing the required one-half clock setup time, as the data is latched into the receiver on the trailing edge of the SCLK in these modes.

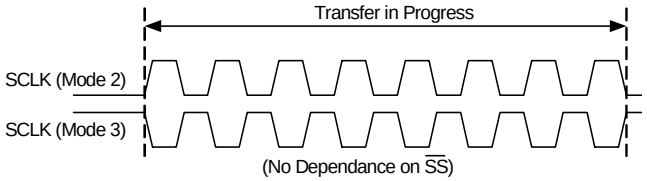

Figure 17-22. Mode 2 and 3 Transfer in Progress

21. Analog Reference

This chapter discusses the Analog Reference generator and its associated register. The reference generator establishes a set of three internally fixed reference voltages for AGND, RefHi, and RefLo.

Table 21-1. Analog Reference Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
0,63h	ARF_CR		HBE	REF[2:0]			PWR[2:0]			RW : 00

21.1 Architectural Description

The PSoC device is a single supply part, with no negative voltage available or applicable. Analog ground (AGND) is constructed near mid-supply. This ground is routed to all analog blocks and separately buffered within each block. Note that there may be a small offset voltage between buffered analog grounds. RefHi and RefLo signals are generated, buffered, and routed to the analog blocks. RefHi and RefLo are used to set the conversion range (i.e., span) of analog to digital (ADC) and digital to analog (DAC) converters. RefHi and RefLo can also be used to set thresholds in comparators.

The reference array supplies voltage to all blocks and current to the Switched Capacitor blocks. At higher block clock rates, there is increased reference current demand; the reference power should be set equal to the highest power level of the analog blocks used.

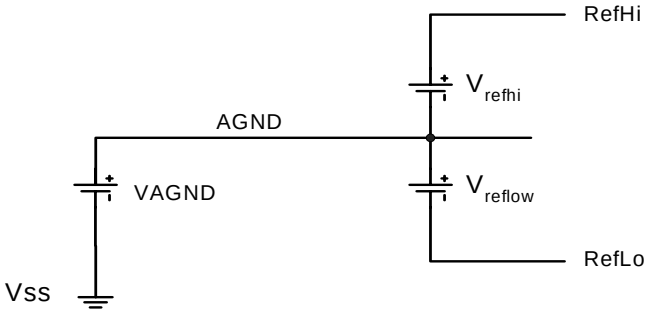

Figure 21-1. Reference Structure

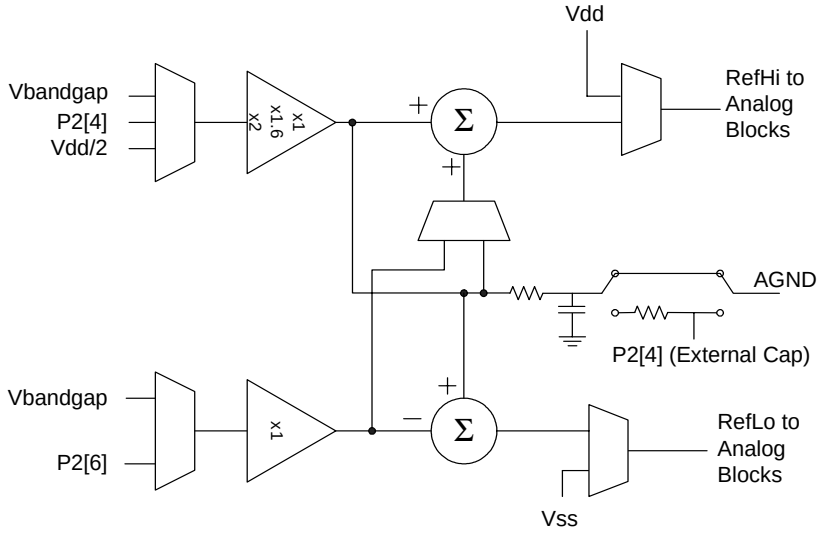

Figure 21-2. Analog Reference Control Schematic

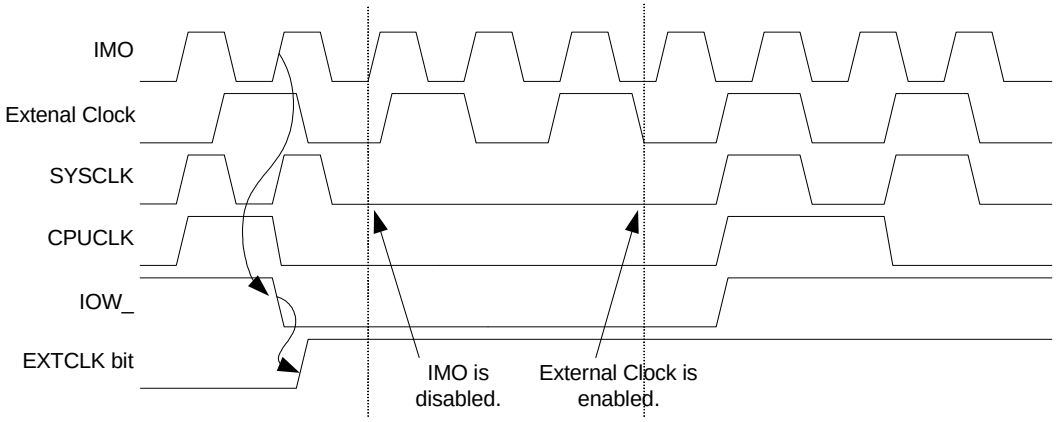

Figure 24-3. Switch from IMO to the External Clock with a CPU Clock Divider of Two or Greater

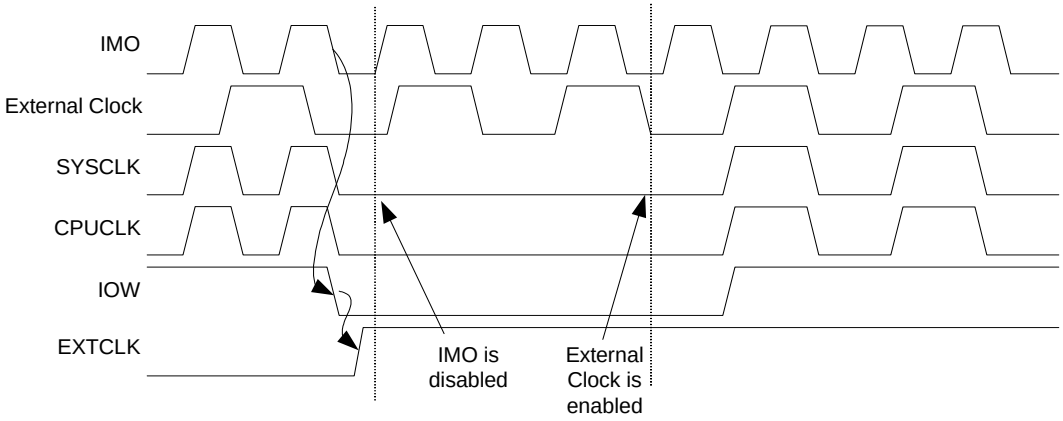

Figure 24-4. Switch from IMO to External Clock with the CPU Running with a CPU Clock Divider of One

24.2.6 OSC_CR3 Register

Bits 7 to 0: VC3 Divider[7:0]. As an example of the flexibility of the clocking structure in PSoC devices, consider a device that is running off of an externally supplied clock at a frequency of 93.7 kHz. This clock value may be divided by the VC1 divider to achieve a VC1 clock net frequency of 5.89 kHz. The VC2 divider could reduce the frequency by another factor of 16, resulting in a VC2 clock net frequency of 366.02 Hz. Finally, the VC3 divider may choose VC2 as its input clock and divide by 256, resulting in a VC3 clock net frequency of 1.43 Hz.

Table 24-6. OSC_CR3[7:0] Bits: VC3 Divider Value

	Divider Source Clock			
Bits	**SYSCLKX2**	**SYSCLK**	**VC1**	**VC2**
00h	SYSCLKX2	SYSCLK	VC1	VC2
01h	SYSCLKX2 / 2	SYSCLK / 2	VC1 / 2	VC2 / 2
02h	SYSCLKX2 / 3	SYSCLK / 3	VC1 / 3	VC2 / 3
03h	SYSCLKX2 / 4	SYSCLK / 4	VC1 / 4	VC2 / 4
...	...	...	...	...
FCh	SYSCLKX2 / 253	SYSCLK / 253	VC1 / 253	VC2 / 253
FDh	SYSCLKX2 / 254	SYSCLK / 254	VC1 / 254	VC2 / 254
FEh	SYSCLKX2 / 255	SYSCLK / 255	VC1 / 255	VC2 / 255
FFh	SYSCLKX2 / 256	SYSCLK / 256	VC1 / 256	VC2 / 256

As mentioned previously the VC3 clock net can generate a system interrupt. Once the input clock and the divider value for the VC3 clock are chosen, only one additional step is needed to enable the interrupt; the VC3 mask bit needs to be set in register INT_MSK0[7]. Once the VC3 mask bit is set, the VC3 clock generates pending interrupts every number of clock periods equal to the VC3 divider register value plus one. Therefore, if the VC3 divider register's value is 05h (divide by 6), an interrupt would occur every six periods of the VC3's input clock. Another example would be if the divider value was 00h (divide by 1), an interrupt would be generated on every period of the VC3 clock. The VC3 mask bit only controls the ability of a posted interrupt to become pending. Because there is no enable for the VC3 interrupt, VC3 interrupts will always be posting. See the Interrupt Controller chapter for more information on posting and pending.

For additional information, reference the OSC_CR3 register on page 175.

24.2.7 OSC_CR4 Register

Bits 7 to 2: Reserved.

Bits 1 and 0: VC3 Input Select [1:0]. The VC3 clock net is the only clock net with the ability to generate an interrupt. The VC3 is most similar to the VC2 in that its input clock comes from a configurable source. As shown in Figure 24-1 on page 263, a 4-to-1 multiplexer determines the clock that will be used as in the input to the VC3 divider. The multiplexer allows either the 48 MHz, 24 MHz, VC1, or VC2 clocks to be used as the input clock to the divider. Because the selection of a clock for the VC3 divider is performed by a simple 4-to-1 mux, runt pulses and glitches may be injected to the VC3 divider when the OSC_CR4[1:0] bits are changed. Care should be taken to ensure that blocks using the VC3 clock are either disabled when OSC_CR4[1:0] is changed or not sensitive to glitches. Unlike the VC1 and VC2 clock dividers, the VC3 clock divider is 8-bits wide. Therefore, there are 256 valid divider values as indicated by Table 24-6.

Table 24-7. OSC_CR4[1:0] Bits: VC3

Bits	Multiplexer Output
00b	SYSCLK
01b	VC1
10b	VC2
11b	SYSCLKX2

It is important to remember that even though the VC3 divider has four choices for input clock, none of the choices have fixed frequencies for all device configurations. Both the 24 MHz and 48 MHz clocks may have very different frequencies, if an external clock is in use. Also, the divider values for the VC1 and VC2 inputs to the multiplexer must be considered.

For additional information, reference the OSC_CR4 register on page 174