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Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 2x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24223-24pvit

11. Phase Locked Loop (PLL)

This chapter briefly presents the Phase Locked Loop (PLL) and its associated registers.

Table 11-1. Phase Locked Loop Registers

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
1,E0h	OSC_CR0	32k Select	PLL Mode	No Buzz	Sleep[1:0]		CPU Speed[2:0]			RW : 00
1,E2h	OSC_CR2	PLLGAIN					EXTCLKEN	IMODIS	SYSCLKX2 DIS	RW : 00

11.1 Architectural Description

A Phase-Locked Loop (PLL) function generates the system clock with crystal accuracy. It is designed to provide a 23.986 MHz oscillator when utilized with an external 32.768 kHz crystal.

Although the PLL tracks crystal accuracy, it requires time to lock onto the reference frequency when first starting. The length of time depends on the PLLGAIN controlled by bit 7 of the OSC_CR2 register. If this bit is held low, the lock time will be less than 10 ms. If this bit is held high, the lock time will be on the order of 50 ms. After lock is achieved, it is recommended that this bit be forced high to decrease the jitter on the output. If longer lock time is tolerable, the PLLGAIN bit can be held high all the time.

After the External Crystal Oscillator has been selected and enabled, the following procedure should be followed to enable the PLL and allow for proper frequency lock.

- Select a CPU frequency of 3 MHz or less.
- Enable the PLL.
- Wait between 10 and 50 ms, depending on the OSC_CR2 register bit 7.
- Set CPU to a faster frequency, if desired. To do this, write the bits CPU Speed[2:0] in the OSC_CR0 register. The CPU frequency will immediately change when these bits are set.

If the proper settings are selected in PSoC Designer, the above steps are automatically done in boot.asm.

11.2 Register Definitions

11.2.1 OSC_CR0 Register

Bit 7: 32k Select. By default, the 32 kHz clock source is the Internal Low-Speed Oscillator (ILO). Optionally, the External Crystal Oscillator (ECO) may be selected.

Bit 6: PLL Mode. This is the only bit in the OSC_CR0 register that directly influences the PLL. When set, this bit enables the PLL. The EXTCLKEN bit in the OSC_CR2 register should be set low during PLL operation.

Bit 5: No Buzz. Normally, when the Sleep bit is set in the CPU_SCR register, all chip systems are powered down, including the Band Gap reference. However, to facilitate the detection of POR and LVD events at a rate higher than the Sleep Interval, the Band Gap circuit is powered up periodically for about 60 us at the Sleep System Duty cycle (set in ECO_TR), which is independent of the Sleep Interval and typically higher. When the No Buzz bit is set, the Sleep System Duty Cycle value is overridden, and the Band Gap circuit is forced to be on during sleep. This results in faster response to an LVD or POR event (continuous detection as opposed to periodic), at the expense of slightly higher average sleep current.

Bits 4 and 3: Sleep[1:0]. The available sleep interval selections are shown in Table 11-2. It must be remembered that when the ILO is the selected 32 kHz clock source, sleep intervals are approximate.

13.1.18 CMP_CR0

Analog Comparator Bus 0 Register

Individual Register Names and Addresses

CMP_CR0: 0,64h

	7	6	5	4	3	2	1	0
Access : POR			R : 0	R : 0			RW : 0	RW : 0
Bit Name			COMP[1]	COMP[0]			AINT[1]	AINT[0]

For additional information, reference the “Register Definitions” on page 238 in the Analog Interface chapter.

Bit	Name	Description
[7:6]	**Reserved**	
[5]	**COMP[1]**	Comparator bus state for column 1. This bit is updated on the rising edge of PHI2, unless the comparator latch disable bits are set. If the comparator latch disable bits are set, then this bit is transparent to the comparator bus in the analog array.
[4]	**COMP[0]**	Comparator bus state for column 0. This bit is updated on the rising edge of PHI2, unless the comparator latch disable bits are set. If the comparator latch disable bits are set, then this bit is transparent to the comparator bus in the analog array.
[3:2]	**Reserved**	
[1]	**AINT[1]**	Controls the selection of the analog comparator interrupt for column 1. 0 The comparator data bit from the column is the input to the interrupt controller. 1 The falling edge of PHI2 for the column is the input to the interrupt controller.
[0]	**AINT[0]**	Controls the selection of the analog comparator interrupt for column 0. 0 The comparator data bit from the column is the input to the interrupt controller. 1 The falling edge of PHI2 for the column is the input to the interrupt controller.

13.1.33 RDIxRI

Row Digital Interconnect Row Input Register

Individual Register Names and Addresses

RDI0RI : x,B0h

	7	6	5	4	3	2	1	0
Access : POR	RW : 0		RW : 0		RW : 0		RW : 0	
Bit Name	RI3[2:0]		RI2[2:0]		RI1[2:0]		RI0[2:0]	

For additional information, reference the “Register Definitions” on page 196 in the Row Digital Interconnect chapter.

Bit	Name	Description
[7:6]	**RI3[2:0]**	Select source for row input 3. 00b GIE[3] 01b GIE[7] 10b GIO[3] 11b GIO[7]
[5:4]	**RI2[2:0]**	Select source for row input 2. 00b GIE[2] 01b GIE[6] 10b GIO[2] 11b GIO[6]
[3:2]	**RI1[2:0]**	Select source for row input 1. 00b GIE[1] 01b GIE[5] 10b GIO[1] 11b GIO[5]
[1:0]	**RI0[2:0]**	Select source for row input 0. 00b GIE[0] 01b GIE[4] 10b GIO[0] 11b GIO[4]

13.1.45 INT_CLR1

Interrupt Clear Register 1

Individual Register Names and Addresses

INT_CLR1: 0,DBh

	7	6	5	4	3	2	1	0
Access : POR					RW : 0	RW : 0	RW : 00	RW : 0
Bit Name					DCB03	DCB02	DBB01	DBB00

When bits in this register are read, a ‘1’ will be returned for every bit position that has a corresponding posted interrupt. When bits in this register are written with a zero (0) and ENSWINT is not set, posted interrupts will be cleared at the corresponding bit positions. If there was not a posted interrupt, there is no effect. When bits in this register are written with a one (1) and ENSWINT is set, an interrupt is posted in the interrupt controller. Note that the ENSWINT bit is in the INT_MSK3 register on page 135. For additional information, reference the “Register Definitions” on page 55 in the Interrupt Controller chapter.

Bit	Name	Description
[7:4]	**Reserved**	
[3]	**DCB03**	Digital Communications Block type B, row 0, position 3. Read 0 No posted interrupt. Read 1 Posted interrupt present. Write 0 AND ENSWINT = 0 Clear posted interrupt if it exists. Write 1 AND ENSWINT = 0 No effect. Write 0 AND ENSWINT = 1 No effect. Write 1 AND ENSWINT = 1 Post an interrupt.
[2]	**DCB02**	Digital Communications Block type B, row 0, position 2. Read 0 No posted interrupt. Read 1 Posted interrupt present. Write 0 AND ENSWINT = 0 Clear posted interrupt if it exists. Write 1 AND ENSWINT = 0 No effect. Write 0 AND ENSWINT = 1 No effect. Write 1 AND ENSWINT = 1 Post an interrupt.
[1]	**DBB01**	Digital Basic Block type B, row 0, position 1. Read 0 No posted interrupt. Read 1 Posted interrupt present. Write 0 AND ENSWINT = 0 Clear posted interrupt if it exists. Write 1 AND ENSWINT = 0 No effect. Write 0 AND ENSWINT = 1 No effect. Write 1 AND ENSWINT = 1 Post an interrupt.
[0]	**DBB00**	Digital Basic Block type B, row 0, position 0. Read 0 No posted interrupt. Read 1 Posted interrupt present. Write 0 AND ENSWINT = 0 Clear posted interrupt if it exists. Write 1 AND ENSWINT = 0 No effect. Write 0 AND ENSWINT = 1 No effect. Write 1 AND ENSWINT = 1 Post an interrupt.

13.1.63 MAC_CL1/ACC_DR2

Accumulator Data Register 2

Individual Register Names and Addresses

MAC_CL1/ACC_DR2: 0,EFh

	7	6	5	4	3	2	1	0
Access : POR	RW : 00							
Bit Name	Data[7:0]							

For additional information, reference the “Register Definitions” on page 270 in the Multiply Accumulate chapter.

Bit	Name	Description	
[7:0]	**Data[7:0]**	Read	Returns the 3rd byte of the 32-bit accumulated value. The 3rd byte is the next to most significant byte for the accumulated value.
		Write	Writing any value to this address will clear all four bytes of the Accumulator.

13.2.7 DxBxxOU *(continued)*

[1:0] **Output Select[1:0]** Row Output Select for Primary Function Output

00b Row Output 0
01b Row Output 1
10b Row Output 2
11b Row Output 3

13.2.22 OSC_CR2

Oscillator Control Register 2

Individual Register Names and Addresses

OSC_CR2: 1,E2h

	7	6	5	4	3	2	1	0
Access : POR	RW : 0					RW : 0	RW : 0	RW : 0
Bit Name	PLLGAIN					EXTCLKEN	IMODIS	SYSCLKX2DIS

Note that in OCD mode (OCDM=1), bits [1:0] have no effect. For additional information, reference the “Register Definitions” on page 266 in the Digital Clocks chapter.

Bit	Name	Description
[7]	**PLLGAIN**	Phase locked loop gain. 0 Recommended value, normal gain. 1 Reduced gain to make PLL more tolerant to noisy or jittery crystal input.
[6:3]	**Reserved**	
[2]	**EXTCLKEN**	External clock mode enable. 0 Disabled. Operate from internal main oscillator. 1 Enabled. Operate from clock supplied at port P1[4].
[1]	**IMODIS**	Internal oscillator disable. Can be set to save power when using an external clock on P1[4]. 0 Enabled. Internal oscillator enabled. 1 Disabled, if SYSCLKX2DIS is set (1).
[0]	**SYSCLKX2DIS**	48 MHz clock source disable. 0 Enabled. If enabled, the 48 MHz clock is forced on. 1 Disabled for power reduction.

14. Global Digital Interconnect (GDI)

This chapter discusses the Global Digital Interconnect (GDI) and its associated registers. GDI is the most general level of interconnect configuration available in the PSoC Mixed Signal Arrays.

Table 14-1. Global Digital Interconnect (GDI) Registers

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
1,D0h	GDI_O_IN	GIONOUT7	GIONOUT6	GIONOUT5	GIONOUT4	GIONOUT3	GIONOUT2	GIONOUT1	GIONOUT0	RW : 00
1,D1h	GDI_E_IN	GIENOUT7	GIENOUT6	GIENOUT5	GIENOUT4	GIENOUT3	GIENOUT2	GIENOUT1	GIENOUT0	RW : 00
1,D2h	GDI_O_OU	GOOUTIN7	GOOUTIN6	GOOUTIN5	GOOUTIN4	GOOUTIN3	GOOUTIN2	GOOUTIN1	GOOUTIN0	RW : 00
1,D3h	GDI_E_OU	GOEUTIN7	GOEUTIN6	GOEUTIN5	GOEUTIN4	GOEUTIN3	GOEUTIN2	GOEUTIN1	GOEUTIN0	RW : 00

Global Digital Interconnect (GDI) consists of four 8-bit busses. Two of the busses are input busses, which allow signals to pass from the device pins to the core of the chip. These busses are called Global Input Odd (GIO[7:0]) and Global Input Even (GIE[7:0]). The other two busses are output busses and allow signals to pass from the core of the chip to the device pins. They are called Global Output Odd (GOO[7:0]) and Global Output Even (GOE[7:0]). The word “odd” or “even” in the bus name indicates which device ports the bus connects to. Busses with odd in their name connect to all odd numbered ports and busses with even in their name connect to all even numbered ports. Note that the word odd or even in the bus name refers to ports and not pins.

There are two ends to the global digital interconnect core signals and port pins. An end may be configured as a source or a destination. For example, a GPIO pin may be configured to drive a global input or receive its output from a global output. Currently there are two types of core signals connected to the global busses. The digital blocks, which may be a source or a destination for a global net, and system clocks, which may only drive global nets.

For the PSoC chips in the PSoc Mixed Signal Array family, there are two 8-bit ports. Therefore, there is one port connected to the even global busses and one port connected to the odd global busses. Table 14-2 lists the mapping between global busses and ports.

Table 14-2. Global Bus to Port Mapping

Global Buss	Ports
GIO[7:0], GOO[7:0]	P1
GIE[7:0], GOE[7:0]	P0

Because only one port is connect to each global input/output pair, the PSoC device does not have the one-to-many relationship between globals and port pins that the CY8C27xxx has. For example, if GIO[1] is used to bring an input signal into a digital PSoC block, only pin P1[1] may be used. The same is true for the outputs. For example, if GOE[3] is used to carry a signal from a digital PSoC block to a port pin, only P0[3] may be used.

14.1 Architectural Description

The primary goal, of the architectural block diagram that follows, is to communicate the relationship between global busses (GOE, GOO, GIE, GIO) and pins. Note that any global input may be connected to its corresponding global output, using the tri-state buffers located in the corners of the figure. Also, global outputs may be shorted to global inputs using these tri-state buffers. The rectangle in the center of the figure represents the array of digital PSoC blocks.

In Figure 15-1, the detailed view of a Digital PSoC block row has been replaced by a box labeled “Digital PSoC Block Row.” The rest of this figure illustrates how all rows are connected to the same globals, clocks, and so on. The figure also illustrates how the broadcast clock nets (BCxxxx) are connected between rows.

17.1.5 Timer Function

A timer consists of a period register, a synchronous down counter, and a capture/compare register, all of which are byte wide. When the timer is disabled and a period value is written into DR1, the period value is also loaded into DR0. When the timer is enabled, the counter counts down until positive terminal count (a count of 00h) is reached. On the next clock edge, the period is reloaded and on subsequent clocks counting continues. The terminal count signal is the primary function output.

Hardware capture occurs on the positive edge of the data input. This event transfers the current count from DR0 to DR2. The captured value may then be read directly from DR2. A software capture function is equivalent to a hardware capture. A CPU read of DR0, with the timer enabled, triggers the same capture mechanism. The hardware and software capture mechanisms are OR'ed in the capture circuitry. Since the capture circuitry is positive edge sensitive, during an interval where the hardware capture input is high, a software capture is masked and will not occur.

The Timer also implements a compare function between DR0 and DR2. The compare signal is the auxiliary function output. A limitation, in regards to the compare function, is that the capture and compare function both use the same register (DR2). Therefore, if a capture event occurs, it will overwrite the compare value.

Mode bit 1 in the Function register sets the compare type (DR0 <= DR2 or DR0 < DR2) and Mode bit 0 sets the interrupt type (Terminal Count or Compare).

Timers may be chained in 8-bit lengths up to 32 bits.

17.1.5.1 Usability Exceptions

The following are usability exceptions for the Timer function.

1. Capture operation is not supported at 48 MHz.
2. DR2 is not writeable when the Timer is enabled.

17.1.5.2 Block Interrupt

The Timer block has a selection of three interrupt sources. Interrupt on Terminal Count (TC) and Compare may be selected in Mode bit 0 of the Function register. The interrupt on Capture may be selected with the Capture Interrupt bit in the Control register.

- Interrupt on Terminal Count: The positive edge of Terminal Count (primary output) generates an interrupt for this block. The timing of the interrupt follows the TC Pulse Width setting in the Control register.
- Interrupt on Compare: The positive edge of Compare (auxiliary output) generates an interrupt for this block.
- Interrupt on Capture: Hardware or software capture generates an interrupt for this block. The interrupt occurs at closing of the DR2 latch on capture.

17.1.6 Counter Function

A Counter consists of a period register, a synchronous down counter, and a compare register. The Counter function is identical to the Timer function except for the following points:

- The Data input is a counter gate (enable), rather than a capture input. Counters do not implement synchronous capture. The DR0 register in a counter should not be read when it is enabled.
- The Compare output is the primary output and the Terminal Count is the auxiliary output (opposite of the Timer).
- Terminal Count output is full cycle only.

When the Counter is disabled and a period value is written into DR1, the period value is also loaded into DR0. When the Counter is enabled, the counter counts down until terminal count (a count of 00h) is reached. On the next clock edge, the period is reloaded and, on subsequent clocks, counting continues.

The Counter implements a compare function between DR0 and DR2. The Compare signal is the primary function output. Mode bit 1 sets the compare type (DR0 <= DR2 or DR0 < DR2) and Mode bit 0 sets the interrupt type (Terminal Count or Compare).

The data input functions as a gate to counter operation. The counter will only count and reload when the data input is asserted (logic '1'). When the data input is negated (logic '0'), counting (including the period reload) is halted.

Counters may be chained in 8-bit blocks up to 32 bits.

17.1.6.1 Usability Exceptions

The following are usability exceptions for the Counter function.

1. DR0 may only be read (to transfer DR0 data to DR2) when the block is disabled.

17.1.6.2 Block Interrupt

The Counter block has a selection of three interrupt sources. Interrupt on Terminal Count and Compare may be selected in Mode bit 0 of the Function register.

- Interrupt on Terminal Count: The positive edge of Terminal Count (auxiliary output) generates an interrupt for this block. The timing of the interrupt follows the TC Pulse Width setting in the Control register.
- Interrupt on Compare: The positive edge of Compare (primary output) generates an interrupt for this block.

17.2.2 DxBxxCR0 Register

The DxBxxCR0 register is the digital blocks' control register. It is described by function in Table 17-14. For additional information, reference the DxBxxCR0 register on page 95.

Table 17-14. DxBxxCR0 Register Description

Function	Description
Timer	There are three bits in the Control (CR0) register: one for enabling the block, one for setting the optional interrupt on capture, and one to select between one-half and a full clock for terminal count output.
Counter	One bit enable only.
Dead Band	There are three bits in the Control (CR0) register: one bit for enabling the block, and two bits to enable and control Dead Band Bit Bang mode. When Bit Bang mode is enabled, the output of this register is substituted for the PWM reference. This register may be toggled by user firmware, to generate PHI1 and PHI2 output clock with the programmed dead time. The options for Bit Bang mode are as follows: 0 Function uses the previous clock primary output as the input reference. 1 Function uses the Bit Bang Clock register as the input reference.
CRCPRS	Two bits are used to enable operation.
SPIM	The SPI Control (CR0) register contains both control and status bits. There are four control bits that are read/write: Enable, Clock Phase and Clock Polarity to set the mode, and LSB First, which controls bit ordering. There are two read-only status bits: Overrun and SPI Complete. There are two additional read-only status bits to indicate TX and RX Buffer status.
SPIS	The SPI Control (CR0) register contains both control and status bits. There are four control bits that are read/write: Enable, Clock Phase and Clock Polarity to set the mode, and LSB First, which controls bit ordering. There are two read-only status bits: Overrun and SPI Complete. There are two additional read-only status bits to indicate TX and RX Buffer status.
TXUART	The Transmitter Control (CR0) register contains three control bits and two status bits. The control bits are Enable, Parity Enable, and Parity Type, and have read/write access. The status bits, TX Reg Empty and TX Complete, are read-only.
RXUART	The Receiver Control (CR0) register contains both control and status bits. Three control bits are read/write: Enable, Parity Enable, and Parity Type. There are five read-only status bits: RX Reg Full, RX Active, Framing Error, Overrun, and Parity Error.

Interrupt Mask Register

17.2.3 INT_MSK1 Register

The INT_MSK1 register is described in the "Interrupt Controller" chapter on page 53. For additional information, reference the INT_MSK1 register on page 137.

Configuration Registers

The Configuration block contains 3 registers: Function (DxBxxFN), Input (DxBxxIN), and Output (DxBxxOU). The values in these registers should not be changed while the block is enabled.

17.2.4 DxBxxFN Registers

These registers contain the primary Function and Mode bits. The function bits configure the block into one of the available block functions (six for the Comm block, four for the Basic block). The mode bits select the options available for the selected function. These bits should only be changed when the block is disabled.

Three additional control bits are found in this register. The End/Single bit is used to indicate the last or most significant block in a chainable function. This bit must also be set if the chainable function only consists of a single block. The Data Invert bit optimally inverts the selected data input.

The BCEN bits enable the primary output of the block, to drive the row broadcast block. The BCEN bits are set independently in each block and therefore, care must be taken to ensure that only one BCEN bit in a given row is enabled. However, if any of the blocks in a given row have the BCEN bit set, the input that allows the broadcast net from other rows to drive the given row's broadcast net is disabled (see Figure 16-2 on page 195).

Table 17-15. DxBxxFN Function Registers

[2:0]: Function	000b: Timer 001b: Counter 010b: CRCPRS 011b: Reserved 100b: Dead band for PWM 101b: UART 110b: SPI 111b: Reserved
[4:3]: Mode	Function specific
[5]: End/Single	1 == Block is not chained or is at the end of a chain 0 == Block is at the start of or in the middle of a chain
[6]: BCEN	1 == Disable 0 == Enable
[7]: Data Invert	1 == Invert block's data input 0 == Do not invert block's data input

For additional information, reference the DxBxxFN register on page 159.

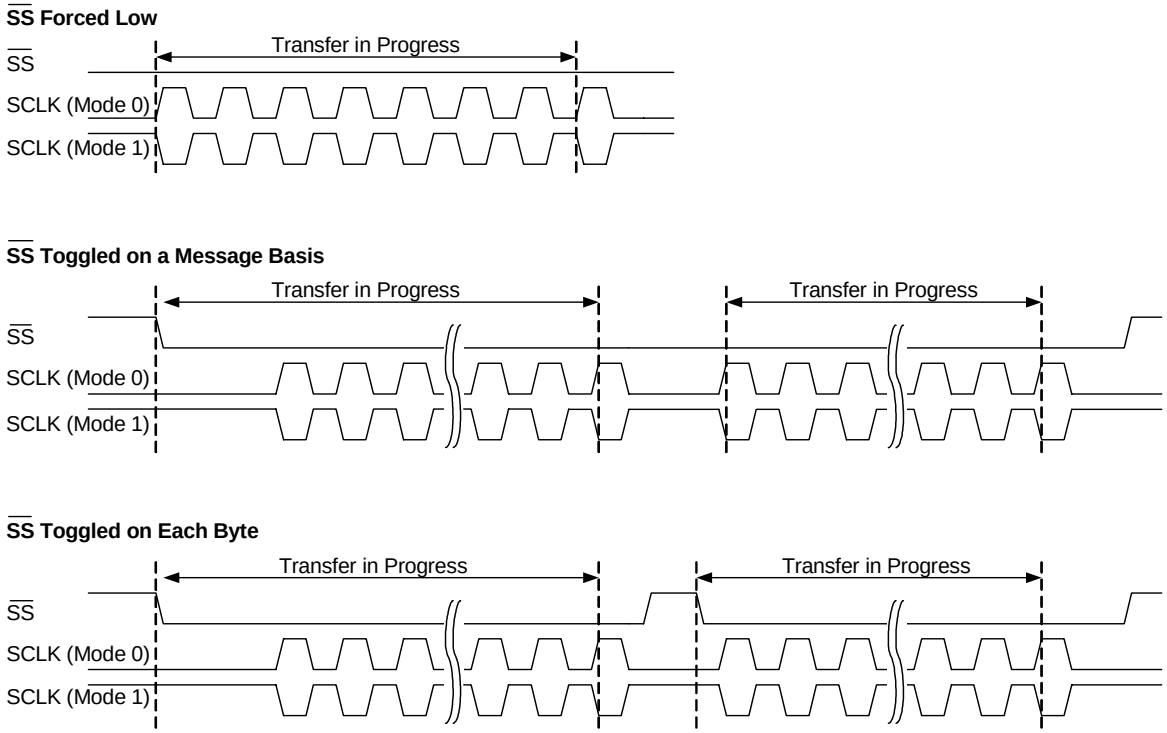

Figure 17-21. Mode 0 and 1 Transfer in Progress

Figure 17-22 illustrates TX data loading in modes 2 and 3. In this case, a transfer in progress is defined to be from the leading edge of the 1st SCLK, to the point at which the RX Buffer register is loaded with the received byte. Loading the shifter by the leading edge of the clock has the effect of providing the required one-half clock setup time, as the data is latched into the receiver on the trailing edge of the SCLK in these modes.

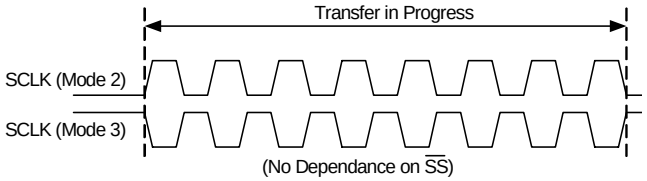

Figure 17-22. Mode 2 and 3 Transfer in Progress

PSoC blocks are user configurable system resources. On-chip analog PSoC blocks reduce the need for many MCU part types and external peripheral components. Analog PSoC blocks are configured to provide a wide variety of peripheral functions. PSoC Designer Software Integrated Development Environment provides automated configuration of PSoC blocks by selecting the desired functions. PSoC Designer then generates the proper configuration information and prints a device data sheet unique to that configuration.

Each of the analog blocks has many potential inputs and several outputs. The inputs to these blocks include analog signals from external sources, intrinsic analog signals driven from neighboring analog blocks, or various voltage reference sources.

There are three analog PSoC block types: Continuous Time (CT) blocks, and Type C and Type D Switch Capacitor (SC) blocks. CT blocks provide continuous time analog functions. SC blocks provide switched capacitor analog functions. Some available supported analog functions are 12-bit Incremental and 11-bit Delta-Sigma ADC, successive approximation ADCs up to 6 bits, DACs up to 8 bits, programmable gain stages, sample and hold circuits, programmable filters, comparators, and a temperature sensor.

The analog blocks are organized into columns. There are two analog columns in the CY8C24xxx, which contain one Continuous Time Block, one Switch Capacitor (SC) Type C, and one Type D Switch Capacitor (SC). The blocks in a particular column all run off the same clocking source. The blocks in a column also share some output bus resources. Refer to the Analog Interface, on page 233 for additional information.

There are three outputs from each analog block. (There are an additional two discrete outputs in the Continuous Time blocks.)

1. The analog output bus (ABUS) is an analog bus resource that is shared by all of the analog blocks in a column. Only one block in a column can actively drive this bus at any one time and the user has control of this output through register settings. This is the only analog output that can be driven directly to a pin.
2. The comparator bus (CBUS) is a digital bus resource that is shared by all of the analog blocks in a column. Only one block in a column can be actively driving this bus at any one time and the user has control of this output through register settings.
3. The local outputs (OUT, plus GOUT, and LOUT in the Continuous Time blocks) are routed to neighbor blocks. The various input multiplexer connections (NMux, PMux, RBotMux, AMux, BMux, and CMux) all use the output bus from one block as their input.

Six analog PSoC blocks are available separately or combined with the digital PSoC blocks. A precision internal voltage reference provides accurate analog comparisons. A temperature sensor input is provided to the analog PSoC block array, supporting applications such as battery chargers and data acquisition, without requiring external components.

The analog functionality provided is as follows.

- A/D and D/A converters, programmable gain blocks, comparators, and switched capacitor filters.
- Single ended configuration is cost effective for reasonable speed and accuracy, and provides a simple interface to most real-world analog inputs and outputs.
- Support is provided for sensor interfaces, audio codes, embedded modems, and general-purpose opamp circuits.
- Flexible, System on-a-Chip programmability, providing variations in functions.
- For a given function, easily selected trade-offs of accuracy and resolution with speed, resources (number of analog blocks), and power dissipated for that application.
- The analog section is an “Analog Computation Unit,” providing programmed steering of signal flow and selecting functionality through register-based control of analog switches. It also sets coefficients in Switched Capacitor Filters and noise shaping (Delta-Sigma) modulators, as well as program gains or attenuation settings in amplifier configurations.
- The architecture provides continuous time blocks and discrete time (Switched Capacitor) blocks. The continuous time blocks allow selection of precision amplifier or comparator circuitry, using programmable resistors as passive configuration and parameter setting elements. The Switched Capacitor (SC) blocks allow configuration of DACs, Delta Sigma, Incremental or Successive Approximation ADCs, or Switched Capacitor filters with programmable coefficients.

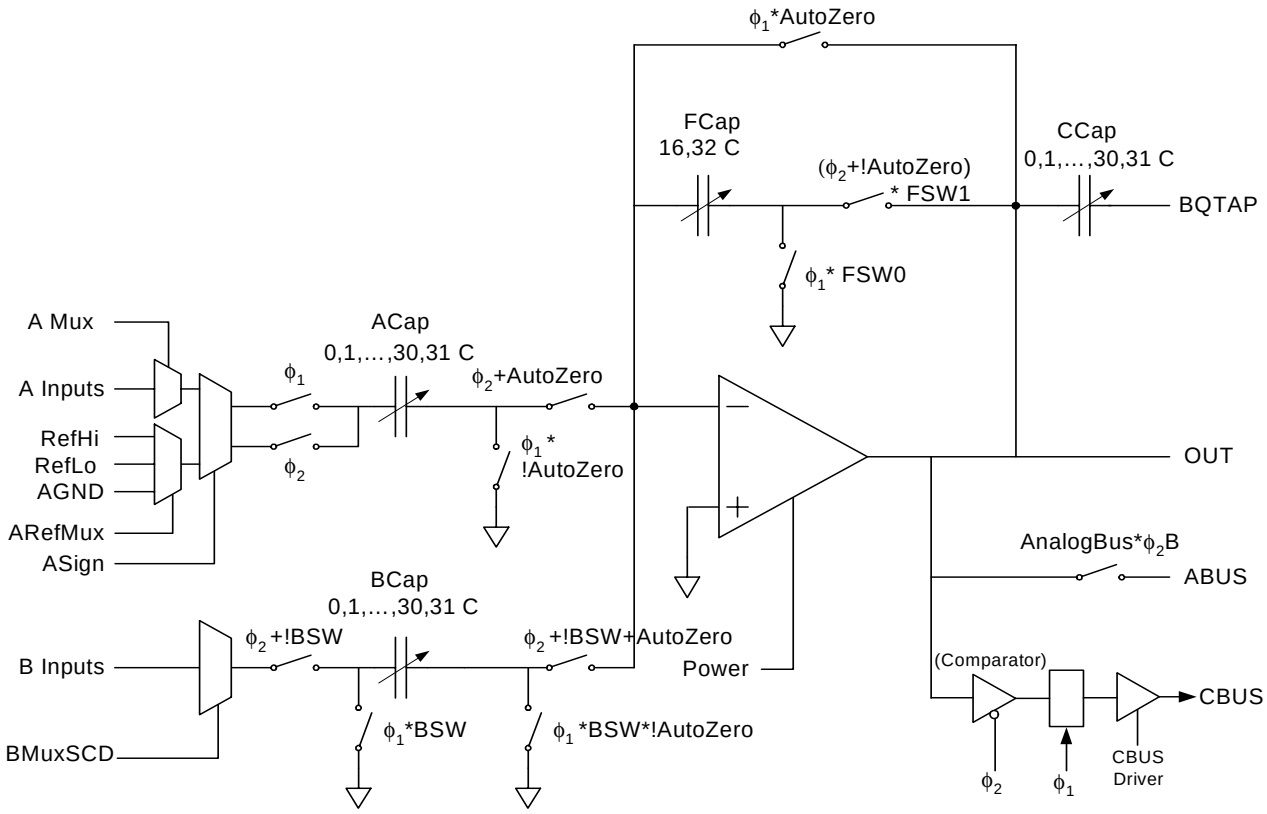

Figure 22-2. Analog Switch Cap Type D PSoC Blocks

22.2 Application Description

The Analog Switched Capacitor blocks support Delta-Sigma, Successive Approximation, and Incremental A/D Conversion, Capacitor DACs, and SC filters. They have three input arrays of binary-weighted switched capacitors, allowing user programmability of the capacitor weights. This provides summing capability of two (CDAC) scaled inputs and a non-switched capacitor input.

The non-switched capacitor node is labeled “BQTAP” in the figure above. The local connection of BQTAP is between horizontal neighboring SC blocks within an analog bi-column in the CY8C24xxx. Since the input of SC Block C has this additional switched capacitor, it is configured for the input stage of such a switched capacitor biquad filter. When followed by an SC Block D Integrator, this combination of blocks can be used to provide a full Switched Capacitor biquad.

22.3 Register Definitions

The *X*Cap field is used to store the binary encoded value for capacitor *X*, where *X* can be A (ACap), B (BCap), or C (CCap), in both the ASCxxCRx and ASDxxCRx registers. Figure 22-3 illustrates the switch settings for the example ACap[4:0]=14h=10100b=20d.

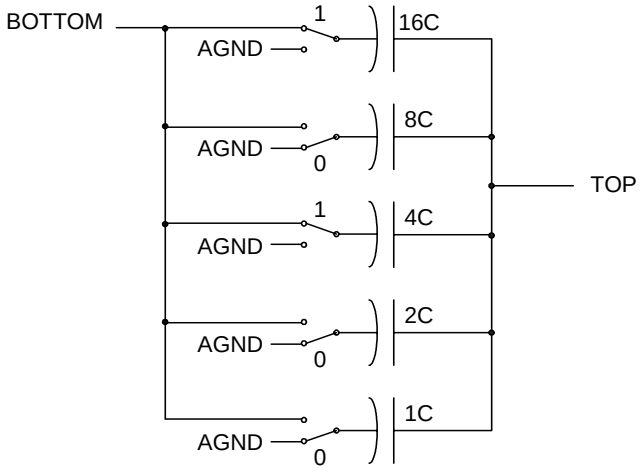

Figure 22-3. Example Switch Capacitor Settings

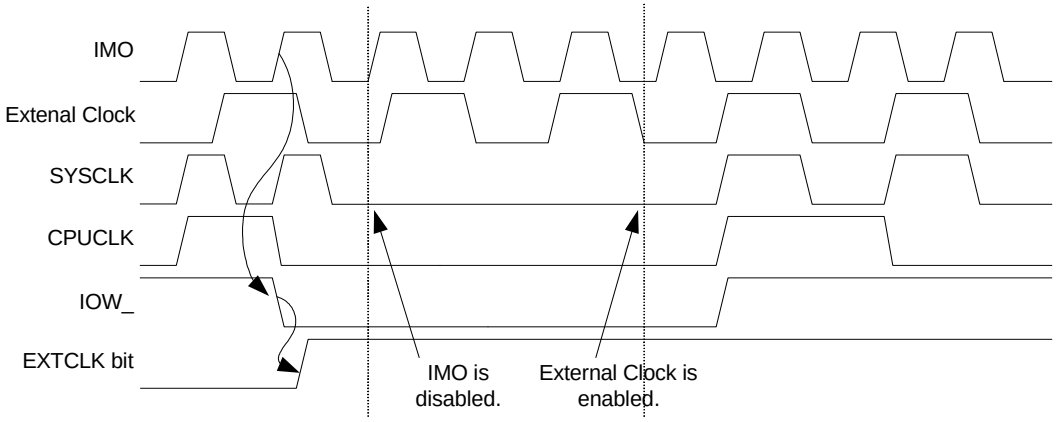

Figure 24-3. Switch from IMO to the External Clock with a CPU Clock Divider of Two or Greater

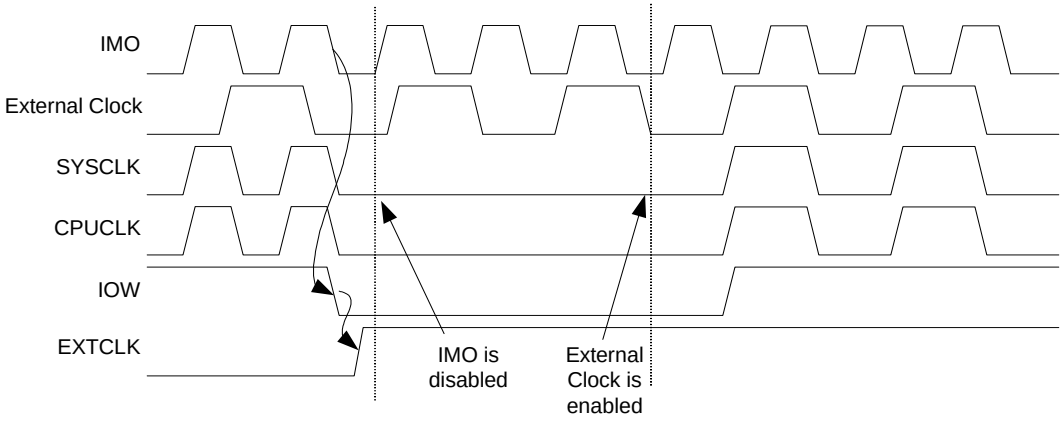

Figure 24-4. Switch from IMO to External Clock with the CPU Running with a CPU Clock Divider of One

The sequence occurs differently between Master transmitter and Master receiver. As a transmitter, the contention will occur on a data bit. On the subsequent Byte Complete interrupt, the Lost Arbitration status will be set. In receiver mode, the contention will occur on the ACK bit. The Master that NACKed the last reception will lose the arbitration. However, the hardware will shift in the next byte in response to the winning Master's ACK, so that a subsequent Byte Complete interrupt occurs. At this point, the losing Master can read the Lost Arbitration status. Contention is checked only at the eight data bit sampling points and one ACK bit sampling point.

Bit 5: Stop Status. Stop status is set on detection of an I2C Stop condition. This bit is sticky, which means that it will remain set until a '0' is written back to it by the firmware. This bit may only be cleared if Byte Complete status is set. If the Stop Interrupt Enable bit is set, an interrupt will also be generated on Stop detection. It is never automatically cleared.

Using this bit, a Slave can distinguish between a previous Stop or Restart on a given address byte interrupt. In Master mode, this bit may be used in conjunction with the Stop IE bit, to generate an interrupt when the bus is free. However, in this case, the bit must have previously been cleared prior to the reception of the Stop, in order to cause an interrupt.

Bit 4: ACK. This control bit defines the acknowledge data bit that will be transmitted out in response to a received byte. When receiving, a Byte Complete interrupt is generated after the eighth data bit is received. On the subsequent write to this register to continue (or terminate) the transfer, the state of this bit will determine the next bit of data that will be transmitted. It is active high. A '1' will send an ACK and a '0' will send a NACK.

A Master Receiver normally terminates a transfer, by writing a '0' (NACK) to this bit. This releases the bus and automatically generates a Stop condition. A Slave Receiver may also send a NACK, to inform the Master that it cannot receive any more bytes.

Bit 3: Address. This bit is set when an address has been received. This consists of a Start or Restart, and an address byte. This bit applies to both master and slave.

In Slave mode, when this status is set, firmware will read the received address from the data register and compare it with its own address. If the address does not match, the firmware will write a NACK indication to this register. No further interrupts will occur, until the next Address is received. If the address does match, firmware must ACK the received byte, then Byte Complete interrupts will be generated on subsequent bytes of the transfer.

This bit will also be set when address transmission is complete in Master mode. If a lost arbitration occurs during the transmission of a Master address, indicated by the Lost Arb bit, the block will revert to Slave mode if enabled. This bit then signifies that the block is being addressed as a slave.

If Slave mode is not enabled, the Byte Complete interrupt will still occur to inform the Master of Lost Arbitration.

Bit 2: Transmit. This bit sets the direction of the shifter for a subsequent byte transfer. The shifter is always shifting in data from the I2C bus, but a write of '1' enables the output of the shifter to drive the SDA output line. Since a write to this register initiates the next transfer, data must be written to the data register prior to writing this bit. In Receive mode, the previously received data must have been read from the data register before this write. In Slave mode, firmware derives this direction from the R/W bit in the received slave address. In Master mode, the firmware decides on the direction and sets it accordingly.

This direction control is only valid for data transfers. The direction of address bytes is determined by the hardware, depending on the Master or Slave mode.

The Master Transmitter terminates a transfer by writing a zero to the transmit bit. This releases the bus and automatically sends a Stop condition, or a Stop/Start or Restart, depending on the I2C_MSCR control bits.

Bit 1: LRB (Last Received Bit). This is the last received bit in response to a previously transmitted byte. In Transmit mode, the hardware will send a byte from the data register and clock in an acknowledge bit from the receiver. On the subsequent byte complete interrupt, firmware will check the value of this bit. A '0' is the ACK value and a '1' is a NACK value. The meaning of the LRB depends on the current operating mode.

Master Transmitter:

'0': ACK, the Slave has accepted the previous byte. The Master may send another byte by first writing the byte to the I2C_DR register and then setting the Transmit bit in the I2C_SCR register. Optionally, the Master may clear the transmit bit in the I2C_SCR register. This will automatically send a Stop. If the Start or Restart bits are set in the I2C_MSCR register, the Stop may be followed by a Start or Restart.

'1': NACK, the Slave cannot accept any more bytes. A Stop is automatically generated by the hardware on the subsequent write to the I2C_SCR register (regardless of the value written). However, a Stop/Start or Restart condition may also be generated, depending on whether firmware has set the Start or Restart bits in the I2C_MSCR register.

Slave Transmitter:

'0': ACK, the Master wants to read another byte. The Slave should load the next byte into the I2C_DR register and set the transmit bit in the I2C_SCR register, to continue the transfer.

'1': NACK, the Master is done reading bytes. The Slave will revert to IDLE state on the subsequent I2C_SCR write (regardless of the value written).

27.4.4 Status Timing

Figure 27-8 illustrates the interrupt timing for Byte Complete, which occurs on the positive edge of the ninth clock (byte + ACK/NACK) in Transmit mode and on the positive edge of the eighth clock in Receive mode. There is a maximum of three cycles of latency due to the input synchronizer/filter circuit. As shown, the interrupt occurs on the clock following a valid SCL positive edge input transition (after the synchronizers). The Address bit is set with the same timing, but only after a Slave address has been received. The LRB (Last Received Bit) status is also set with the same timing, but only on the ninth bit after a transmitted byte.

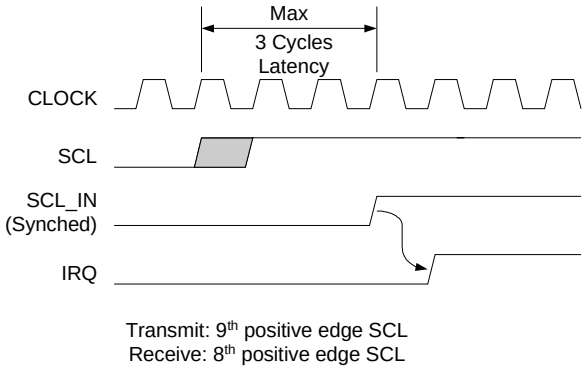

Figure 27-8. Byte Complete, Address, LRB Timing

Figure 27-9 shows the timing for Stop status. This bit is set (and the interrupt occurs) two clocks after the synchronized and filtered SDA line transitions to a '1', when the SCL line is high.

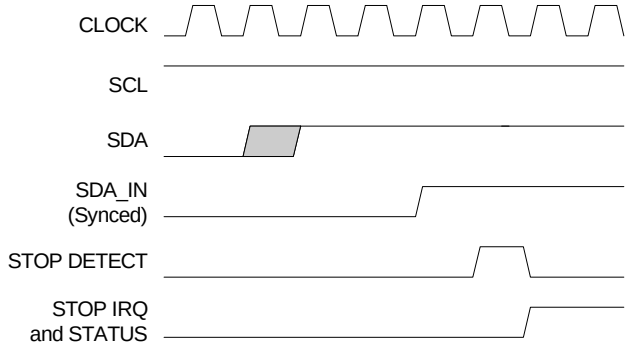

Figure 27-9. Stop Status and Interrupt Timing

Figure 27-10 illustrates the timing for bus error interrupts. Bus Error Status (and interrupt) occurs one cycle after the internal Start or Stop detect (two cycles after the filtered and synced SDA input transition).

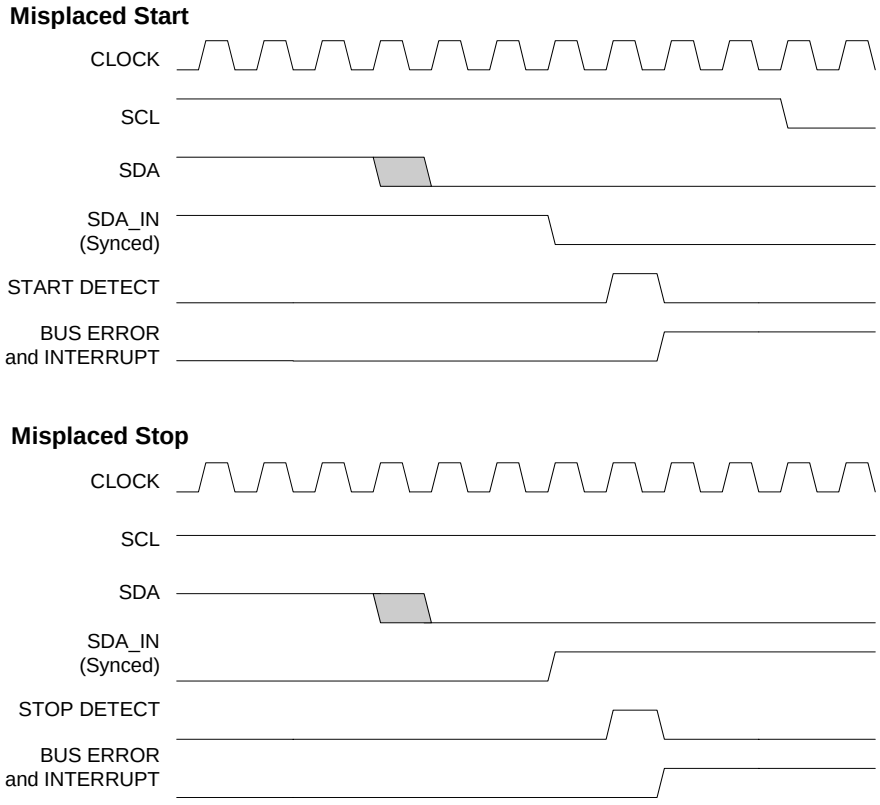

Figure 27-10. Bus Error Interrupt Timing

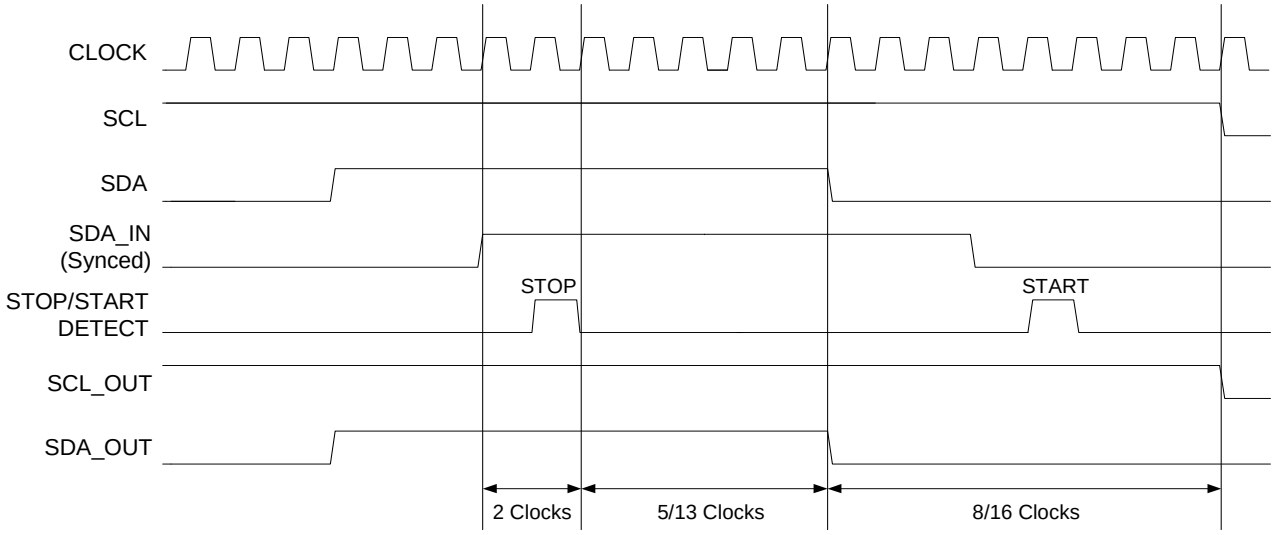

Figure 27-13. Master Stop/Start Chaining

27.4.6 Master Restart Timing

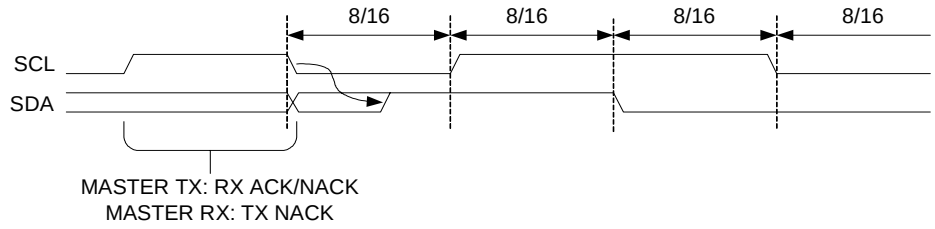

Figure 27-14. Master Restart Timing

27.4.7 Master Stop Timing

Figure 27-15 shows basic Master Stop timing. In order to generate a Stop, the SDA line is first pulled low, in accordance with the basic SDA output timing. Then, after the full low of SCL is completed and the SCL line is pulled high, the SDA line remains low for a full one-half bit time before it is pulled high to signal the Stop.

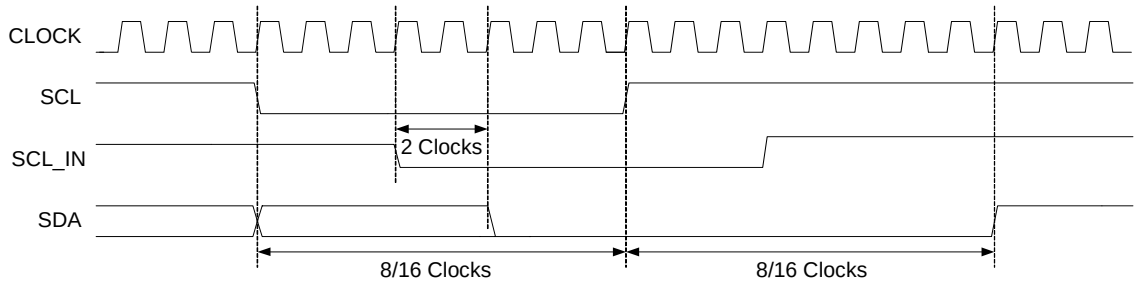

Figure 27-15. Master Stop Timing

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{IPOR}	AVDD Value for IPOR Trip	1.60	1.90	2.30	V	
	AVDD Value for PPOR Trip (positive ramp)					
V_{PPOR0R}	PORLEV1,PORLEV0=00b		2.908		V	
V_{PPOR1R}	PORLEV1,PORLEV0=01b	–	4.394	–	V	
V_{PPOR2R}	PORLEV1,PORLEV0=10b		4.548		V	
	AVDD Value for PPOR Trip (negative ramp)					
V_{PPOR0}	PORLEV1,PORLEV0=00b		2.816		V	
V_{PPOR1}	PORLEV1,PORLEV0=01b	–	4.394	–	V	
V_{PPOR2}	PORLEV1,PORLEV0=10b		4.548		V	
	PPOR Hysteresis					
V_{PH0}	PORLEV1,PORLEV0=00b	–	92	–	mV	
V_{PH1}	PORLEV1,PORLEV0=01b	–	0	–	mV	
V_{PH2}	PORLEV1,PORLEV0=10b	–	0	–	mV	
	AVDD Value for LVD Trip					
V_{LVD0}	VM2,VM1,VM0=000b	2.863	2.921	2.979[a]	V	
V_{LVD1}	VM2,VM1,VM0=001b	2.963	3.023	3.083	V	
V_{LVD2}	VM2,VM1,VM0=010b	3.070	3.133	3.196	V	
V_{LVD3}	VM2,VM1,VM0=011b	3.920	4.00	4.080	V	
V_{LVD4}	VM2,VM1,VM0=100b	4.393	4.483	4.573	V	
V_{LVD5}	VM2,VM1,VM0=101b	4.550	4.643	4.736[b]	V	
V_{LVD6}	VM2,VM1,VM0=110b	4.632	4.727	4.822	V	
V_{LVD7}	VM2,VM1,VM0=111b	4.718	4.814	4.910	V	
	AVDD Value for PUMP Trip					
V_{PUMP0}	VM2,VM1,VM0=000b	2.963	3.023	3.083	V	
V_{PUMP1}	VM2,VM1,VM0=001b	3.033	3.095	3.157	V	
V_{PUMP2}	VM2,VM1,VM0=010b	3.185	3.250	3.315	V	
V_{PUMP3}	VM2,VM1,VM0=011b	4.110	4.194	4.278	V	
V_{PUMP4}	VM2,VM1,VM0=100b	4.550	4.643	4.736	V	
V_{PUMP5}	VM2,VM1,VM0=101b	4.632	4.727	4.822	V	
V_{PUMP6}	VM2,VM1,VM0=110b	4.719	4.815	4.911	V	
V_{PUMP7}	VM2,VM1,VM0=111b	4.900	5.000	5.100	V	

a. Always greater than 50 mV above PPOR (PORLEV=00) for falling supply.
b. Always greater than 50 mV above PPOR (PORLEV=10) for falling supply.