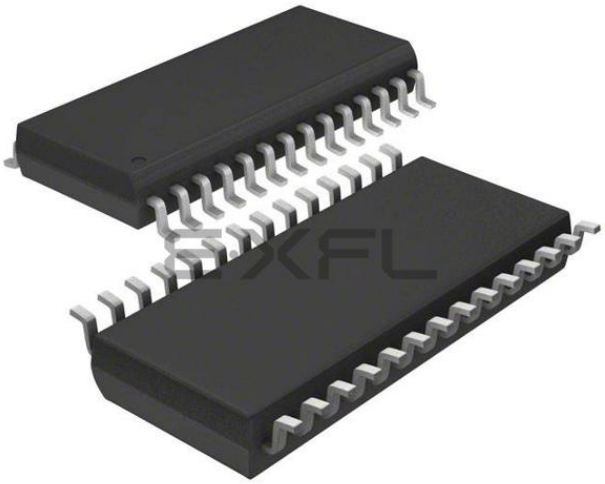

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Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 2x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24423-24pvi

3.4.3 Three-Byte Instructions

The three-byte instruction formats are the second most prevalent instruction formats. These instructions need three bytes because they either move data between two addresses in the user-accessible address space (registers and RAM) or they hold 16-bit absolute addresses as the destination of a long jump or long call.

Table 3-5. Three-Byte Instruction Formats

Byte 0	Byte 1	Byte 2
8-bit opcode	16-bit address (MSB, LSB)	
8-bit opcode	8-bit address	8-bit data
8-bit opcode	8-bit address	8-bit address

The first instruction format shown in Table 3-5 is used by the `LJMP` and `LCALL` instructions. These instructions change program execution unconditionally to an absolute address. The instructions use an 8-bit opcode leaving room for a 16-bit destination address.

The second three-byte instruction format shown in Table 3-5 is used by the following two addressing modes:

- Destination Direct Source Immediate (`ADD [7], 5`).
- Destination Indexed Source Immediate (`ADD [X+7], 5`).

The third three-byte instruction format is for the Destination Direct Source Direct addressing mode which is used by only one instruction. This instruction format uses an 8-bit opcode followed by two 8-bit addresses. The first address is the destination address in RAM while the second address is source address in RAM. The following is an example of this instruction: `MOV [7], [5]`.

3.5 Addressing Modes

The M8C has ten addressing modes:

- Source Immediate
- Source Direct
- Source Indexed
- Destination Direct
- Destination Indexed
- Destination Direct Source Immediate
- Destination Indexed Source Immediate
- Destination Direct Source Direct
- Source Indirect Post Increment
- Destination Indirect Post Increment

3.5.1 Source Immediate

For these instructions the source value is stored in operand 1 of the instruction. The result of these instructions is placed in either the M8C A, F, or X register as indicated by the instruction's opcode. All instructions using the Source Immediate addressing mode are two bytes in length.

Table 3-6. Source Immediate

Opcode	Operand 1
Instruction	Immediate Value

Source Immediate Examples:

Source Code	Machine Code	Comments
`ADD A, 7`	`01 07`	The immediate value 7 is added to the Accumulator. The result is placed in the Accumulator.
`MOV X, 8`	`57 08`	The immediate value 8 is moved into the X register.
`AND F, 9`	`70 09`	The immediate value of 9 is logically AND'ed with the F register and the result is placed in the F register.

The interrupt logic portion of the block is shown in Figure 6-2.

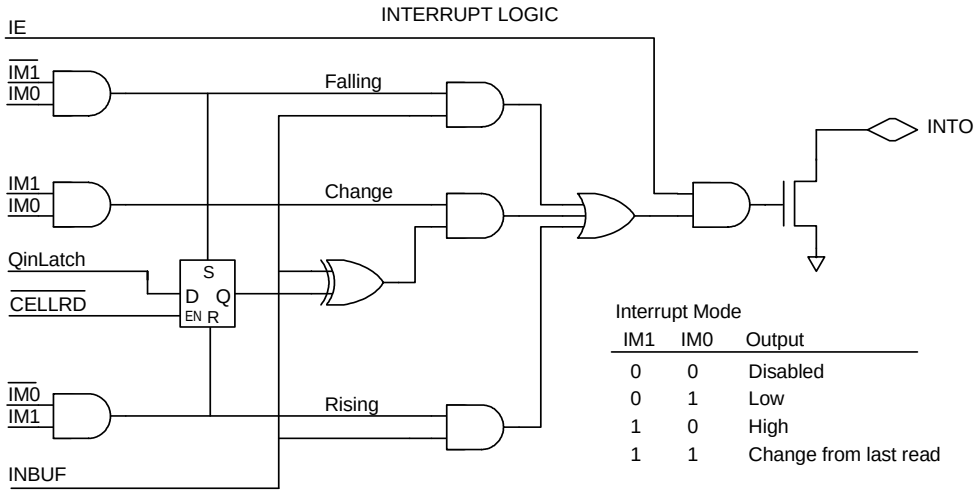

Figure 6-2. GPIO Interrupt Mode Block Diagram

6.2 Register Definitions

For a selected GPIO block, the individual registers are addressed as shown in Table 6-2. In the register names, the 'x' is the port number, configured at the chip level (x = 0 to 7 typically). DA[1:0] refers to the two LSB of the register address.

All register values are readable, except for the PRTxDR register; reads of this register return the pin state instead of the register bit state.

Table 6-2. Internal Register Bit Addressing

XOI	DA[1:0]	Register	Resets to:	(Name)	Function
0	00b	PRTxDR	0	DIN	Data
0	01b	PRTxIE	0	IE	Interrupt Enable
0	10b	PRTxGS	0	BYP	Global Select
0	11b	PRTxDM2	**1**	DM2	Drive Mode, Bit 2
1	00b	PRTxDM0	0	DM0	Drive Mode, Bit 0
1	01b	PRTxDM1	1	DM1	Drive Mode, BIt 1
1	10b	PRTxIC0	0	IM0	Intrpt. Mask, Bit 0
1	11b	PRTxIC1	0	IM1	Intrpt. Mask, Bit 1

6.2.1 PRTxDR Registers

Writing the PRTxDR register bit sets the output drive state for the pin to high (for DIN=1) or low (DIN=0), unless a bypass mode is selected (either I2C Enable=1 or the global select register written high).

Reading PRTxDR returns the actual pin state, as seen by the input buffer. This may not be the same as the expected output state, if the load pulls the pin more strongly than the pin's configured output drive.

For additional information, reference the PRTxDR register on page 88.

group. These are referred to as DM2, DM1, and DM0, or

6.2.2 PRTxIE Registers

The PRTxIE register is used to enable/disable the interrupt enable internal to the GPIO block. A '1' enables the INTO output at the block, a '0' disables INTO so it can only be Hi-Z.

For additional information, reference the PRTxIE register on page 89.

6.2.3 PRTxGS Registers

The PRTxGS register is used to select the block for connection to global inputs or outputs. Writing this register high enables the global bypass (BYP=1 in Figure 6-1). If the drive mode is set to digital Hi-Z (DM[2:0] = 010b), then the pin is selected for global input (PIN drives to the Global Input Bus). In non-Hi-Z modes, the block is selected for global output (the Global Output Bus drives to PIN), bypassing the data register value (assuming I2C Enable=0).

If the PRTxGS register is written to zero, the global in/out function is disabled for the pin.

For additional information, reference the PRTxGS register on page 90.

6.2.4 PRTxDMx Registers

There are eight possible drive modes for each port pin. Three mode bits are required to select one of these modes, and these three bits are spread into three different registers (PRTxDM0, PRTxDM1, and PRTxDM2). The bit position of the effected port pin (Example: Pin[2] in Port 0) is the same as the bit position of each of the three Drive Mode register bits that control the drive mode for that pin (Example: Bit[2] in PRT0DM0, bit[2] in PRT0DM1 and bit[2] in PRT0DM2). The three bits from the three registers are treated as a

10. 32 kHz Crystal Oscillator (ECO)

This chapter briefly explains the 32 kHz Crystal Oscillator (ECO) and its associated register. The 32 kHz crystal oscillator circuit allows the user to replace the internal low speed oscillator with a more precise time source at low cost and low power.

Table 10-1. Crystal Oscillator Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
1,E0h	OSC_CR0	32k Select	PLL Mode	No Buzz	Sleep[1:0]		CPU Speed[2:0]			RW : 00
1,EBh	ECO_TR	PSSDC[1:0]								W : 00
x,FEh	CPU_SCR1								IRAMDIS	RW:00

10.1 Architectural Description

The crystal oscillator circuit uses an inexpensive watch crystal and two small valued load capacitors as external components. All other components are on the PSoC chip. The crystal oscillator may be configured to provide a reference to the internal main oscillator in PLL mode for generating a more accurate 24 MHz system clock.

The XTALIn and XTALOut pins support connection of a 32.768 kHz watch crystal. To run from the external crystal, Bit 7 of the Oscillator Control 0 Register (OSC_CR0) must be set (default is off). The only external components are the crystal and the two load capacitors that connect to Vdd. Transitions between the internal and external oscillator domains may produce glitches on the clock bus.

During the process of activating the ECO, there must be a hold-off period before using it as the 32 kHz source. This hold off period is partially implemented in hardware using the Sleep Timer. Firmware must set up a sleep period of one second (maximum ECO settling time), and then enable the ECO in the OSC_CR0 register. At the one second time-out (the Sleep Interrupt), the switch is made by hardware to the ECO. If the ECO is subsequently deactivated, the ILO will again be activated and the switch is made back to the ILO immediately.

The firmware steps involved in switching between the internal low speed oscillator to the 32 kHz Crystal Oscillator are as follows.

1. At reset, the chip begins operation, using the internal low speed oscillator.
2. Select sleep interval of 1 second using bits[4:3] in the Oscillator Control 0 Register (OSC_CR0), as the oscillator stabilization interval.
3. Enable the 32 kHz Crystal Oscillator, by setting bit [7] in Oscillator Control 0 Register (OSC_CR0) to 1.
4. The 32 kHz Crystal Oscillator becomes the selected source, at the end of the one-second interval on the edge created by the Sleep Interrupt logic. The one-second interval gives the oscillator time to stabilize, before it becomes the active source. The Sleep Interrupt need not be enabled for the switch-over to occur. Reset the sleep timer (if this does not interfere with any ongoing real-time clock operation), to guarantee the interval length. Note that the internal low speed oscillator continues to run, until the oscillator is automatically switched over by the sleep timer interrupt.
5. It is strongly advised to wait the one-second stabilization period prior to engaging the PLL mode to lock the Internal Main Oscillator frequency to the 32 kHz Crystal Oscillator frequency.

Note 1 The internal low speed oscillator switches back instantaneously by writing the 32K Select control bit to zero.

Note 2 If the proper settings are selected in PSoC Designer, the above steps are automatically done in *boot.asm*.

Note 3 Transitions between oscillator domains may produce glitches on the 32K clock bus. Functions that require accuracy on the 32K clock should be enabled after the transition in oscillator domains.

Table 11-2. Sleep Interval Selections

Sleep Interval OSC_CR[4:3]	Sleep Timer Clocks	Sleep Period (nominal)	Watchdog Period (nominal)
00b (default)	64	1.95 ms	6 ms
01b	512	15.6 ms	47 ms
10b	4096	125 ms	375 ms
11b	32,768	1 sec	3 sec

Bits 2, 1, and 0: CPU Speed[2:0]. The PSoC M8C may operate over a range of CPU clock speeds (Table 11-3), allowing the M8C's performance and power requirements to be tailored to the application.

The reset value for the CPU Speed bits is zero. Therefore, the default CPU speed is one-eighth of the clock source. The internal main oscillator is the default clock source for the CPU speed circuit; therefore, the default CPU speed is 3 MHz.

The CPU frequency is changed with a write to the OSC_CR0 register. There are eight frequencies generated from a power-of-2 divide circuit, which are selected by a 3-bit code. At any given time, the CPU 8:1 clock multiplexer is selecting one of the available frequencies, which is re-synchronized to the 24 MHz master clock at the output.

Regardless of the CPU speed bit's setting, if the actual CPU speed is greater than 12 MHz, the 24 MHz operating requirements apply. An example of this scenario is a device that is configured to use an external clock, which is supplying a frequency of 20 MHz. If the CPU speed register's value is 0b011, the CPU clock will be 20 MHz. Therefore, the supply voltage requirements for the device are the same as if the part was operating at 24 MHz off of the internal main oscillator. The operating voltage requirements are not relaxed until the CPU speed is at 12.0 MHz or less.

Table 11-3. OSC_CR0[2:0] Bits: CPU Speed

Bits	Internal Main Oscillator	External Clock
000b	3 MHz	EXTCLK/ 8
001b	6 MHz	EXTCLK/ 4
010b	12 MHz	EXTCLK/ 2
011b	24 MHz	EXTCLK/ 1
100b	1.5 MHz	EXTCLK/ 16
101b	750 kHz	EXTCLK/ 32
110b	187.5 kHz	EXTCLK/ 128
111b	93.7 kHz	EXTCLK/ 256

For additional information, reference the OSC_CR0 register on page 176.

11.2.2 OSC_CR2 Register

Bit 7: PLLGAIN. This is the only bit in the OSC_CR2 register that directly influences the PLL. When set, this bit keeps the PLL in a low gain mode.

Bits 6 to 3: Reserved.

Bit 2: EXTCLKEN. When the EXTCLKEN bit is set, the external clock becomes the source for the internal clock tree, SYSCLK, which drives most chip clocking functions. All external and internal signals, including the 32 kHz clock, whether derived from the internal low speed oscillator (ILO) or the crystal oscillator, are synchronized to this clock source. If an external clock is enabled, PLL mode should be off.

Bit 1: IMODIS. When set, the Internal Main Oscillator is disabled. If the doubler is enabled (SYSCLKX2DIS=0), the Internal Main oscillator will be forced on.

Bit 0: SYSCLKX2DIS. When set, the Internal Main Oscillator's doubler is disabled. This will result in a reduction of overall device power, on the order of 1 mA. It is advised that any application that does not require this doubled clock should have it turned off.

For additional information, reference the OSC_CR2 register on page 178.

13.1.31 ASDxxCR2

Analog Switch Cap Type D Block Control Register 2

Individual Register Names and Addresses

ASD11CR2 : x,86h ASD20CR2 : x,92h

	7	6	5	4	3	2	1	0
Access : POR	RW : 0	RW : 0	RW : 0	RW : 00				
Bit Name	AnalogBus	CompBus	AutoZero	CCap[4:0]				

For additional information, reference the “Register Definitions” on page 251 in the Switched Capacitor Block chapter.

Bit	Name	Description
[7]	**AnalogBus**	Enable output to the analog bus. 0 Disable output to analog column bus. 1 Enable output to analog column bus.
[6]	**CompBus**	Enable output to the comparator bus. 0 Disable output to comparator bus. 1 Enable output to comparator bus.
[5]	**AutoZero**	Bit for controlling gated switches. 0 Shorting switch is not active. Input cap branches shorted to opamp input. 1 Shorting switch is enabled during internal PHI1. Input cap branches shorted to analog ground during internal PHI1 and to opamp input during internal PHI2.
[4:0]	**CCap[4:0]**	Binary encoding for 32 possible capacitor sizes for capacitor CCap.

13.1.51 RES_WDT

Reset Watchdog Timer Register

Individual Register Names and Addresses

RES_WDT: 0,E3h

	7	6	5	4	3	2	1	0
Access : POR	W : 00							
Bit Name	WDSL_Clear[7:0]							

For additional information, reference the “Register Definitions” on page 77 in the Sleep and Watchdog chapter.

Bit	Name	Description
[7:0]	**WDSL_Clear[7:0]**	Any write clears the Watchdog timer. A write of 38h clears both the Watchdog and Sleep timers.

13.2 Bank 1 Registers

The following registers are all in bank 1 and are listed in offset order.

13.2.1 PRTxDM0

Port Drive Mode Bit Register 0

Individual Register Names and Addresses

PRT0DM0 : 1,00h PRT1DM0 : 1,04h PRT2DM0 : 1,08h

	7	6	5	4	3	2	1	0
Access : POR	RW : 00							
Bit Name	Drive Mode 0[7:0]							

In register PRTxDM0 there are eight possible drive modes for each port pin. Three mode bits are required to select one of these modes, and these three bits are spread into three different registers (PRTxDM0, "PRTxDM1" on page 156, and "PRTxDM2" on page 91). The bit position of the effected port pin (Example: Pin[2] in Port 0) is the same as the bit position of each of the three Drive Mode register bits that control the drive mode for that pin (Example: Bit[2] in PRT0DM0, bit[2] in PRT0DM1 and bit[2] in PRT0DM2). The three bits from the three registers are treated as a group. These are referred to as DM2, DM1, and DM0, or together as DM[2:0].

All drive mode bits are shown in the sub-table below ([21**0**] refers to the combination (in order) of bits in a given bit position); however, this register only controls the least significant bit of the drive mode. For additional information, reference the "Register Definitions" on page 60 in the GPIO chapter.

Bit	Name	Description			
[7:0]	**Drive Mode 0[7:0]**	Bit 0 of the drive mode, for each of 8-port pins, for a GPIO port.			
		[210**]**	**Pin Output High**	**Pin Output Low**	**Notes**
		00**0**b	Strong	Resistive	
		00**1**b	Strong	Strong	
		01**0**b	Hi-z	Hi-z	Digital input enabled.
		01**1**b	Resistive	Strong	
		10**0**b	Slow + strong	Hi-z	
		10**1**b	Slow + strong	Slow + strong	
		11**0**b	Hi-z	Hi-z	Digital input disabled for zero power. Reset state.
		11**1**b	Hi-z	Slow + strong	I^2C Compatible mode.
		Note A bold digit, in the table above, signifies that the digit is used in this register.			

13.2.7 DxBxxOU

Digital Basic/Communications Type B Block Output Register

Individual Register Names and Addresses

DBB00OU : 1,22h DBB01OU : 1,26h DCB02OU : 1,2Ah DCB03OU : 1,2Eh

	7	6	5	4	3	2	1	0
Access : POR	RW : 0		RW : 0	RW : 0		RW : 0	RW : 0	
Bit Name	AUXCLK		AUXEN	AUX IO Select[1:0]t		OUTEN	Output Select[1:0]	

Before changing any of the configuration registers (DxBxxFN, DxBxxIN, and DxBxxOU), disable the corresponding digital block by setting bit 0 in the CR0 or DxBxxCR0 register to '0'. The values in this register should not be changed while the block is enabled. After all configuration changes are made, enable the block by setting bit 0 in the DxBxxCR0 register to '1'.

For additional information, reference the "Register Definitions" on page 208 in the Digital Blocks chapter.

Bit	Name	Description		
[7:6]	**AUXCLK**	00b	No sync	16 to 1 clock mux output
		01b	Synchronize to SYSCLK	Output of 16 to 1 clock mux to SYSCLK
		10b	Synchronize to SYSCLKX2	Output of 16 to 1 clock mux to SYSCLKX2
		11b	SYSCLK	Directly connect SYSCLK to block clock input
[5]	**AUXEN**	Aux IO Enable (function dependent) All Functions except SPI Slave: Enable Auxiliary Output Driver 0 Disabled 1 Enabled SPI Slave: Slave Select Input		
		Aux IO Enable, Aux IO Select[1:0] (function dependent, SPIS only) Source for SS_ input 000b AUXDATA[0] (Row Input 0) 001b AUXDATA[1] (Row Input 1) 010b AUXDATA[2] (Row input 2) 011b AUXDATA[3] (Row input 3) 100b Force SS_ active 101b Reserved 110b Reserved 111b Reserved		
[4:3]	**AUX IO Select[1:0]**	All Functions except SPI Slave: Row Output Select for Auxiliary Function Output (function dependent) 00b Row Output 0 01b Row Output 1 10b Row Output 2 11b Row Output 3		
[2]	**OUTEN**	Enable Primary Function Output Driver 0 Disabled. 1 Enabled.		

(continued on next page)

13.2.10 ABF_CR0

Analog Output Buffer Control Register 0

Individual Register Names and Addresses

ABF_CR0: 1,62h

	7	6	5	4	3	2	1	0
Access : POR	RW : 0		RW : 0		RW : 0		RW : 0	RW : 0
Bit Name	ACol1Mux		ABUF1EN0		ABUF0EN0		Bypass	PWR

For additional information, reference the "Register Definitions" on page 63 in the Analog Output Drivers chapter or the "Register Definitions" on page 245 in the Analog Input Configuration chapter.

Bit	Name	Description
[7]	**ACol1Mux**	0 Set column 1 input to column 1 input mux output. 1 Set column 1 input to column 0 input mux output.
[6]	**Reserved**	
[5]	**ABUF1EN0**	Enables the analog output buffer for Analog Column 1 (Pin P0[5]). 0 Disable analog output buffer. 1 Enable analog output buffer.
[4]	**Reserved**	
[3]	**ABUF0EN0**	Enables the analog output buffer for Analog Column 0 (Pin P0[3]). 0 Disable analog output buffer. 1 Enable analog output buffer.
[2]	**Reserved**	
[1]	**Bypass**	Connects the positive input of both amplifiers directly to their output. Amplifiers need to be disabled when in Bypass mode. 0 Disable 1 Enable
[0]	**PWR**	Determines power level of all output buffers. 0 Low output power 1 High output power

13.2.13 ALT_CR0

Analog LUT Control Register 0

Individual Register Names and Addresses

ALT_CR0: 1,67h

	7	6	5	4	3	2	1	0
Access : POR	RW : 0				RW : 0			
Bit Name	LUT1[3:0]				LUT0[3:0]			

For additional information, reference the “Register Definitions” on page 238 in the Analog Interface chapter.

Bit	Name	Description
[7:4]	**LUT1[3:0]**	Select one of 16 logic functions for the output of comparator bus 1. 0h FALSE 1h A AND B 2h A AND $\overline{B}$ 3h A 4h $\overline{A}$ AND B 5h B 6h A XOR B 7h A OR B 8h A NOR B 9h A XNOR B Ah $\overline{B}$ Bh A OR $\overline{B}$ Ch $\overline{A}$ Dh $\overline{A}$ OR B Eh A NAND B Fh TRUE
[3:0]	**LUT0[3:0]**	Select one of 16 logic functions for the output of comparator bus 0. 0h FALSE 1h A AND B 2h A AND $\overline{B}$ 3h A 4h $\overline{A}$ AND B 5h B 6h A XOR B 7h A OR B 8h A NOR B 9h A XNOR B Ah $\overline{B}$ Bh A OR $\overline{B}$ Ch $\overline{A}$ Dh $\overline{A}$ OR B Eh A NAND B Fh TRUE

13.2.20 OSC_CR0

Oscillator Control Register 0

Individual Register Names and Addresses

OSC_CR0: 1,E0h

	7	6	5	4	3	2	1	0
Access : POR	RW : 0	RW : 0	RW : 0	RW : 0		RW : 0		
Bit Name	32k Select	PLL Mode	No Buzz	Sleep[1:0]		CPU Speed[2:0]		

For additional information, reference the “Register Definitions” on page 266 in the Digital Clocks chapter.

Bit	Name	Description		
[7]	**32k Select**	0	Internal low precision 32 kHz oscillator	
		1	External Crystal Oscillator	
[6]	**PLL Mode**	0	Disabled	
		1	Enabled. Internal main oscillator is frequency locked to External Crystal Oscillator.	
[5]	**No Buzz**	0	BUZZ bandgap during power down.	
		1	Bandgap is always powered even during sleep.	
[4:3]	**Sleep[1:0]**		**Sleep Interval**	
		00b	1.95 ms (512 Hz)	
		01b	15.6 ms (64 Hz)	
		10b	125 ms (8 Hz)	
		11b	1 s (1 Hz)	
[2:0]	**CPU Speed[2:0]**		**Internal Main Oscillator**	**External Clock**
		000b	3 MHz	EXTCLK / 8
		001b	6 MHz	EXTCLK / 4
		010b	12 MHz	EXTCLK / 2
		011b	24 MHz	EXTCLK / 1
		100b	1.5 MHz	EXTCLK / 16
		101b	750 kHz	EXTCLK / 32
		110b	187.5 kHz	EXTCLK / 128
		111b	93.7 kHz	EXTCLK / 256

In Figure 15-1, the detailed view of a Digital PSoC block row has been replaced by a box labeled “Digital PSoC Block Row.” The rest of this figure illustrates how all rows are connected to the same globals, clocks, and so on. The figure also illustrates how the broadcast clock nets (BCxxxx) are connected between rows.

17.2.1.3 Dead Band Register Definitions

Bank 0: There are three 8-bit data registers and a 3-bit control register. Table 17-8 explains the meaning of these registers in the context of Dead Band operation.

Bank 1: The Mode bits in the Function register are block type specific. Other bit fields in this register, as well as the definitions of the Input and Output registers, are common to all functions.

Mode [1:0] is encoded as the Kill Type. In all cases, the output is forced low immediately. Mode bits are encoded for Kill options and are detailed in the following table.

Reference "Dead Band Timing" on page 216 for additional information on the Dead Band Kill options.

Table 17-8. Dead Band Register Descriptions

Name	Function	Description
DR0	Count Value	Not Directly Readable or Writeable. During normal operation, DR0 stores the current count of a synchronous down counter. When disabled, a write to the DR1 Period register is also simultaneously loaded into DR0 from the data bus. When disabled, a read of DR0 returns 00h to the data bus and transfers the contents of DR0 to DR2.
DR1	Period	Write Only Register. Data in this register sets the period of the dead band count. The actual number of clocks counted is Period + 1. The minimum period value is 00h, which sets a dead band time of one clock. When disabled, a write to this register also transfers the period value directly into DR0. When enabled, if the block frequency is 24 MHz or below, this register may be written to at any time, but the period will only be reloaded into DR0 in the clock following a terminal count. If the block frequency is 48 MHz, the terminal count or compare interrupt should be used to synchronize the new Period register write; otherwise, the counter could be incorrectly loaded.
DR2	Buffer	When disabled, a read of DR0 will transfer the contents of DR0 into DR2.

17.2.1.4 CRCPRS Register Definitions

Bank 0: There are three data registers and one control register. Table 17-9 explains the meaning of these registers in the context of CRCPRS operation. Note that in the CRCPRS function, a write to the DR2 Seed register is also loaded simultaneously into DR0.

Bank 1: The mode bits in the Function register are block type specific. Other bit fields in this register, as well as the definitions of the Input and Output registers, are common to all functions and are described in the "DxBxxIN Registers" on page 214 and the "DxBxxOU Registers" on page 214.

The mode bits are encoded to determine the Compare type.

Table 17-9. CRCPRS Register Descriptions

Name	Function	Description
DR0	LFSR	Not Directly Readable or Writeable. During normal operation, DR0 stores the state of a synchronous Linear Feedback Shift Register. When disabled, a write to the DR2 Seed register is also simultaneously loaded into DR0 from the data bus. When disabled, a read of DR0 returns 00h to the data bus and transfers the contents of DR0 to DR2. This register should not be read while the block is enabled.
DR1	Polynomial	Write Only Register. Data in this register sets the polynomial for the CRC or PRS function. **Exception**: This register must only be written when the block is disabled.
DR2	Seed/Residue	Read Write Register. DR2 functions as a Seed and Residue register. When disabled, a write to this register also transfers the seed value directly into DR0. When enabled, DR2 may be written to at any time. Value written will be used in the Compare function. When enabled, the compare output is computed using the Compare Type (set in the Function register mode bits) between DR0 and DR2. The result of the compare is output to the auxiliary output. When disabled, a read of DR0 will transfer the contents of DR0 into DR2. This feature can be used to read out the residue, after a CRC operation is complete.

The figures that follow illustrate the analog mux connections for the PSoC device.

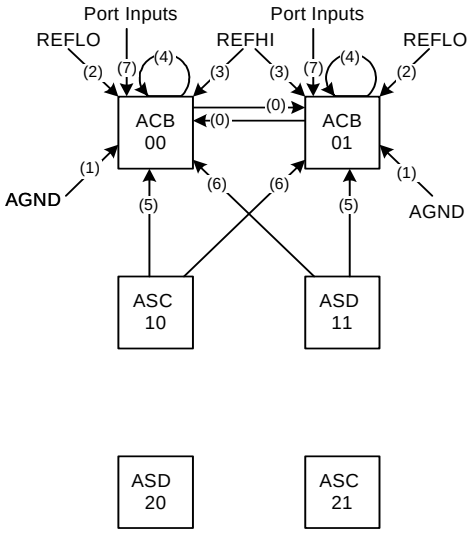

Figure 19-2. NMux Connections

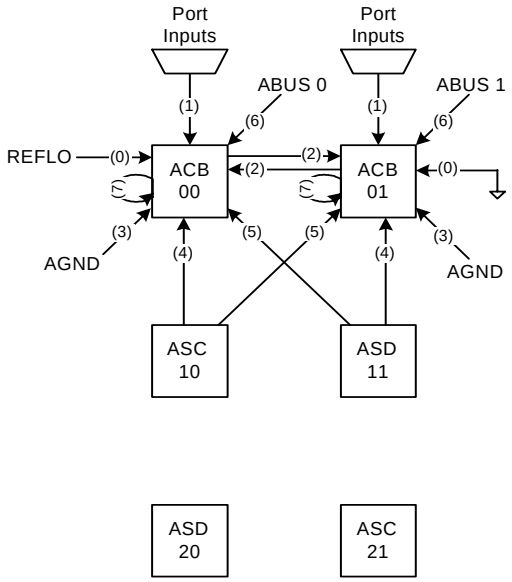

Figure 19-3. PMux Connections

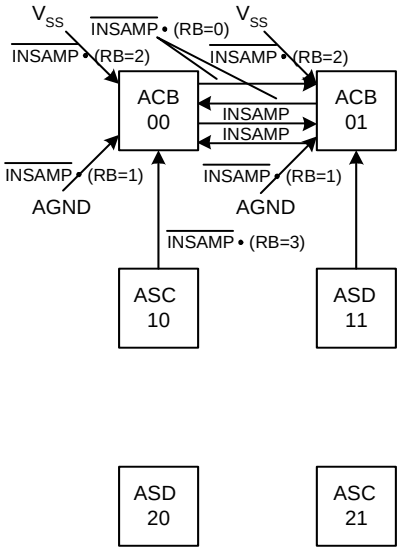

Figure 19-4. RBotMux Connections

The ACMux, as shown in the Analog Switch Cap Type C Block xx Control 1 register, controls the input muxing for both the A and C capacitor branches. The high order bit, ACMux[2], selects one of two inputs for the C branch. See the individual AMux and CMux diagrams.

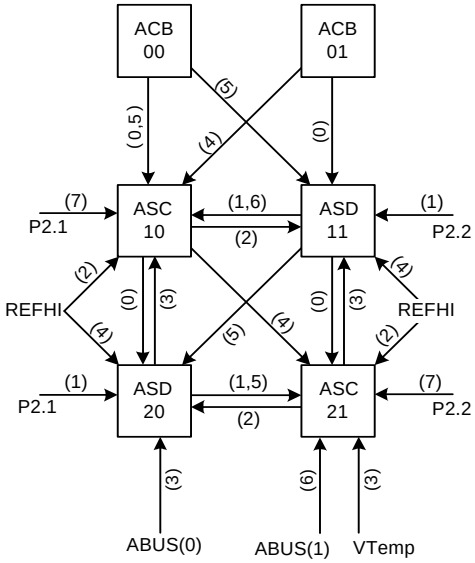

Figure 19-5. AMux Connections

20.2 Architectural Description

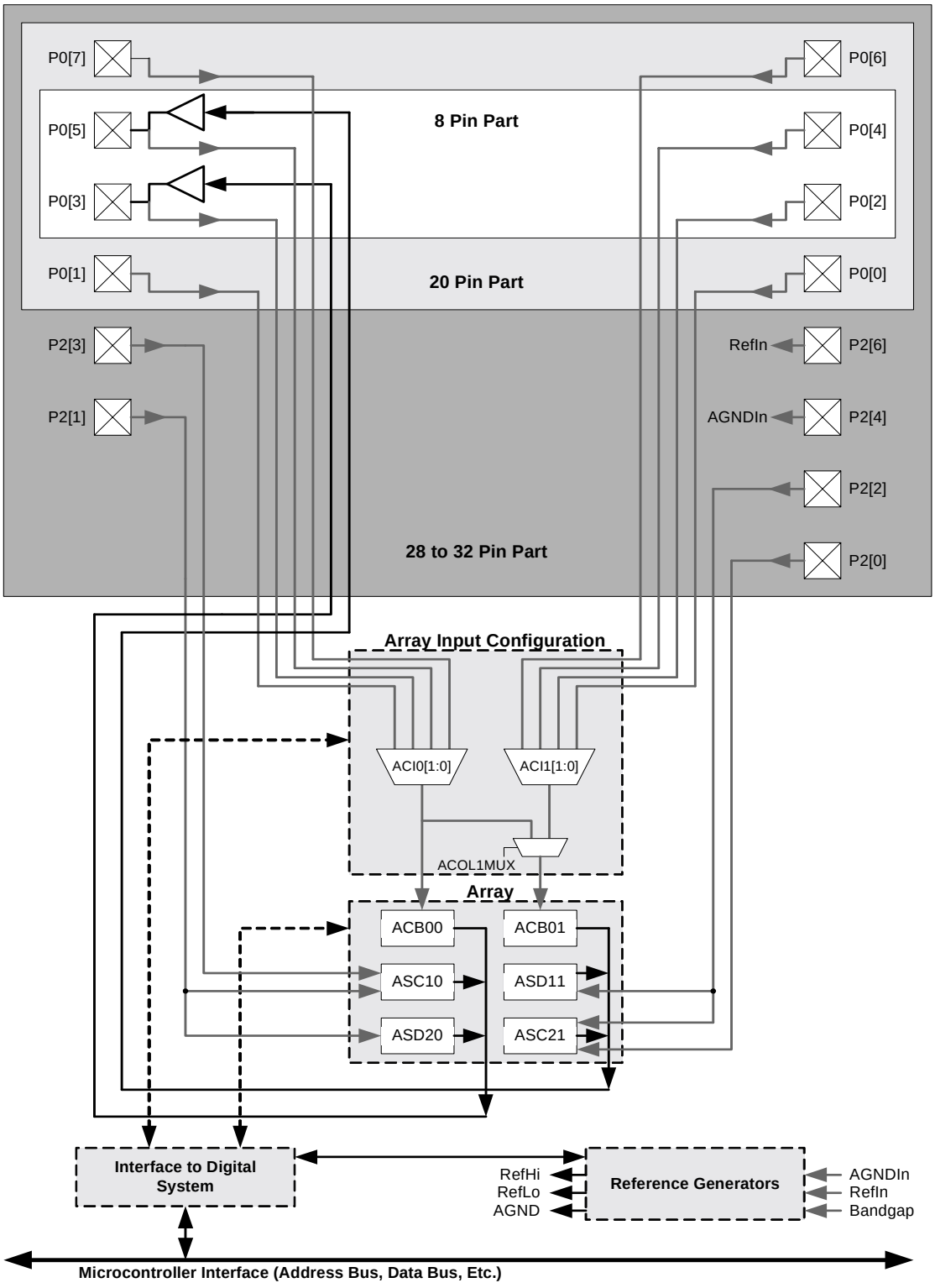

Figure 20-1. Analog Pin Block Diagram

Analog Switch Cap Type C PSoC Block Control Registers

22.3.1 ASCxxCR0 Register

Bit 7: FCap. This bit controls the size of the switched feedback capacitor in the integrator.

Bit 6: ClockPhase. This bit controls the internal clock phasing relative to the input clock phasing. ClockPhase affects the output of the analog column bus, which is controlled by the AnalogBus bit in Control 2 Register (ASC10CR2, ASC21CR2).

Bit[6] is the ClockPhase select that inverts the clock internal to the blocks. During normal operation of an SC block for the amplifier of a column enabled to drive the output bus, the connection is only made for the last half of PHI2 (during PHI1 and for the first half of PHI2, the output bus floats at the last voltage to which it was driven). This forms a sample and hold operation using the output bus and its associated capacitance. This design prevents the output bus from being perturbed by the intermediate states of the SC operation (often a reset state for PHI1 and settling to the valid state during PHI2).

Following are the exceptions: 1) If the ClockPhase bit in CR0 (for the SC block in question) is set to 1, then the output is enabled for the whole of PHI2. 2) If the SHDIS signal is set in bit 6 of the Analog Clock Source Control Register, then sample and hold operation is disabled for all columns and all enabled outputs of SC blocks are connected to their respective output busses for the entire period of their respective PHI2s.

This bit also affects the latching of the comparator output (CBUS). Both clock phases, PHI1 and PHI2, are involved in the output latching mechanism. The capture of the next value to be output from the latch (capture point event) happens during the falling edge of one clock phase, and the rising edge of the other clock phase will cause the value to come out (output point event). This bit determines which clock phase triggers the capture point event, and the other clock will trigger the output point event. The value output to the comparator bus will remain stable between output point events.

Bit 5: ASign. This bit controls the switch phasing of the switches on the bottom plate of the ACap capacitor. The bottom plate samples the input or the reference.

Bits 4 to 0: ACap[4:0]. The ACap bits set the value of the capacitor in the A path.

For additional information, reference the ASCxxCR0 register on page 112.

22.3.2 ASCxxCR1 Register

Bits 7, 6, and 5: ACMUX[2:0]. ACMux controls the input muxing for both the A and C capacitor branches. The high order bit, ACMux[2], selects one of two inputs for the C branch.

Bits 4 to 0: BCap[4:0]. The BCap bits set the value of the capacitor in the B path.

For additional information, reference the ASCxxCR1 register on page 113.

22.3.3 ASCxxCR2 Register

Bit 7: AnalogBus. This bit gates the output to the analog column bus. The output on the analog column bus is affected by the state of the ClockPhase bit in Control 0 Register (ASC10CR0, ASC21CR0). If AnalogBus is set to 0, the output to the analog column bus is tri-stated. If AnalogBus is set to 1, the signal that is output to the analog column bus is selected by the ClockPhase bit. If the ClockPhase bit is 0, the block output is gated by sampling clock on last part of PHI2. If the ClockPhase bit is 1, the block output continuously drives the analog column bus (ABUS).

Bit 6: CompBus. This bit controls the output to the column comparator bus (CBUS). Note that if the comparator bus is not driven by anything in the column, it is pulled low. The comparator output is evaluated on the rising edge of internal PHI1 and is latched so it is available during internal PHI2.

Bit 5: AutoZero. This bit controls the shorting of the output to the inverting input of the opamp. When shorted, the opamp is basically a follower. The output is the opamp offset. By using the feedback capacitor of the integrator, the block can memorize the offset and create an offset cancellation scheme. AutoZero also controls a pair of switches between the A and B branches and the summing node of the opamp. If AutoZero is enabled, then the pair of switches is active. AutoZero also affects the function of the FSW1 bit in Control 3 Register.

Bits 4 to 0: CCap[4:0]. The CCap bits set the value of the capacitor in the C path.

For additional information, reference the ASCxxCR2 register on page 114.

DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only.

5V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Low Power	–	1.6	10	mV	
	Input Offset Voltage (absolute value) Mid Power	–	1.3	8	mV	
	Input Offset Voltage (absolute value) High Power	–	1.2	7.5	mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/ºC	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25ºC.
V_{CMOA}	Common Mode Voltage Range	0.0	–	Vdd	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
	Common Mode Voltage Range (high power or high opamp bias)	0.5	–	Vdd-0.5		
G_{OLOA}	Open Loop Gain		–	–	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
	Power=Low	60				
	Power=Medium	60				
	Power=High	80				
$V_{OHIGHOA}$	High Output Voltage Swing (worst case internal load)					
	Power=Low	Vdd-0.2	–	–	V	
	Power=Medium	Vdd-0.2	–	–	V	
	Power=High	Vdd-0.5	–	–	V	
V_{OLOWOA}	Low Output Voltage Swing (worst case internal load)					
	Power=Low	–	–	0.2	V	
	Power=Medium	–	–	0.2	V	
	Power=High	–	–	0.5	V	
I_{SOA}	Supply Current (including associated AGND buffer)					
	Power=Low	–	150	200	µA	
	Power=Low, Opamp Bias=High	–	300	400	µA	
	Power=Medium	–	600	800	µA	
	Power=Medium, Opamp Bias=High	–	1200	1600	µA	
	Power=High	–	2400	3200	µA	
	Power=High, Opamp Bias=High	–	4600	6400	µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	60	–	–	dB	

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO}	Internal Main Oscillator Frequency	23.4	24	24.6[a,c]	MHz	Trimmed. Utilizing factory trim values.
F_{CPU1}	CPU Frequency (5 V Nominal)	0.93	24	24.6[a,b]	MHz	
F_{CPU2}	CPU Frequency (3.3V Nominal)	0.93	12	12.3[b,c]	MHz	
F_{48M}	Digital PSoC Block Frequency	0	48	49.2[a,b,d]	MHz	Refer to the AC Digital Block Specifications below.
F_{24M}	Digital PSoC Block Frequency	0	24	24.6[b,e,d]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{PLL}	PLL Frequency	–	23.986	–	MHz	Is a multiple (x732) of crystal frequency.
Jitter24M2	24 MHz Period Jitter (PLL)	600	–		ps	
$T_{PLLSLEW}$	PLL Lock Time	0.5	–	10	ms	
$T_{PLLSLEWSLOW}$	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	
T_{OS}	External Crystal Oscillator Startup to 1%	–	1700	2620	ms	
T_{OSACC}	External Crystal Oscillator Startup to 100 ppm	–	2800	3800[f]	ms	
Jitter32k	32 kHz Period Jitter	–	100		ns	
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2[a,c]	MHz	Trimmed. Utilizing factory trim values.
Jitter24M1	24 MHz Period Jitter (IMO)	–	600		ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12	MHz	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	

a. 4.75V < Vdd < 5.25V.
b. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
c. 3.0V < Vdd < 3.6V.
d. See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on maximum frequency for User Modules.
e. 3.0V < 5.25V.
f. The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 uW maximum drive level 32.768 kHz crystal. 3.0V ≤ Vdd ≤ 5.5V, -40 °C ≤ T_A ≤ 85 °C.

AC General Purpose IO (GPIO) Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12	MHz	
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.5V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.5V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	Vdd = 3 to 5.5V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	Vdd = 3 to 5.5V, 10% - 90%

AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

5V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	–	–	2.5	µs	
	Power = High	–	–	2.5	µs	
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	–	–	2.2	µs	
	Power = High	–	–	2.2	µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load					
	Power = Low	0.65	–	–	V/µs	
	Power = High	0.65	–	–	V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load					
	Power = Low	0.65	–	–	V/µs	
	Power = High	0.65	–	–	V/µs	
BW_{OB}	Small Signal Bandwidth, 20mV_{pp}, 3dB BW, 100pF Load					
	Power = Low	0.8	–	–	MHz	
	Power = High	0.8	–	–	MHz	
BW_{OB}	Large Signal Bandwidth, 1V_{pp}, 3dB BW, 100pF Load					
	Power = Low	300	–	–	kHz	
	Power = High	300	–	–	kHz	

3.3V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	–	–	3.8	µs	
	Power = High	–	–	3.8	µs	
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	–	–	2.6	µs	
	Power = High	–	–	2.6	µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load					
	Power = Low	.5	–	–	V/µs	
	Power = High	.5	–	–	V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load					
	Power = Low	.5	–	–	V/µs	
	Power = High	.5	–	–	V/µs	
BW_{OB}	Small Signal Bandwidth, 20mV_{pp}, 3dB BW, 100pF Load					
	Power = Low	0.7	–	–	MHz	
	Power = High	0.7	–	–	MHz	
BW_{OB}	Large Signal Bandwidth, 1V_{pp}, 3dB BW, 100pF Load					
	Power = Low	200	–	–	kHz	
	Power = High	200	–	–	kHz	