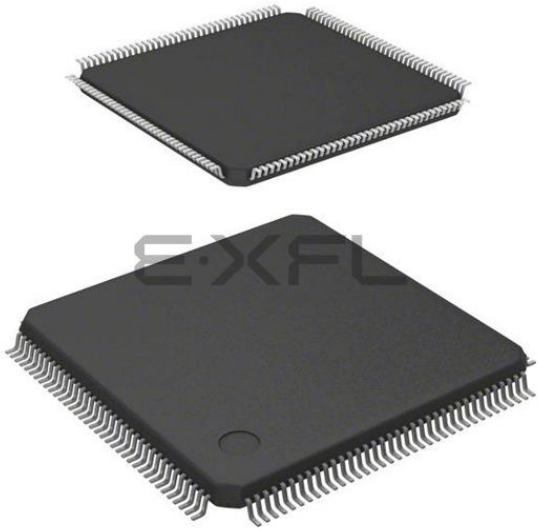

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	64MHz
Connectivity	ASC, CANbus, EBI/EMI, I²C, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	144-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10f272z2q3

Table 32. Compare modes

Compare Modes	Function
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated
Mode 3	Pin set ‘1’ on match; pin reset ‘0’ on compare time overflow; only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; pin toggles on each compare match; several compare events per timer period are possible.

Table 33. CAPCOM timer input frequencies, resolutions and periods at 40 MHz

f_{CPU} = 40 MHz	Timer Input Selection TxI							
	000b	001b	010b	011b	100b	101b	110b	111b
Prescaler for f_{CPU}	8	16	32	64	128	256	512	1024
Input Frequency	5 MHz	2.5 MHz	1.25 MHz	625 kHz	312.5 kHz	156.25 kHz	78.125 kHz	39.1 kHz
Resolution	200 ns	400 ns	0.8 µs	1.6 µs	3.2 µs	6.4 µs	12.8 µs	25.6 µs
Period	13.1 ms	26.2 ms	52.4 ms	104.8 ms	209.7 ms	419.4 ms	838.9 ms	1.678 s

Table 34. CAPCOM timer input frequencies, resolutions and periods at 64 MHz

f_{CPU} = 64 MHz	Timer Input Selection TxI							
	000b	001b	010b	011b	100b	101b	110b	111b
Prescaler for f_{CPU}	8	16	32	64	128	256	512	1024
Input Frequency	8 MHz	4 MHz	2 MHz	1 kHz	500 kHz	250 kHz	128 kHz	64 kHz
Resolution	125 ns	250 ns	0.5 µs	1.0 µs	2.0 µs	4.0 µs	8.0 µs	16.0 µs
Period	8.2 ms	16.4 ms	32.8 ms	65.5 ms	131.1 ms	262.1ms	524.3 ms	1.049 s

Table 35. GPT1 timer input frequencies, resolutions and periods at 40 MHz (continued)

f_{CPU} = 40 MHz	Timer Input Selection T2I / T3I / T4I							
	000b	**001b**	**010b**	**011b**	**100b**	**101b**	**110b**	**111b**
Resolution	200 ns	400 ns	0.8 µs	1.6 µs	3.2 µs	6.4 µs	12.8 µs	25.6 µs
Period maximum	13.1 ms	26.2 ms	52.4 ms	104.8 ms	209.7 ms	419.4 ms	838.9 ms	1.678 s

Table 36. GPT1 timer input frequencies, resolutions and periods at 64 MHz

f_{CPU} = 64 MHz	Timer Input Selection T2I / T3I / T4I							
	000b	**001b**	**010b**	**011b**	**100b**	**101b**	**110b**	**111b**
Pre-scaler factor	8	16	32	64	128	256	512	1024
Input Freq	8 MHz	4 MHz	2 MHz	1 kHz	500 kHz	250 kHz	128 kHz	64 kHz
Resolution	125 ns	250 ns	0.5 µs	1.0 µs	2.0 µs	4.0 µs	8.0 µs	16.0 µs
Period maximum	8.2 ms	16.4 ms	32.8 ms	65.5 ms	131.1 ms	262.1 ms	524.3 ms	1.049 s

Figure 10. Block diagram of GPT1

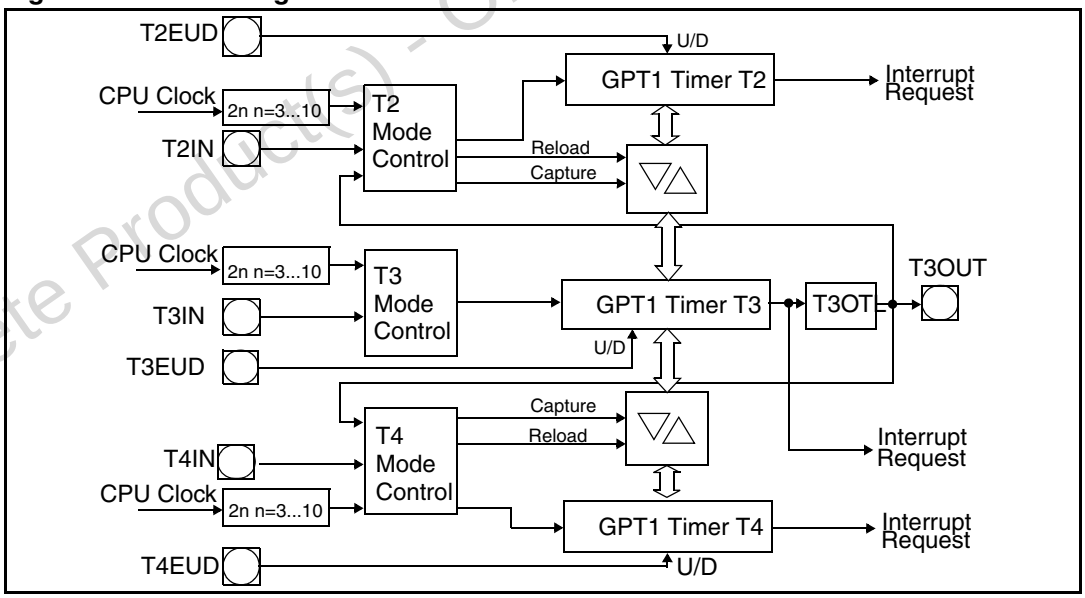


Table 43. ASC synchronous baud rates by reload value and deviation errors (f_{CPU} = 40 MHz)

S0BRS = '0', f_{CPU} = 40 MHz			S0BRS = '1', f_{CPU} = 40 MHz		
Baud Rate (Baud)	Deviation Error	Reload Value (hex)	Baud Rate (Baud)	Deviation Error	Reload Value (hex)
900	0.0% / 0.0%	15B2 / 15B3	600	0.0% / 0.0%	15B2 / 15B3
612	0.0% / 0.0%	1FE8 / 1FE9	407	0.0% / 0.0%	1FFD / 1FFE

Table 44. ASC synchronous baud rates by reload value and deviation errors (f_{CPU} = 64 MHz)

S0BRS = '0', f_{CPU} = 64 MHz			S0BRS = '1', f_{CPU} = 64 MHz		
Baud Rate (Baud)	Deviation Error	Reload Value (hex)	Baud Rate (Baud)	Deviation Error	Reload Value (hex)
8 000 000	0.0% / 0.0%	0000 / 0000	5 333 333	0.0% / 0.0%	0000 / 0000
112 000	+0.6% / -0.8%	0046 / 0047	112 000	+1.3% / -0.8%	002E / 002F
56 000	+0.6% / -0.1%	008D / 008E	56 000	+0.3% / -0.8%	005E / 005F
38 400	+0.2% / -0.3%	00CF / 00D0	38 400	+0.6% / -0.1%	0089 / 008A
19 200	+0.2% / -0.1%	019F / 01A0	19 200	+0.3% / -0.1%	0114 / 0115
9 600	+0.0% / -0.1%	0340 / 0341	9 600	+0.1% / -0.1%	022A / 022B
4 800	0.0% / 0.0%	0681 / 0682	4 800	0.0% / -0.1%	0456 / 0457
2 400	0.0% / 0.0%	0D04 / 0D05	2 400	0.0% / 0.0%	08AD / 08AE
1 200	0.0% / 0.0%	1A09 / 1A0A	1 200	0.0% / 0.0%	115B / 115C
977	0.0% / 0.0%	1FFB / 1FFC	900	0.0% / 0.0%	1724 / 1725
			652	0.0% / 0.0%	1FF2 / 1FF3

Note: The deviation errors given in the Table 43 and Table 44 are rounded. To avoid deviation errors use a Baud rate crystal (providing a multiple of the ASC0 sampling frequency)

15.4 High speed synchronous serial interfaces

The High-Speed Synchronous Serial Interfaces (SSC0 and SSC1) provides flexible high-speed serial communication between the ST10F272Z2 and other microcontrollers, microprocessors or external peripherals.

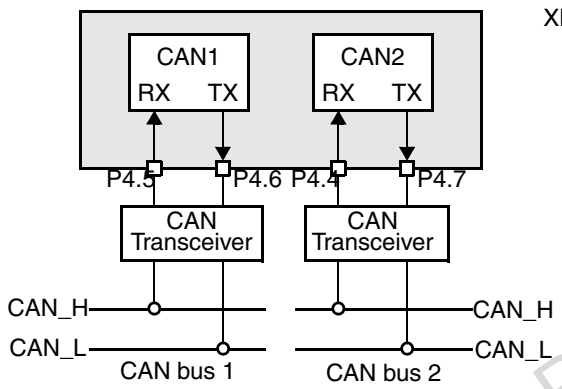
The SSCx supports full-duplex and half-duplex synchronous communication. The serial clock signal can be generated by the SSCx itself (master mode) or be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable.

This allows communication with SPI-compatible devices. Transmission and reception of data is double-buffered. A 16-bit Baud rate generator provides the SSCx with a separate serial clock signal. The serial channel SSCx has its own dedicated 16-bit Baud rate generator with 16-bit reload capability, allowing Baud rate generation independent from the timers.

Multiple CAN bus

The ST10F272Z2 provides two CAN interfaces to support such kind of bus configuration as shown in *Figure 15*.

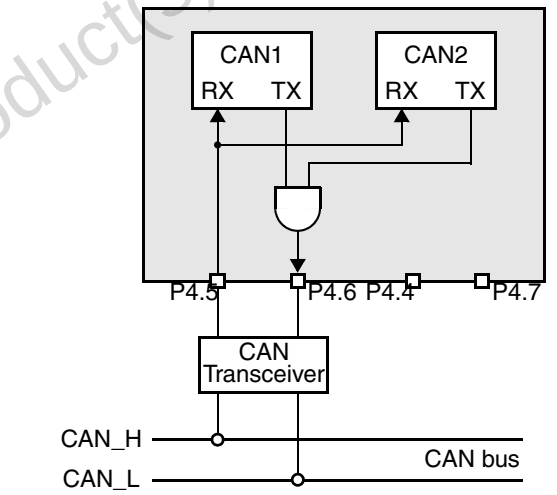
Figure 15. Connection to two different CAN buses (e.g. for gateway application)



Parallel Mode

In addition to previous configurations, a parallel mode is supported. This is shown in *Figure 16*.

Figure 16. Connection to one CAN bus with internal Parallel Mode enabled



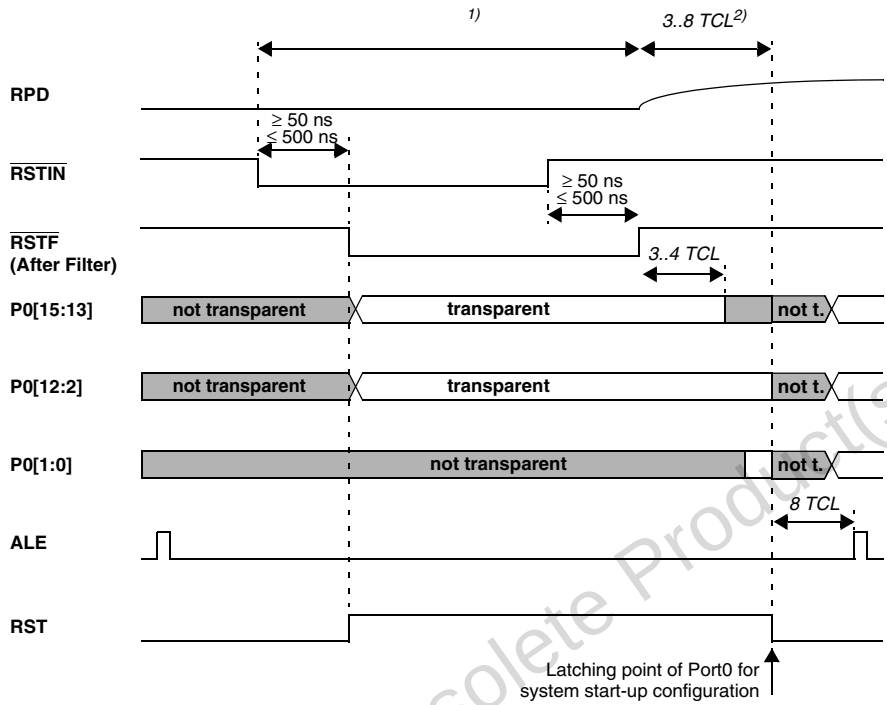
1. P4.4 and P4.7 when not used as CAN functions can be used as general purpose I/O while they cannot be used as external bus address lines.

sufficient: anyway, a maximum of 100 nF on V_{18} pin should not generate problems of over-current (higher value is allowed if current is limited by the external hardware). External current limitation is anyway recommended also to avoid risks of damage in case of temporary short between V_{18} and ground: the internal 1.8 V drivers are sized to drive currents of several tens of Ampere, so the current shall be limited by the external hardware. The limit of current is imposed by power dissipation considerations (Refer to Electrical Characteristics Section).

In next Figures *17* and *18* Asynchronous Power-on timing diagrams are reported, respectively with boot from internal or external memory, highlighting the reset phase extension introduced by the embedded FLASH module when selected.

Note: Never power the device without keeping $\overline{RSTIN}$ pin grounded: the device could enter in unpredictable states, risking also permanent damages.

Figure 20. Asynchronous hardware RESET ($\overline{EA}$ = 0)



Note 1. Longer than Port0 settling time + PLL synchronization (if needed, that is P0(15:13) changed)
Longer than 500ns to take into account of Input Filter on RSTIN pin

Note 2. 3 to 8 TCL depending on clock source selection.

Exit from asynchronous reset state

When the $\overline{RSTIN}$ pin is pulled high, the device restarts: as already mentioned, if internal FLASH is used, the restarting occurs after the embedded Flash initialization routine is completed. The system configuration is latched from Port0: ALE, $\overline{RD}$ and $\overline{WR}$/$\overline{WRL}$ pins are driven to their inactive level. The ST10F272Z2 starts program execution from memory location 00'0000h in code segment 0. This starting location will typically point to the general initialization routine. Timing of asynchronous Hardware Reset sequence are summarized in *Figure 19* and *Figure 20*.

20.3 Synchronous reset (warm reset)

A synchronous reset is triggered when $\overline{RSTIN}$ pin is pulled low while RPD pin is at high level. In order to properly activate the internal reset logic of the device, the $\overline{RSTIN}$ pin must be held low, at least, during 4 TCL (2 periods of CPU clock): refer also to *Section 20.1* for details on minimum reset pulse duration. The I/O pins are set to high impedance and $\overline{RSTOUT}$ pin is driven low. After $\overline{RSTIN}$ level is detected, a short duration of a maximum of 12 TCL (six periods of CPU clock) elapses, during which pending internal hold states are cancelled and the current internal access cycle if any is completed. External bus cycle is aborted. The internal pull-down of $\overline{RSTIN}$ pin is activated if bit BDRSTEN of SYSCON register was previously set by software. Note that this bit is always cleared on power-on or after a reset sequence.

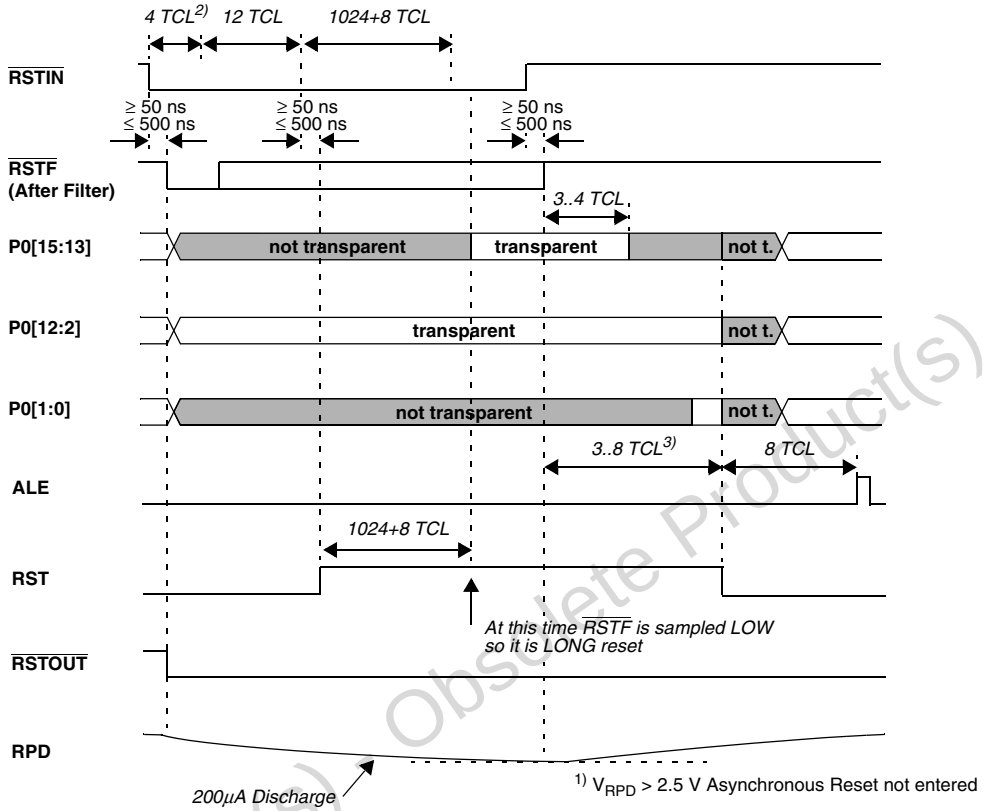
Synchronous reset and RPD pin

Whenever the $\overline{\text{RSTIN}}$ pin is pulled low (by external hardware or as a consequence of a Bidirectional reset), the RPD internal weak pull-down is activated. The external capacitance (if any) on RPD pin is slowly discharged through the internal weak pull-down. If the voltage level on RPD pin reaches the input low threshold (around 2.5 V), the reset event becomes immediately asynchronous. In case of hardware reset (short or long) the situation goes immediately to the one illustrated in *Figure 19*. There is no effect if RPD comes again above the input threshold: the asynchronous reset is completed coherently. To grant the normal completion of a synchronous reset, the value of the capacitance shall be big enough to maintain the voltage on RPD pin sufficient high along the duration of the internal reset sequence.

For a Software or Watchdog reset events, an active synchronous reset is completed regardless of the RPD status.

It is important to highlight that the signal that makes RPD status transparent under reset is the internal $\overline{\text{RSTF}}$ (after the noise filter).

Figure 24. Synchronous long hardware RESET ($\overline{EA}$ = 0)



Notes:

1. *If during the reset condition ($\overline{RSTIN}$ low), RPD voltage drops below the threshold voltage (about 2.5 V for 5 V operation), the asynchronous reset is then immediately entered.*
2. *Minimum $\overline{RSTIN}$ low pulse duration shall also be longer than 500ns to guarantee the pulse is not masked by the internal filter (refer to Section 21.1).*
3. *3 to 8 TCL depending on clock source selection.*

20.4 Software reset

A software reset sequence can be triggered at any time by the protected SRST (software reset) instruction. This instruction can be deliberately executed within a program, e.g. to leave bootstrap loader mode, or on a hardware trap that reveals system failure.

On execution of the SRST instruction, the internal reset sequence is started. The microcontroller behavior is the same as for a synchronous short reset, except that only bits P0.12...P0.8 are latched at the end of the reset sequence, while previously latched, bits P0.7...P0.2 are cleared (that is written at '1').

A Software reset is always taken as synchronous: there is no influence on Software Reset behavior with RPD status. In case Bidirectional Reset is selected, a Software Reset event pulls $\overline{RSTIN}$ pin low: this occurs only if RPD is high; if RPD is low, $\overline{RSTIN}$ pin is not pulled low even though Bidirectional Reset is selected.

Before entering Power Down mode (by executing the instruction PWRDN), bit VREGOFF in XMISC register must be set.

Note: Leaving the main voltage regulator active during Power Down may lead to unexpected behavior (ex: CPU wake-up) and power consumption higher than what specified.

21.2.1 Protected power down mode

This mode is selected when PWDCFG (bit 5) of SYSCON register is cleared. The Protected Power Down mode is only activated if the $\overline{\text{NMI}}$ pin is pulled low when executing PWRDN instruction (this means that the PWRD instruction belongs to the $\overline{\text{NMI}}$ software routine). This mode is only deactivated with an external hardware reset on $\overline{\text{RSTIN}}$ pin.

21.2.2 Interruptible power down mode

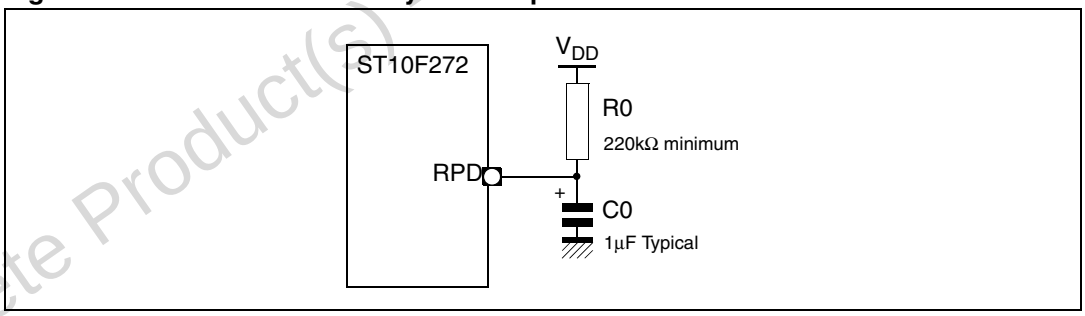
This mode is selected when PWDCFG (bit 5) of SYSCON register is set.

The Interruptible Power Down mode is only activated if all the enabled Fast External Interrupt pins are in their inactive level.

This mode is deactivated with an external reset applied to $\overline{\text{RSTIN}}$ pin or with an interrupt request applied to one of the Fast External Interrupt pins, or with an interrupt generated by the Real-Time Clock, or with an interrupt generated by the activity on CAN's and I^2C module interfaces. To allow the internal PLL and clock to stabilize, the $\overline{\text{RSTIN}}$ pin must be held low according the recommendations described in *Chapter 20: System reset on page 81*.

An external RC circuit must be connected to RPD pin, as shown in the *Figure 36*.

Figure 36. External RC circuitry on RPD pin



To exit Power Down mode with an external interrupt, an EXxIN (x = 7...0) pin has to be asserted for at least 40 ns.

21.3 Stand-by mode

In Stand-by mode, it is possible to turn off the main V_{DD} provided that V_{STBY} is available through the dedicated pin of the ST10F272Z2.

To enter Stand-by mode it is mandatory to held the device under reset: once the device is under reset, the RAM is disabled (see XRAM2EN bit of XPERCON register), and its digital interface is frozen in order to avoid any kind of data corruption.

A dedicated embedded low-power voltage regulator is implemented to generate the internal low voltage supply (about 1.65 V in Stand-by mode) to bias all those circuits that shall remain active: the portion of XRAM, the RTC counters and 32 kHz on-chip oscillator amplifier.

Table 53. List of special function registers (continued)

Name		Physical address		8-bit address	Description	Reset value
ODP7	b	F1D2h	E	E9h	Port 7 open drain control register	- - 00h
ODP8	b	F1D6h	E	EBh	Port 8 open drain control register	- - 00h
ONES	b	FF1Eh		8Fh	Constant value 1's register (read only)	FFFFh
P0L	b	FF00h		80h	PORT0 low register (lower half of PORT0)	- - 00h
P0H	b	FF02h		81h	PORT0 high register (upper half of PORT0)	- - 00h
P1L	b	FF04h		82h	PORT1 low register (lower half of PORT1)	- - 00h
P1H	b	FF06h		83h	PORT1 high register (upper half of PORT1)	- - 00h
P2	b	FFC0h		E0h	Port 2 register	0000h
P3	b	FFC4h		E2h	Port 3 register	0000h
P4	b	FFC8h		E4h	Port 4 register (8-bit)	- - 00h
P5	b	FFA2h		D1h	Port 5 register (read only)	XXXXh
P6	b	FFCCh		E6h	Port 6 register (8-bit)	- - 00h
P7	b	FFD0h		E8h	Port 7 register (8-bit)	- - 00h
P8	b	FFD4h		EAh	Port 8 register (8-bit)	- - 00h
P5DIDIS	b	FFA4h		D2h	Port 5 digital disable register	0000h
PECC0		FEC0h		60h	PEC channel 0 control register	0000h
PECC1		FEC2h		61h	PEC channel 1 control register	0000h
PECC2		FEC4h		62h	PEC channel 2 control register	0000h
PECC3		FEC6h		63h	PEC channel 3 control register	0000h
PECC4		FEC8h		64h	PEC channel 4 control register	0000h
PECC5		FECAh		65h	PEC channel 5 control register	0000h
PECC6		FECCh		66h	PEC channel 6 control register	0000h
PECC7		FECEh		67h	PEC channel 7 control register	0000h
PICON	b	F1C4h	E	E2h	Port input threshold control register	- - 00h
PP0		F038h	E	1Ch	PWM module period register 0	0000h
PP1		F03Ah	E	1Dh	PWM module period register 1	0000h
PP2		F03Ch	E	1Eh	PWM module period register 2	0000h
PP3		F03Eh	E	1Fh	PWM module period register 3	0000h
PSW	b	FF10h		88h	CPU program status word	0000h
PT0		F030h	E	18h	PWM module up/down counter 0	0000h
PT1		F032h	E	19h	PWM module up/down counter 1	0000h
PT2		F034h	E	1Ah	PWM module up/down counter 2	0000h
PT3		F036h	E	1Bh	PWM module up/down counter 3	0000h
PW0		FE30h		18h	PWM module pulse width register 0	0000h

Table 54. List of XBus registers (continued)

Name	Physical address	Description	Reset value
CAN2IF2A1	EE48h	CAN2: IF2 arbitration 1	0000h
CAN2IF2A2	EE4Ah	CAN2: IF2 arbitration 2	0000h
CAN2IF2CM	EE42h	CAN2: IF2 command mask	0000h
CAN2IF2CR	EE40h	CAN2: IF2 command request	0001h
CAN2IF2DA1	EE4Eh	CAN2: IF2 data A 1	0000h
CAN2IF2DA2	EE50h	CAN2: IF2 data A 2	0000h
CAN2IF2DB1	EE52h	CAN2: IF2 data B 1	0000h
CAN2IF2DB2	EE54h	CAN2: IF2 data B 2	0000h
CAN2IF2M1	EE44h	CAN2: IF2 mask 1	FFFFh
CAN2IF2M2	EE46h	CAN2: IF2 mask 2	FFFFh
CAN2IF2MC	EE4Ch	CAN2: IF2 message control	0000h
CAN2IP1	EEA0h	CAN2: interrupt pending 1	0000h
CAN2IP2	EEA2h	CAN2: interrupt pending 2	0000h
CAN2IR	EE08h	CAN2: interrupt register	0000h
CAN2MV1	EEB0h	CAN2: message valid 1	0000h
CAN2MV2	EEB2h	CAN2: message valid 2	0000h
CAN2ND1	EE90h	CAN2: new data 1	0000h
CAN2ND2	EE92h	CAN2: new data 2	0000h
CAN2SR	EE02h	CAN2: status register	0000h
CAN2TR	EE0Ah	CAN2: test register	00x0h
CAN2TR1	EE80h	CAN2: transmission request 1	0000h
CAN2TR2	EE82h	CAN2: Transmission request 2	0000h
I2CCCR1	EA06h	I2C clock control register 1	0000h
I2CCCR2	EA0Eh	I2C clock control register 2	0000h
I2CCR	EA00h	I2C control register	0000h
I2CDR	EA0Ch	I2C data register	0000h
I2COAR1	EA08h	I2C own address register 1	0000h
I2COAR2	EA0Ah	I2C own address register 2	0000h
I2CSR1	EA02h	I2C status register 1	0000h
I2CSR2	EA04h	I2C status register 2	0000h
RTCAH	ED14h	RTC alarm register high byte	XXXXh
RTCAL	ED12h	RTC alarm register low byte	XXXXh
RTCCON	ED00H	RTC control register	000Xh
RTCDH	ED0Ch	RTC divider counter high byte	XXXXh

24.3 Transmission request disabled (C-CAN module)

Description

The transmission request of a message object may remain disabled (even if the host immediately enables it again) in the following situations:

1. if the host disables the pending transmission request of the lowest-priority message object (number 32 by default) in the short time window during which the message handler state machine prepares the transmission of the message
2. if the transmission has not started.

Reading the transmission request bit of this message object does not show that the transmission request is disabled. This only happens when this message object is the only one with a pending transmission request.

If the transmission request is blocked in the disabled state, it will be re-enabled by the first activity detected on the CAN bus or by setting the transmission request of any other message object.

The other message objects are not affected by this phenomenon.

Workaround

It is usually not necessary to disable the transmission request of a message object. If the message object is to be used for another message, it is sufficient to prepare the new content for this message object in the CPU interface register (Identifier, DLC, Data, with TxRqst and NewDat [optionally TxIE] bits) and to transfer this content into the message object. The new content is transmitted at the next opportunity. It is not altered by a possibly ongoing transmission of the previous content of the same message object.

Table 65. DC characteristics (continued)

Parameter	Symbol	Limit values		Unit	Test Condition
		min.	max.		
Power Down supply current (11) *(RTC off, Oscillators off, Main Voltage Regulator off)*	I_{PD1}	–	400	µA	T_A = 25 °C
Power Down supply current (11) *(RTC on, Main Oscillator on, Main Voltage Regulator off)*	I_{PD2}	–	400 *Typical Value*	µA	T_A = 25 °C
Power Down supply current (11) *(RTC on, 32kHz Oscillator on, Main Voltage Regulator off)*	I_{PD3}	–	400	µA	T_A = 25 °C
Stand-by supply current (11) *(RTC off, Oscillators off, V_{DD} off, V_{STBY} on)*	I_{SB1}	–	120	µA	V_{STBY} = 5.5 V $T_A = T_J$ = 25°C
		–	500	µA	V_{STBY} = 5.5 V $T_A = T_J$ = 125 °C
Stand-by supply current (11) *(RTC on, 32kHz Oscillator on, main V_{DD} off, V_{STBY} on)*	I_{SB2}	–	120	µA	V_{STBY} = 5.5 V T_A = 25°C
Stand-by supply current (1) (11) *(V_{DD} transient condition)*	I_{SB3}	–	2.5	mA	–

1. Not 100% tested, guaranteed by design characterization.
2. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is imposed by the external circuitry.
3. Port 5 leakage values are granted for not selected A/D Converter channel. One channels is always selected (by default, after reset, P5.0 is selected). For the selected channel the leakage value is similar to that of other port pins.
4. The leakage of P2.0 is higher than other pins due to the additional logic (pass gates active only in specific test modes) implemented on input path. Pay attention to not stress P2.0 input pin with negative overload beyond the specified limits: failures in Flash reading may occur (sense amplifier perturbation). Refer to next *Figure 40* for a scheme of the input circuitry.
5. Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD} + 0.3$ V or $V_{OV} < -0.3$ V). The absolute sum of input overload currents on all port pins may not exceed 50mA. The supply voltage must remain within the specified limits.
6. This specification is only valid during Reset, or during Hold- or Adapt-mode. Port 6 pins are only affected, if they are used for $\overline{CS}$ output and the open drain function is not enabled.
7. The maximum current may be drawn while the respective signal line remains inactive.
8. The minimum current must be drawn in order to drive the respective signal line active.
9. The power supply current is a function of the operating frequency (f_{CPU} is expressed in MHz). This dependency is illustrated in the Figure 41 below. This parameter is tested at V_{DDmax} and at maximum CPU clock frequency with all outputs disconnected and all inputs at V_{IL} or V_{IH}, $\overline{RSTIN}$ pin at V_{IH1min}: **this implies I/O current is not considered**. The device is doing the following:
   – *Fetching code from IRAM and XRAM1, accessing in read and write to both XRAM modules* ***(for ICC1)***
   Fetching code from all sectors of IFlash, accessing in read (few fetches) and write to XRAM ***(for ICC2)***
   – *Watchdog Timer is enabled and regularly serviced*
   – *RTC is running with main oscillator clock as reference, generating a tick interrupts every 192 clock cycles*
   – *Four channel of XPWM are running (waves period: 2, 2.5, 3 and 4 CPU clock cycles): no output toggling*
   – *Five General Purpose Timers are running in timer mode with prescaler equal to 8 (T2, T3, T4, T5, T6)*
   – *ADC is in* **Auto Scan Continuous Conversion mode** *on all 16 channels of Port5*
   – *All interrupts generated by XPWM, RTC, Timers and ADC are not serviced*
10. The Idle mode supply current is a function of the operating frequency (f_{CPU} is expressed in MHz). This dependency is illustrated in the *Figure 40* below. These parameters are tested and at maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}, $\overline{RSTIN}$ pin at V_{IH1min}.
11. This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} – 0.1 V to V_{DD}, V_{AREF} = 0 V, all outputs (including pins configured as outputs) disconnected. Besides, the Main Voltage Regulator is assumed off: in case it is not, additional 1mA shall be assumed.

25.6 Flash characteristics

V_{DD} = 5 V ± 10%, V_{SS} = 0 V

Table 66. Flash characteristics

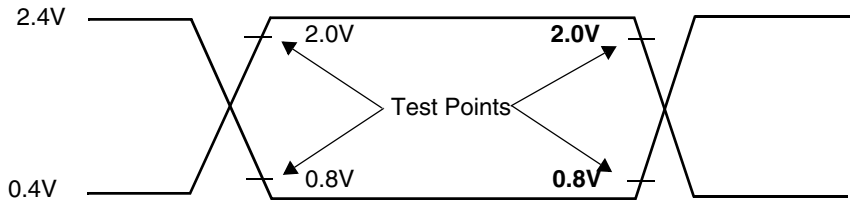
Parameter	Typical	Maximum		Unit	Notes
	T_A = 25°C	T_A = 125°C			
	0 cycles(1)	0 cycles(1)	100k cycles		
Word Program (32-bit) (2)	35	80	290	µs	–
Double Word Program (64-bit)(2))	60	150	570	µs	–
Bank 0 Program (256K) (Double Word Program)	1.6	2.0	3.9	s	–
Sector Erase (8K)	0.6 0.5	0.9 0.8	1.0 0.9	s	not preprogrammed preprogrammed
Sector Erase (32K)	1.1 0.8	2.0 1.8	2.7 2.5	s	not preprogrammed preprogrammed
Sector Erase (64K)	1.7 1.3	3.7 3.3	5.1 4.7	s	not preprogrammed preprogrammed
Bank 0 Erase (256K) (3)	5.6 4.0	13.6 11.9	19.2 17.5	s	not preprogrammed preprogrammed
Recovery from Power-Down (t_{PD})	–	40	40	µs	(4)
Program Suspend Latency (4)	–	10	10	µs	
Erase Suspend Latency (4)	–	30	30	µs	
Erase Suspend Request Rate (4)	20	20	20	ms	Min delay between 2 requests
Set Protection (4)	40	90	300	µs	

1. The figures are given after about 100 cycles due to testing routines (0 cycles at the final customer).
2. Word and Double Word Programming times are provided as average values derived from a full sector programming time: absolute value of a Word or Double Word Programming time could be longer than the average value.
3. Bank Erase is obtained through a multiple Sector Erase operation (setting bits related to all sectors of the Bank). As ST10F272Z2 implements only one bank, the Bank Erase operation is equivalent to Module and Chip Erase operations.
4. Not 100% tested, guaranteed by Design Characterization.

25.8 AC characteristics

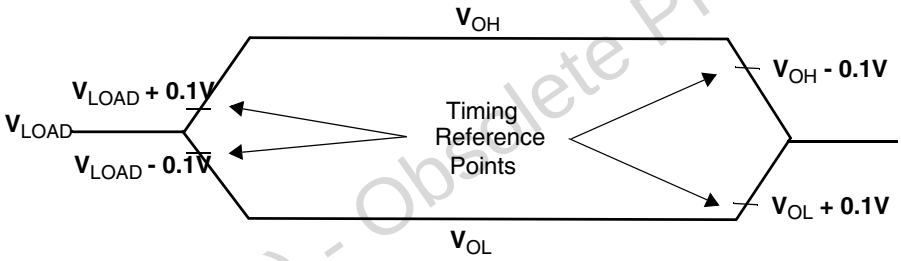
25.8.1 Test waveforms

Figure 46. Input / output waveforms



AC inputs during testing are driven at 2.4V for a logic '1' and 0.4V for a logic '0'.
Timing measurements are made at V_{IH} min. for a logic '1' and V_{IL} max for a logic '0'.

Figure 47. Float waveforms



For timing purposes a port pin is no longer floating when V_{LOAD} changes of ±100mV.
It begins to float when a 100mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20r

25.8.2 Definition of internal timing

The internal operation of the ST10F272Z2 is controlled by the internal CPU clock f_{CPU}. Both edges of the CPU clock can trigger internal (for example pipeline) or external (for example bus cycles) operations.

The specification of the external timing (AC Characteristics) therefore depends on the time between two consecutive edges of the CPU clock, called "TCL".

The CPU clock signal can be generated by different mechanisms. The duration of TCL and its variation (and also the derived external timing) depends on the mechanism used to generate f_{CPU}.

This influence must be regarded when calculating the timings for the ST10F272Z2.

The example for PLL operation shown in *Figure 48* refers to a PLL factor of 4.

The mechanism used to generate the CPU clock is selected during reset by the logic levels on pins P0.15-13 (P0H.7-5).

an external clock failure occurs, then the watchdog counter overflows (after 16 PLL clock cycles).

The CPU clock signal will be switched to the PLL free-running clock signal, and the oscillator watchdog Interrupt Request is flagged. The CPU clock will not switch back to the external clock even if a valid external clock exits on XTAL1 pin. Only a hardware reset (or bidirectional Software / Watchdog reset) can switch the CPU clock source back to direct clock input.

When the OWD is disabled, the CPU clock is always the external oscillator clock (in Direct Drive or Prescaler Operation) and the PLL is switched off to decrease consumption supply current.

25.8.7 Phase Locked Loop (PLL)

For all other combinations of pins P0.15-13 (P0H.7-5) during reset the on-chip phase locked loop is enabled and it provides the CPU clock (see *Table 70*). The PLL multiplies the input frequency by the factor F which is selected via the combination of pins P0.15-13 (f_{CPU} = f_{XTAL} x F). With every F'th transition of f_{XTAL} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothly, so the CPU clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{XTAL}. The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCLs.

The timings listed in the AC Characteristics that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances.

The real minimum value for TCL depends on the jitter of the PLL. The PLL tunes f_{CPU} to keep it locked on f_{XTAL}. The relative deviation of TCL is the maximum when it is referred to one TCL period.

This is especially important for bus cycles using wait states and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower Baud rates, etc.) the deviation caused by the PLL jitter is negligible. Refer to next *Section 25.8.9: PLL Jitter* for more details.

25.8.8 Voltage Controlled Oscillator

The ST10F272Z2 implements a PLL which combines different levels of frequency dividers with a Voltage Controlled Oscillator (VCO) working as frequency multiplier. In the following table, a detailed summary of the internal settings and VCO frequency is reported.

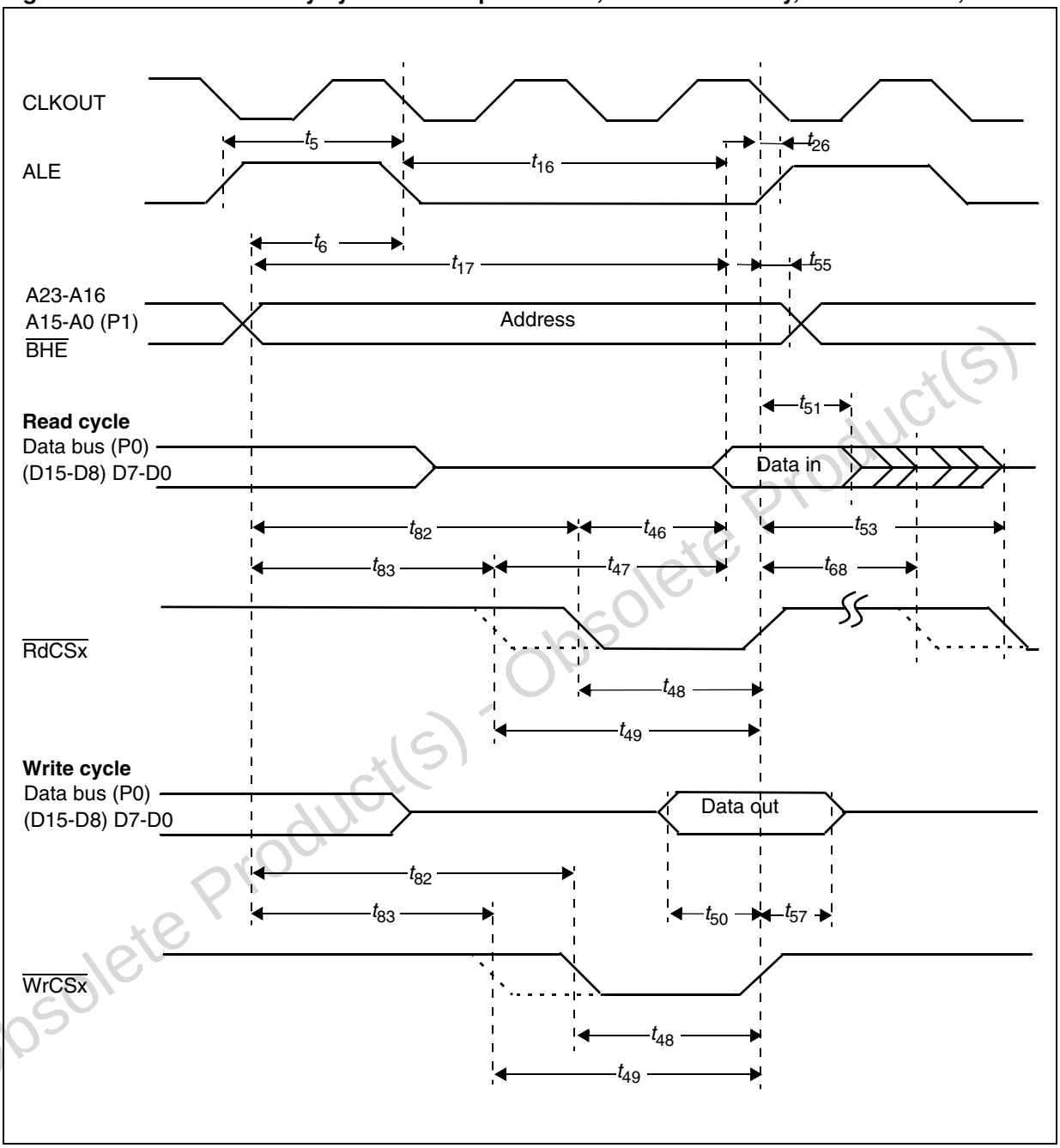
Table 71. Internal PLL divider mechanism

P0.15-13 (P0H.7-5)			XTAL Frequency	Input Prescaler	PLL		Output Prescaler	CPU Frequency $f_{CPU} = f_{XTAL}$ x F
					Multiply by	Divide by		
1	1	1	4 to 8 MHz	F_{XTAL} / 4	64	4	–	F_{XTAL} x 4
1	1	0	5.3 to 10.6 MHz 1)	F_{XTAL} / 4	48	4	–	F_{XTAL} x 3
1	0	1	4 to 8 MHz	F_{XTAL} / 4	64	2	–	F_{XTAL} x 8
1	0	0	6.4 to 12 MHz 1)	F_{XTAL} / 4	40	2	–	F_{XTAL} x 5

Table 79. Multiplexed bus timings (continued)

Symbol		Parameter	F_{CPU} = 40 MHz TCL = 12.5 ns		Variable CPU Clock 1/2 TCL = 1 to 64 MHz		Unit
			min.	max.	min.	max.	
t_{39}	SR	Latched $\overline{CS}$ low to Valid Data In	–	16.5 + t_C + + 2t_A	–	3TCL – 21 + + t_C + 2t_A	ns
t_{40}	CC	Latched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	27 + t_F	–	3TCL – 10.5 + t_F	–	ns
t_{42}	CC	ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	7 + t_A	–	TCL – 5.5 + t_A	–	ns
t_{43}	CC	ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	– 5.5 + t_A	–	– 5.5 + t_A	–	ns
t_{44}	CC	Address float after $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	–	1.5	–	1.5	ns
t_{45}	CC	Address float after $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	–	14	–	TCL + 1.5	ns
t_{46}	SR	$\overline{RdCS}$ to Valid Data In (with RW delay)	–	4 + t_C	–	2TCL – 21 + t_C	ns
t_{47}	SR	$\overline{RdCS}$ to Valid Data In (no RW delay)	–	16.5 + t_C	–	3TCL – 21 + t_C	ns
t_{48}	CC	$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW delay)	15.5 + t_C	–	2TCL – 9.5 + t_C	–	ns
t_{49}	CC	$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW delay)	28 + t_C	–	3TCL – 9.5 + t_C	–	ns
t_{50}	CC	Data valid to $\overline{WrCS}$	10 + t_C	–	2TCL – 15 + t_C	–	ns
t_{51}	SR	Data hold after $\overline{RdCS}$	0	–	0	–	ns
t_{52}	SR	Data float after $\overline{RdCS}$	–	16.5 + t_F	–	2TCL – 8.5 + t_F	ns
t_{54}	CC	Address hold after $\overline{RdCS}$, $\overline{WrCS}$	6 + t_F	–	2TCL – 19 + t_F	–	ns
t_{56}	CC	Data hold after $\overline{WrCS}$	6 + t_F	–	2TCL – 19 + t_F	–	ns

Figure 60. External memory cycle: Demultiplexed bus, without r/w delay, extended ALE, r/w CS



27 Revision history

Table 87. Document revision history

Date	Revision	Changes
29-Jun-2006	1	Initial release on www.st.com
11-Jan-2008	2	ST10F272 replaced by ST10F272Z2 Added *Section 24: Known limitations on page 128* Modified example 1 in *Section 25.8.8: Voltage Controlled Oscillator on page 158* Modified *Section 26: Package information on page 185*: added information on ECOPACK specifications and modified figures and tables