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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M7 |
| Core Size | 32-Bit Single-Core |
| Speed | 216MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 168 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.7V ~ 3.6V |
| Data Converters | A/D 24x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 208-LQFP |
| Supplier Device Package | 208-LQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f765bgt6 |

disappear. The following conditions $V_{DDUSB}$ must be respected:

– During the power-on phase ($V_{DD} < V_{DD\_MIN}$), $V_{DDUSB}$ should be always lower than $V_{DD}$

– During the power-down phase ($V_{DD} < V_{DD\_MIN}$), $V_{DDUSB}$ should be always lower than $V_{DD}$

– The $V_{DDUSB}$ rising and falling time rate specifications must be respected (see *Table 20* and *Table 21*)

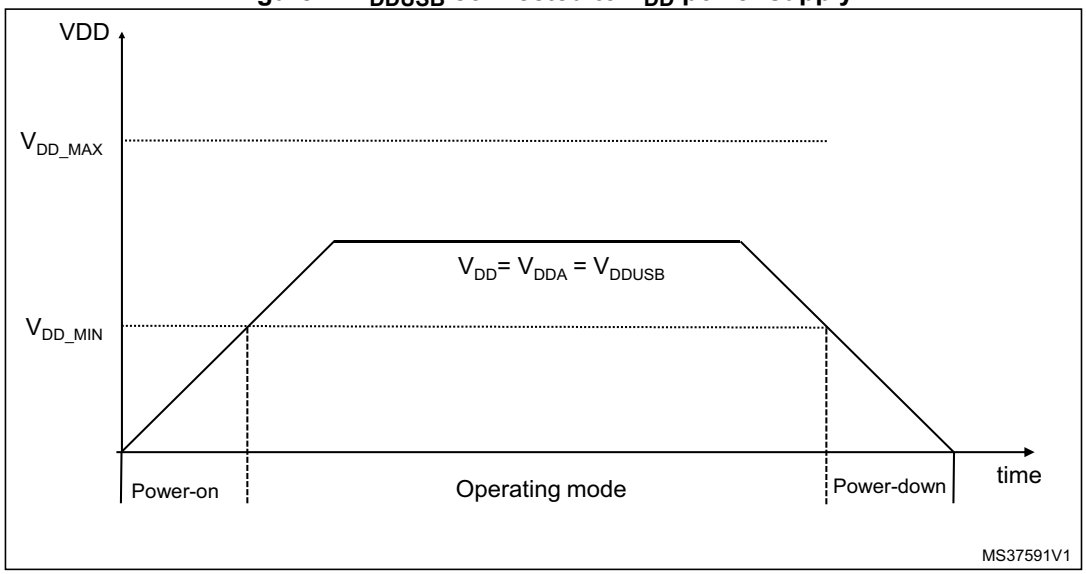
– In operating mode phase, $V_{DDUSB}$ could be lower or higher than $V_{DD}$:

  - If USB (USB OTG_HS/OTG_FS) is used, the associated GPIOs powered by $V_{DDUSB}$ are operating between $V_{DDUSB\_MIN}$ and $V_{DDUSB\_MAX}$.

  - The $V_{DDUSB}$ supply both USB transceiver (USB OTG_HS and USB OTG_FS). If only one USB transceiver is used in the application, the GPIOs associated to the other USB transceiver are still supplied by $V_{DDUSB}$.

  - If USB (USB OTG_HS/OTG_FS) is not used, the associated GPIOs powered by $V_{DDUSB}$ are operating between $V_{DD\_MIN}$ and $V_{DD\_MAX}$.

**Figure 4. $V_{DDUSB}$ connected to $V_{DD}$ power supply**



Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising or falling edge on one of the 6 WKUP pins (PA0, PA2, PC1, PC13, PI8, PI11), or an RTC alarm / wakeup / tamper /time stamp event occurs.

The Standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

## 2.22 $V_{BAT}$ operation

The $V_{BAT}$ pin allows to power the device $V_{BAT}$ domain from an external battery, an external supercapacitor, or from $V_{DD}$ when no external battery and an external supercapacitor are present.

$V_{BAT}$ operation is activated when $V_{DD}$ is not present.

The $V_{BAT}$ pin supplies the RTC, the backup registers and the backup SRAM.

*Note: When the microcontroller is supplied from $V_{BAT}$, external interrupts and RTC alarm/events do not exit it from $V_{BAT}$ operation.*

*When the PDR_ON pin is connected to $V_{SS}$ (Internal Reset OFF), the $V_{BAT}$ functionality is no more available and the $V_{BAT}$ pin should be connected to $V_{DD}$.*

## 2.23 Timers and watchdogs

The devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

*Table 6* compares the features of the advanced-control, general-purpose and basic timers.

**Table 6. Timer feature comparison**

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/ compare channels | Complementary output | Max interface clock (MHz) | Max timer clock (MHz)(1) |
|---|---|---|---|---|---|---|---|---|---|
| Advanced -control | TIM1, TIM8 | 16-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | Yes | 108 | 216 |
| General purpose | TIM2, TIM5 | 32-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No | 54 | 108/216 |
| | TIM3, TIM4 | 16-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No | 54 | 108/216 |
| | TIM9 | 16-bit | Up | Any integer between 1 and 65536 | No | 2 | No | 108 | 216 |
| | TIM10, TIM11 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No | 108 | 216 |
| | TIM12 | 16-bit | Up | Any integer between 1 and 65536 | No | 2 | No | 54 | 108/216 |
| | TIM13, TIM14 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No | 54 | 108/216 |
| Basic | TIM6, TIM7 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | No | 54 | 108/216 |

1. The maximum timer clock is either 108 or 216 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

## 2.24 Inter-integrated circuit interface ($I^2C$)

The devices embed 4 I2C. Refer to table *Table 7: I2C implementation* for the features implementation.

The $I^2C$ bus interface handles communications between the microcontroller and the serial $I^2C$ bus. It controls all $I^2C$ bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- $I^2C$-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

**Table 7. I2C implementation**

| I2C features(1) | I2C1 | I2C2 | I2C3 | I2C4 |
|---|---|---|---|---|
| Standard-mode (up to 100 kbit/s) | X | X | X | X |
| Fast-mode (up to 400 kbit/s) | X | X | X | X |
| Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s) | X | X | X | X |
| Programmable analog and digital noise filters | X | X | X | X |
| SMBus/PMBus hardware support | X | X | X | X |
| Independent clock | X | X | X | X |

1. X: supported.

## 2.33 Controller area network (bxCAN)

The three CANs are compliant with the 2.0A and B (active) specifications with a bit rate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated for CAN1 and CAN2. 512 bytes of SRAM are dedicated for CAN3.

## 2.34 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 1.28 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 1 bidirectional control endpoint + 5 IN endpoints + 5 OUT endpoints
- 12 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Battery Charging Specification Revision 1.2 support
- Internal FS OTG PHY support
- HNP/SNP/IP inside (no need for any external resistor)

For the OTG/Host modes, a power switch is needed in case bus-powered devices are connected

## 2.35 Universal serial bus on-the-go high-speed (OTG_HS)

The devices embed a USB OTG high-speed (up to 480 Mbit/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 Mbit/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 Mbit/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 4 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 8 bidirectional endpoints
- 16 host channels with periodic OUT support

**Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)**

| Pin Number | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32F765xx STM32F767xx | | | | | | STM32F768Ax STM32F769xx | | | | | | | | | |
| LQFP100 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | WLCSP180[1] | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| 3 | 3 | B1 | 3 | 3 | A1 | C12 | 3 | 3 | A1 | PE4 | I/O | FT | - | TRACED1, SPI4_NSS, SAI1_FS_A, DFSDM1_DATIN3, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT | - |
| 4 | 4 | B2 | 4 | 4 | B1 | D12 | 4 | 4 | B1 | PE5 | I/O | FT | - | TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, DFSDM1_CKIN3, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT | - |
| 5 | 5 | B3 | 5 | 5 | B2 | E11 | 5 | 5 | B2 | PE6 | I/O | FT | - | TRACED3, TIM1_BKIN2, TIM9_CH2, SPI4_MOSI, SAI1_SD_A, SAI2_MCLK_B, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT | - |
| - | - | - | - | - | G6 | - | - | - | G6 | VSS | S | - | - | - | - |
| - | - | - | - | - | F5 | - | - | - | F5 | VDD | S | - | - | - | - |
| 6 | 6 | C1 | 6 | 6 | C1 | C13 | 6 | 6 | C1 | VBAT | S | - | - | - | - |
| - | - | D2 | 7 | 7 | C2 | NC | 7 | 7 | C2 | PI8 | I/O | FT | (2) | EVENTOUT | RTC_TAMP2/RTC_TS/ WKUP5 |
| 7 | 7 | D1 | 8 | 8 | D1 | D13 | 8 | 8 | D1 | PC13 | I/O | FT | (2) | EVENTOUT | RTC_TAMP1/RTC_TS/ RTC_OUT/ WKUP4 |
| 8 | 8 | E1 | 9 | 9 | E1 | E12 | 9 | 9 | E1 | PC14-OSC32_IN | I/O | FT | (2) (3) | EVENTOUT | OSC32_IN |
| 9 | 9 | F1 | 10 | 10 | F1 | E13 | 10 | 10 | F1 | PC15-OSC32_OUT | I/O | FT | (2) (3) | EVENTOUT | OSC32_OUT |
| - | - | - | - | - | G5 | - | - | - | G5 | VDD | S | - | - | - | - |

**Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)**

| Pin Number | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32F765xx STM32F767xx | | | | | | STM32F768Ax STM32F769xx | | | | | | | | | |
| LQFP100 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | WLCSP180[1] | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| 47 | 70 | R13 | 80 | 91 | R13 | L5 | 80 | 91 | R13 | PB11 | I/O | FT | - | TIM2_CH4, I2C2_SDA, DFSDM1_CKIN7, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_RMII_TX_EN, DSI_TE, LCD_G5, EVENTOUT | - |
| 48 | 71 | M10 | 81 | 92 | L11 | P5 | 81 | 92 | L11 | VCAP_1 | S | - | - | - | - |
| 49 | - | - | - | 93 | K9 | N5 | - | 93 | K9 | VSS | S | - | - | - | - |
| 50 | 72 | N10 | 82 | 94 | L10 | P4 | 82 | 94 | L10 | VDD | S | - | - | - | - |
| - | - | - | - | 95 | M14 | NC | - | 95 | M14 | PJ5 | I/O | FT | - | LCD_R6, EVENTOUT | - |
| - | - | M11 | 83 | 96 | P13 | NC | 83 | 96 | P13 | PH6 | I/O | FT | - | I2C2_SMBA, SPI5_SCK, TIM12_CH1, ETH_MII_RXD2, FMC_SDNE1, DCMI_D8, EVENTOUT | - |
| - | - | N12 | 84 | 97 | N13 | NC | 84 | 97 | N13 | PH7 | I/O | FT | - | I2C3_SCL, SPI5_MISO, ETH_MII_RXD3, FMC_SDCKE1, DCMI_D9, EVENTOUT | - |
| - | - | M12 | 85 | 98 | P14 | M5 | - | 98 | P14 | PH8 | I/O | FT | - | I2C3_SDA, FMC_D16, DCMI_HSYNC, LCD_R2, EVENTOUT | - |
| - | - | M13 | 86 | 99 | N14 | K4 | - | 99 | N14 | PH9 | I/O | FT | - | I2C3_SMBA, TIM12_CH2, FMC_D17, DCMI_D0, LCD_R3, EVENTOUT | - |
| - | - | L13 | 87 | 100 | P15 | L4 | - | 100 | P15 | PH10 | I/O | FT | - | TIM5_CH1, I2C4_SMBA, FMC_D18, DCMI_D1, LCD_R4, EVENTOUT | - |
| - | - | L12 | 88 | 101 | N15 | M4 | - | 101 | N15 | PH11 | I/O | FT | - | TIM5_CH2, I2C4_SCL, FMC_D19, DCMI_D2, LCD_R5, EVENTOUT | - |

**Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)**

| Pin Number | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32F765xx STM32F767xx | | | | | | STM32F768Ax STM32F769xx | | | | | | | | | |
| LQFP100 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | WLCSP180[1] | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| - | - | C13 | 134 | 157 | C13 | D3 | 134 | 157 | C13 | PI3 | I/O | FT | - | TIM8_ETR, SPI2_MOSI/I2S2_SD, FMC_D27, DCMI_D10, EVENTOUT | - |
| - | - | D9 | 135 | - | F9 | - | 135 | - | F9 | VSS | S | - | - | - | |
| - | - | C9 | 136 | 158 | E10 | - | 136 | 158 | E10 | VDD | S | - | - | - | -- |
| 76 | 109 | A14 | 137 | 159 | A14 | A3 | 137 | 159 | A14 | PA14(JTCK-SWCLK) | I/O | FT | - | JTCK-SWCLK, EVENTOUT | - |
| 77 | 110 | A13 | 138 | 160 | A13 | F8 | 138 | 160 | A13 | PA15(JTDI) | I/O | FT | - | JTDI, TIM2_CH1/TIM2_ETR, HDMI_CEC, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SPI6_NSS, UART4_RTS, CAN3_TX, UART7_TX, EVENTOUT | - |
| 78 | 111 | B14 | 139 | 161 | B14 | B4 | 139 | 161 | B14 | PC10 | I/O | FT | - | DFSDM1_CKIN5, SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDMMC1_D2, DCMI_D8, LCD_R2, EVENTOUT | - |
| 79 | 112 | B13 | 140 | 162 | B13 | C4 | 140 | 162 | B13 | PC11 | I/O | FT | - | DFSDM1_DATIN5, SPI3_MISO, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SDMMC1_D3, DCMI_D4, EVENTOUT | - |
| 80 | 113 | A12 | 141 | 163 | A12 | D4 | 141 | 163 | A12 | PC12 | I/O | FT | - | TRACED3, SPI3_MOSI/I2S3_SD, USART3_CK, UART5_TX, SDMMC1_CK, DCMI_D9, EVENTOUT | - |

**Table 12. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1/DFSDM1/CEC | I2C1/2/3/4/USART1/CEC | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF | CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD | SAI2/QUADSPI/SDMMC2/DFSDM1/OTG2_HS/OTG1_FS/LCD | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMMC1/MDIOS/OTG2_FS | DCMI/LCD/DSI | LCD | SYS |
| Port E | PE4 | TRACED1 | - | - | - | - | SPI4_NSS | SAI1_FS_A | - | - | - | DFSDM1_DATAIN3 | - | FMC_A20 | DCMI_D4 | LCD_B0 | EVENTOUT |
| | PE5 | TRACED2 | - | - | TIM9_CH1 | - | SPI4_MISO | SAI1_SCK_A | - | - | - | DFSDM1_CKIN3 | - | FMC_A21 | DCMI_D6 | LCD_G0 | EVENTOUT |
| | PE6 | TRACED3 | TIM1_BKIN2 | - | TIM9_CH2 | - | SPI4_MOSI | SAI1_SD_A | - | - | - | SAI2_MCK_B | - | FMC_A22 | DCMI_D7 | LCD_G1 | EVENTOUT |
| | PE7 | - | TIM1_ETR | - | - | - | - | DFSDM1_DATAIN2 | - | UART7_Rx | - | QUADSPI_BK2_IO0 | - | FMC_D4 | - | - | EVENTOUT |
| | PE8 | - | TIM1_CH1N | - | - | - | - | DFSDM1_CKIN2 | - | UART7_Tx | - | QUADSPI_BK2_IO1 | - | FMC_D5 | - | - | EVENTOUT |
| | PE9 | - | TIM1_CH1 | - | - | - | - | DFSDM1_CKOUT | - | UART7_RTS | - | QUADSPI_BK2_IO2 | - | FMC_D6 | - | - | EVENTOUT |
| | PE10 | - | TIM1_CH2N | - | - | - | - | DFSDM1_DATAIN4 | - | UART7_CTS | - | QUADSPI_BK2_IO3 | - | FMC_D7 | - | - | EVENTOUT |
| | PE11 | - | TIM1_CH2 | - | - | - | SPI4_NSS | DFSDM1_CKIN4 | - | - | - | SAI2_SD_B | - | FMC_D8 | - | LCD_G3 | EVENTOUT |
| | PE12 | - | TIM1_CH3N | - | - | - | SPI4_SCK | DFSDM1_DATAIN5 | - | - | - | SAI2_SCK_B | - | FMC_D9 | - | LCD_B4 | EVENTOUT |
| | PE13 | - | TIM1_CH3 | - | - | - | SPI4_MISO | DFSDM1_CKIN5 | - | - | - | SAI2_FS_B | - | FMC_D10 | - | LCD_DE | EVENTOUT |
| | PE14 | - | TIM1_CH4 | - | - | - | SPI4_MOSI | - | - | - | - | SAI2_MCK_B | - | FMC_D11 | - | LCD_CLK | EVENTOUT |
| | PE15 | - | TIM1_BKIN | - | - | - | - | - | - | - | - | - | - | FMC_D12 | - | LCD_R7 | EVENTOUT |

# 5 Electrical characteristics

## 5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to $V_{SS}$.

### 5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$ = 25 °C and $T_A$ = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

### 5.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD}$ = 3.3 V (for the 1.7 V ≤ $V_{DD}$ ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

### 5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 22*.

### 5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 23*.

**Figure 22. Pin loading conditions**

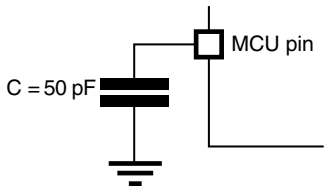
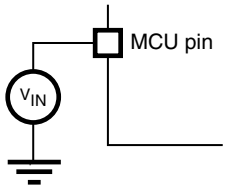


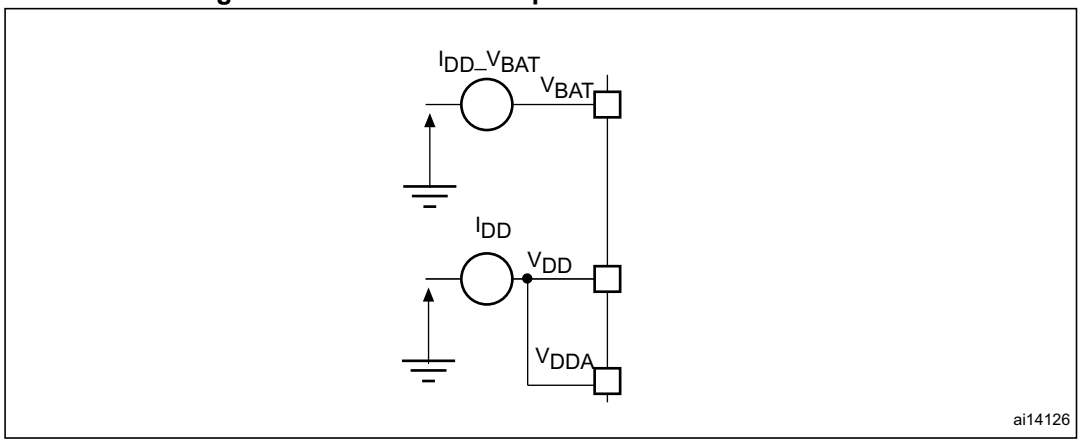

**Figure 23. Pin input voltage**



**Caution:** Each power supply pair ($V_{DD}/V_{SS}$, $V_{DDA}/V_{SSA}$ ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

### 5.1.7 Current consumption measurement

**Figure 26. Current consumption measurement scheme**




## 5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 14: Voltage characteristics*, *Table 15: Current characteristics*, and *Table 16: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. The device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard. Extended mission profiles are available on demand.

**Table 14. Voltage characteristics**

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$–$V_{SS}$ | External main supply voltage (including $V_{DDA}$, $V_{DD}$, $V_{BAT}$, $V_{DDUSB}$, $V_{DDDSI}$ (1) and $V_{DDSDMMC}$)(2) | − 0.3 | 4.0 | V |
| $V_{IN}$ | Input voltage on FT pins(3) | $V_{SS}$ − 0.3 | $V_{DD}$+4.0 | |
| | Input voltage on TTa pins | $V_{SS}$ − 0.3 | 4.0 | |
| | Input voltage on any other pin | $V_{SS}$ − 0.3 | 4.0 | |
| | Input voltage on BOOT pin | $V_{SS}$ | 9.0 | |
| $\lvert\Delta V_{DDx}\rvert$ | Variations between different $V_{DD}$ power pins | - | 50 | mV |
| $\lvert V_{SSX} - V_{SS}\rvert$ | Variations between all the different ground pins(4) | - | 50 | |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see *Section 5.3.18: Absolute maximum ratings (electrical sensitivity)* | | - |

# 5.3 Operating conditions

## 5.3.1 General operating conditions

**Table 17. General operating conditions**

| Symbol | Parameter | Conditions[1] | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | Power Scale 3 (VOS[1:0] bits in PWR_CR register = 0x01), Regulator ON, over-drive OFF | | 0 | - | 144 | MHz |
| | | Power Scale 2 (VOS[1:0] bits in PWR_CR register = 0x10), Regulator ON | Over-drive OFF | 0 | - | 168 | |
| | | | Over-drive ON | | - | 180 | |
| | | Power Scale 1 (VOS[1:0] bits in PWR_CR register= 0x11), Regulator ON | Over-drive OFF | 0 | - | 180 | |
| | | | Over-drive ON | | - | 216[2] | |
| $f_{PCLK1}$ | Internal APB1 clock frequency | Over-drive OFF | | 0 | - | 45 | |
| | | Over-drive ON | | 0 | - | 54 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | Over-drive OFF | | 0 | - | 90 | |
| | | Over-drive ON | | 0 | - | 108 | |
| $V_{DD}$ | Standard operating voltage | - | | 1.7[3] | - | 3.6 | V |
| $V_{DDA}$[4][5] | Analog operating voltage (ADC limited to 1.2 M samples) | Must be the same potential as $V_{DD}$[6] | | 1.7[3] | - | 2.4 | |
| | Analog operating voltage (ADC limited to 2.4 M samples) | | | 2.4 | - | 3.6 | |
| $V_{DDUSB}$ | USB supply voltage (supply voltage for PA11,PA12, PB14 and PB15 pins) | USB not used | | 1.7 | 3.3 | 3.6 | |
| | | USB used | | 3.0 | - | 3.6 | |
| $V_{BAT}$ | Backup operating voltage | - | | 1.65 | - | 3.6 | |
| $V_{DDSDMMC}$ | SDMMC2 supply voltage (supply voltage for PG[12:9] and PD6 pins) | It can be different from VDD | | 1.7 | - | 3.6 | |
| $V_{DDDSI}$ | DSI system operating | - | | 1.7 | - | 3.6 | |

1. Guaranteed by design.
2. The reset temporization is measured from the power-on (POR reset or wakeup from $V_{BAT}$) to the instant when first instruction is read by the user application code.

### 5.3.6 Over-drive switching characteristics

When the over-drive mode switches from enabled to disabled or disabled to enabled, the system clock is stalled during the internal voltage set-up.

The over-drive switching characteristics are given in *Table 23*. They are subject to general operating conditions for $T_A$.

**Table 23. Over-drive switching characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Tod_swen | Over_drive switch enable time | HSI | - | 45 | - | µs |
| | | HSE max for 4 MHz and min for 26 MHz | 45 | - | 100 | |
| | | External HSE 50 MHz | - | 40 | - | |
| Tod_swdis | Over_drive switch disable time | HSI | - | 20 | - | |
| | | HSE max for 4 MHz and min for 26 MHz. | 20 | - | 80 | |
| | | External HSE 50 MHz | - | 15 | - | |

1. Guaranteed by design.

### 5.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 26: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

**Table 33. Typical and maximum current consumption in Sleep mode, regulator ON**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Sleep mode | All peripherals enabled(2) | 216 | 128 | 144(3) | 190(3) | - | mA |
| | | | 200 | 119 | 134 | 180 | 214 | |
| | | | 180 | 105 | 118(3) | 153(3) | 178(3) | |
| | | | 168 | 93 | 105 | 136 | 156 | |
| | | | 144 | 72 | 80 | 107 | 124 | |
| | | | 60 | 33 | 39 | 65 | 82 | |
| | | | 25 | 17 | 21 | 47 | 65 | |
| | | All peripherals disabled | 216 | 18 | 25(3) | 71(3) | - | |
| | | | 200 | 17 | 24 | 70 | 112 | |
| | | | 180 | 14 | 20(3) | 54(3) | 75(3) | |
| | | | 168 | 13 | 18 | 49 | 69 | |
| | | | 144 | 10 | 14 | 40 | 58 | |
| | | | 60 | 6 | 10 | 36 | 53 | |
| | | | 25 | 4 | 8 | 34 | 51 | |

1. Guaranteed by characterization results, unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. Guaranteed by test in production.

## 5.3.10 Internal clock source characteristics

The parameters given in *Table 45* and *Table 46* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 17*.

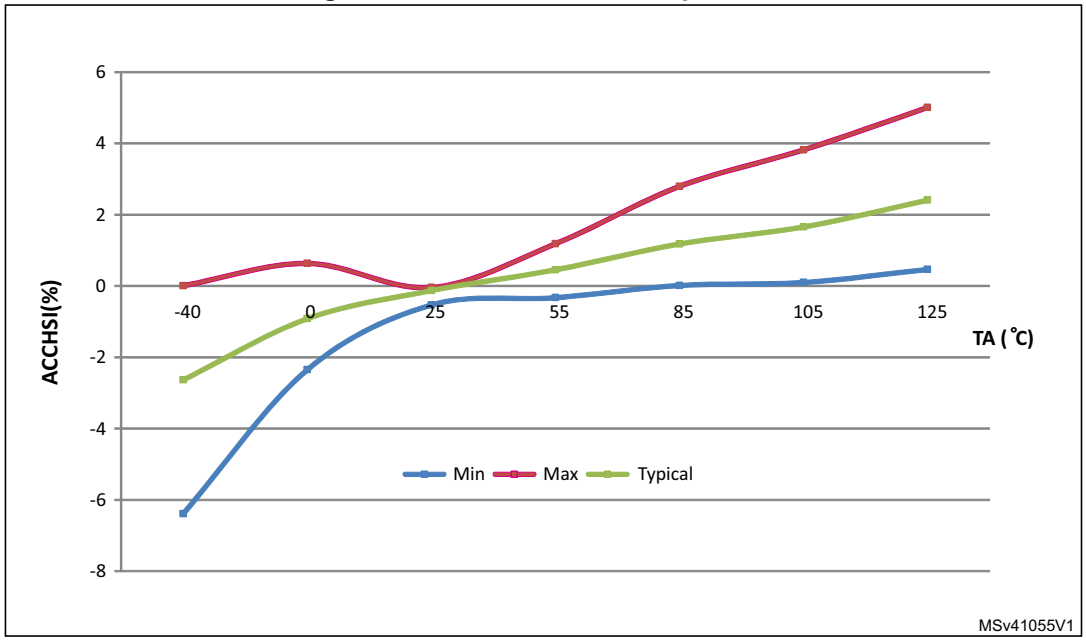
### High-speed internal (HSI) RC oscillator

**Table 45. HSI oscillator characteristics (1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | - | - | 16 | - | MHz |
| $ACC_{HSI}$ | HSI user trimming step(2) | - | - | - | 1 | % |
| | Accuracy of the HSI oscillator | $T_A$ = –40 to 105 °C(3) | − 8 | - | 4.5 | % |
| | | $T_A$ = –10 to 85 °C(3) | − 4 | - | 4 | % |
| | | $T_A$ = 25 °C(4) | − 1 | - | 1 | % |
| $t_{su(HSI)}$(2) | HSI oscillator startup time | - | - | 2.2 | 4 | µs |
| $I_{DD(HSI)}$(2) | HSI oscillator power consumption | - | - | 60 | 80 | µA |

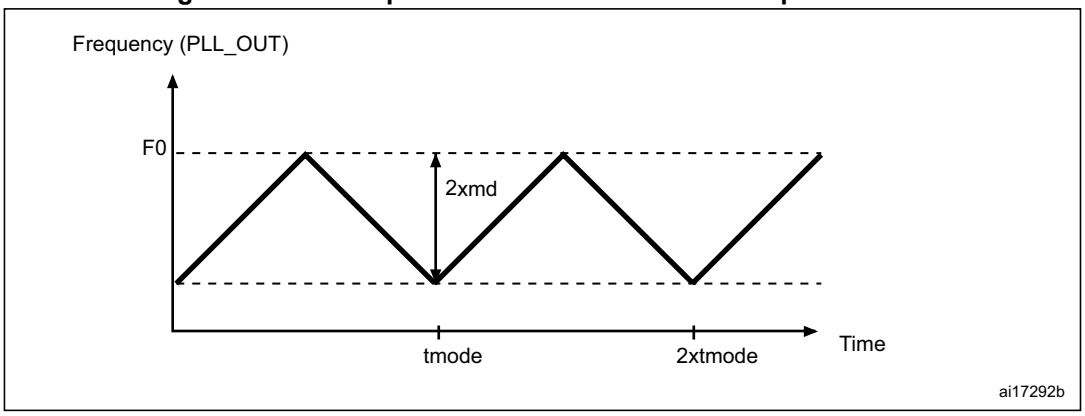
1. $V_{DD}$ = 3.3 V, $T_A$ = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Factory calibrated, parts not soldered.

**Figure 32. ACCHSI versus temperature**




1. Guaranteed by characterization results.

**Figure 35. PLL output clock waveforms in down spread mode**




## 5.3.13 MIPI D-PHY characteristics

The parameters given in *Table 51* and *Table 52* are derived from tests performed under temperature and $V_{DD}$ supply voltage conditions summarized in *Table 17*.

**Table 51. MIPI D-PHY characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Hi-Speed Input/Output Characteristics | | | | | | |
| $U_{INST}$ | UI instantaneous | - | 2 | - | 12.5 | ns |
| $V_{CMTX}$ | HS transmit common mode voltage | - | 150 | 200 | 250 | mV |
| $\|\Delta V_{CMTX}\|$ | $V_{CMTX}$ mismatch when output is Differential-1 or Differential-0 | - | - | - | 5 | |
| $\|V_{OD}\|$ | HS transmit differential voltage | - | 140 | 200 | 270 | |
| $\|\Delta V_{OD}\|$ | $V_{OD}$ mismatch when output is Differential-1 or Differential-0 | - | - | - | 14 | |
| $V_{OHHS}$ | HS output high voltage | - | - | - | 360 | |
| $Z_{OS}$ | Single ended output impedance | - | 40 | 50 | 62.5 | Ω |
| $\Delta Z_{OS}$ | Single ended output impedance mismatch | - | - | - | 10 | % |
| $t_{HSr}$ & $t_{HSf}$ | 20%-80% rise and fall time | - | 100 | - | 0.35*UI | ps |
| LP Receiver Input Characteristics | | | | | | |
| $V_{IL}$ | Logic 0 input voltage (not in ULP State) | - | - | - | 550 | mV |
| $V_{IL-ULPS}$ | Logic 0 input voltage in ULP State | - | - | - | 300 | |
| $V_{IH}$ | Input high level voltage | - | 880 | - | - | |
| $V_{hys}$ | Voltage hysteresis | - | 25 | - | - | |
| LP Emitter Output Characteristics | | | | | | |

**Table 66. Output voltage characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$(1) | Output low level voltage for an I/O pin | CMOS port(2) $I_{IO}$ = +8 mA 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | - | 0.4 | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin except PC14 | CMOS port(2) $I_{IO}$ = -8 mA 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | $V_{DD}$ − 0.4 | - | |
| $V_{OH}$(3) | Output high level voltage for PC14 | CMOS port(2) $I_{IO}$ = -2 mA 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | $V_{DD}$ − 0.4 | | |
| $V_{OL}$ (1) | Output low level voltage for an I/O pin | TTL port(2) $I_{IO}$ =+8mA 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | - | 0.4 | V |
| $V_{OH}$ (3) | Output high level voltage for an I/O pin except PC14 | TTL port(2) $I_{IO}$ =-8mA 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 2.4 | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin | $I_{IO}$ = +20 mA 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | - | 1.3(4) | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin except PC14 | $I_{IO}$ = -20 mA 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | $V_{DD}$−1.3(4) | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin | $I_{IO}$ = +6 mA 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | - | 0.4(4) | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin except PC14 | $I_{IO}$ = -6 mA 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | $V_{DD}$−0.4(4) | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin | $I_{IO}$ = +4 mA 1.7 V ≤ $V_{DD}$ ≤ 3.6V | - | 0.4(5) | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin except PC14 | $I_{IO}$ = -4 mA 1.7 V ≤ $V_{DD}$ ≤ 3.6V | $V_{DD}$−0.4(5) | - | |
| $V_{OH}$(3) | Output high level voltage for PC14 | $I_{IO}$ = -1 mA 1.7 V ≤ $V_{DD}$ ≤ 3.6V | $V_{DD}$−0.4(5) | - | |

1. The $I_{IO}$ current sunk by the device must always respect the absolute maximum rating specified in *Table 15*. and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The $I_{IO}$ current sourced by the device must always respect the absolute maximum rating specified in *Table 15* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VDD}$.
4. Based on characterization data.
5. Guaranteed by design.

### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 39* and *Table 67*, respectively.

**Table 74. ADC static accuracy at $f_{ADC}$ = 36 MHz**

| Symbol | Parameter | Test conditions | Typ | Max(1) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{ADC}$ =36 MHz, $V_{DDA}$ = 2.4 to 3.6 V, $V_{REF}$ = 1.7 to 3.6 V $V_{DDA} - V_{REF} < 1.2$ V | ±4 | ±7 | LSB |
| EO | Offset error | | ±2 | ±3 | |
| EG | Gain error | | ±3 | ±6 | |
| ED | Differential linearity error | | ±2 | ±3 | |
| EL | Integral linearity error | | ±3 | ±6 | |

1. Guaranteed by characterization results.

**Table 75. ADC dynamic accuracy at $f_{ADC}$ = 18 MHz - limited test conditions(1)**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ENOB | Effective number of bits | $f_{ADC}$ =18 MHz $V_{DDA} = V_{REF+}$= 1.7 V Input Frequency = 20 KHz Temperature = 25 °C | 10.3 | 10.4 | - | bits |
| SINAD | Signal-to-noise and distortion ratio | | 64 | 64.2 | - | dB |
| SNR | Signal-to-noise ratio | | 64 | 65 | - | |
| THD | Total harmonic distortion | | − 67 | − 72 | - | |

1. Guaranteed by characterization results.

**Table 76. ADC dynamic accuracy at $f_{ADC}$ = 36 MHz - limited test conditions(1)**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ENOB | Effective number of bits | $f_{ADC}$ =36 MHz $V_{DDA} = V_{REF+}$ = 3.3 V Input Frequency = 20 KHz Temperature = 25 °C | 10.6 | 10.8 | - | bits |
| SINAD | Signal-to noise and distortion ratio | | 66 | 67 | - | dB |
| SNR | Signal-to noise ratio | | 64 | 68 | - | |
| THD | Total harmonic distortion | | − 70 | − 72 | - | |

1. Guaranteed by characterization results.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.20* does not affect the ADC accuracy.

**Table 104. Asynchronous multiplexed PSRAM/NOR read timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $3T_{HCLK} - 1$ | $3T_{HCLK} + 1$ | ns |
| $t_{v(NOE\_NE)}$ | FMC_NEx low to FMC_NOE low | $2T_{HCLK}$ | $2T_{HCLK} + 0.5$ | |
| $t_{tw(NOE)}$ | FMC_NOE low time | $T_{HCLK} - 1$ | $T_{HCLK} + 1$ | |
| $t_{h(NE\_NOE)}$ | FMC_NOE high to FMC_NE high hold time | 0 | - | |
| $t_{v(A\_NE)}$ | FMC_NEx low to FMC_A valid | - | 0.5 | |
| $t_{v(NADV\_NE)}$ | FMC_NEx low to FMC_NADV low | 0 | 0.5 | |
| $t_{w(NADV)}$ | FMC_NADV low time | $T_{HCLK} - 0.5$ | $T_{HCLK}+1$ | |
| $t_{h(AD\_NADV)}$ | FMC_AD(address) valid hold time after FMC_NADV high) | $T_{HCLK} + 0.5$ | - | |
| $t_{h(A\_NOE)}$ | Address hold time after FMC_NOE high | $T_{HCLK} - 0.5$ | - | |
| $t_{h(BL\_NOE)}$ | FMC_BL time after FMC_NOE high | 0 | - | |
| $t_{v(BL\_NE)}$ | FMC_NEx low to FMC_BL valid | - | 0.5 | |
| $t_{su(Data\_NE)}$ | Data to FMC_NEx high setup time | $T_{HCLK} - 1$ | - | |
| $t_{su(Data\_NOE)}$ | Data to FMC_NOE high setup time | $T_{HCLK} - 1$ | - | |
| $t_{h(Data\_NE)}$ | Data hold time after FMC_NEx high | 0 | - | |
| $t_{h(Data\_NOE)}$ | Data hold time after FMC_NOE high | 0 | - | |

1. Guaranteed by characterization results.

**Table 105. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $8T_{HCLK} - 1$ | $8T_{HCLK} + 1$ | ns |
| $t_{w(NOE)}$ | FMC_NWE low time | $5T_{HCLK} - 1.5$ | $5T_{HCLK} + 0.5$ | |
| $t_{su(NWAIT\_NE)}$ | FMC_NWAIT valid before FMC_NEx high | $5T_{HCLK} + 1.5$ | - | |
| $t_{h(NE\_NWAIT)}$ | FMC_NEx hold time after FMC_NWAIT invalid | $4T_{HCLK}+ 1$ | - | |

1. Guaranteed by characterization results.

**Figure 99. UFBGA176+25, 10 x 10 mm x 0.65 mm, ultra fine-pitch ball grid array package recommended footprint**

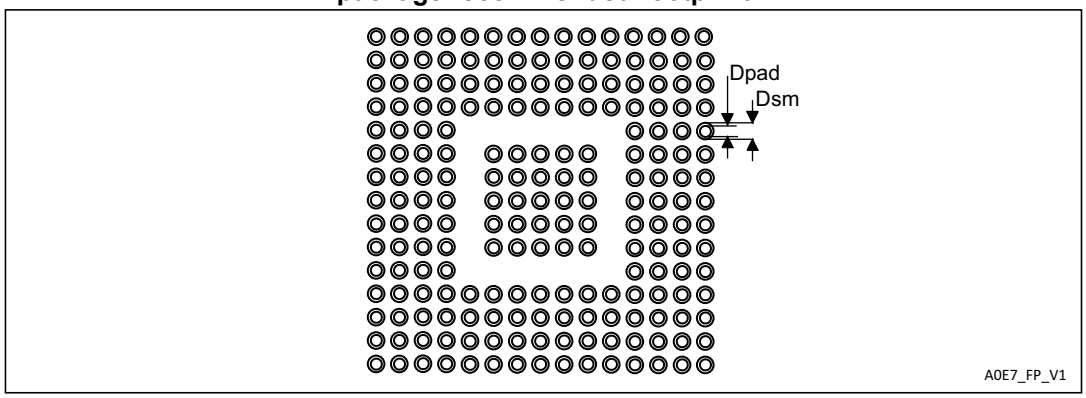



**Table 132. UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA)**

| Dimension | Recommended values |
|---|---|
| Pitch | 0.65 mm |
| Dpad | 0.300 mm |
| Dsm | 0.400 mm typ. (depends on the soldermask registration tolerance) |
| Stencil opening | 0.300 mm |
| Stencil thickness | Between 0.100 mm and 0.125 mm |
| Pad trace width | 0.100 mm |