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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	168
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f765bit6

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2.13 JPEG codec (JPEG)

The JPEG codec provides an fast and simple hardware compressor and decompressor of JPEG images with full management of JPEG headers.

The JPEG codec main features:

- 8-bit/channel pixel depths
- Single clock per pixel encoding and decoding
- Support for JPEG header generation and parsing
- Up to four programmable quantization tables
- Fully programmable Huffman tables (two AC and two DC)
- Fully programmable minimum coded unit (MCU)
- Encode/decode support (non simultaneous)
- Single clock Huffman coding and decoding
- Two-channel interface: Pixel/Compress In, Pixel/Compressed Out
- Stallable design
- Support for single, greyscale component
- Functionality to enable/disable header processing
- Internal register interface
- Fully synchronous design
- Configured for high-speed decode mode

2.14 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 25 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 168 GPIOs can be connected to the 16 external interrupt lines.

2.15 Clocks and startup

On reset the 16 MHz internal HSI RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 216 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the two AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the two AHB buses is 216 MHz while the maximum frequency of the high-speed APB domains is 108 MHz. The maximum allowed frequency of the low-speed APB domain is 54 MHz.

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	-	D3	11	11	E4	G10	11	11	E4	PI9	I/O	FT	-	UART4_RX, CAN1_RX, FMC_D30, LCD_VSYNC, EVENTOUT	-
-	-	E3	12	12	D5	H10	12	12	D5	PI10	I/O	FT	-	ETH_MII_RX_ER, FMC_D31, LCD_HSYNC, EVENTOUT	-
-	-	E4	13	13	F3	F11	13	13	F3	PI11	I/O	FT	-	LCD_G6, OTG_HS_ULPI_DIR, EVENTOUT	WKUP6
-	-	F2	14	14	F2	F13	14	14	F2	VSS	S	-	-	-	-
-	-	F3	15	15	F4	F12	15	15	F4	VDD	S	-	-	-	-
-	10	E2	16	16	D2	G11	16	16	D2	PF0	I/O	FT	-	I2C2_SDA, FMC_A0, EVENTOUT	-
-	11	H3	17	17	E2	G12	17	17	E2	PF1	I/O	FT	-	I2C2_SCL, FMC_A1, EVENTOUT	-
-	12	H2	18	18	G2	G13	18	18	G2	PF2	I/O	FT	-	I2C2_SMBA, FMC_A2, EVENTOUT	-
-	-	-	-	19	E3	NC	-	19	E3	PI12	I/O	FT	-	LCD_HSYNC, EVENTOUT	-
-	-	-	-	20	G3	NC	-	20	G3	PI13	I/O	FT	-	LCD_VSYNC, EVENTOUT	-
-	-	-	-	21	H3	NC	-	21	H3	PI14	I/O	FT	-	LCD_CLK, EVENTOUT	-
-	13	J2	19	22	H2	H11	19	22	H2	PF3	I/O	FT	-	FMC_A3, EVENTOUT	ADC3_IN9
-	14	J3	20	23	J2	H12	20	23	J2	PF4	I/O	FT	-	FMC_A4, EVENTOUT	ADC3_IN14
-	15	K3	21	24	K3	H13	21	24	K3	PF5	I/O	FT	-	FMC_A5, EVENTOUT	ADC3_IN15
10	16	G2	22	25	H6	J13	22	25	H6	VSS	S	-	-	-	-
11	17	G3	23	26	H5	J12	23	26	H5	VDD	S	-	-	-	-
-	18	K2	24	27	K2	NC	24	27	K2	PF6	I/O	FT	-	TIM10_CH1, SPI5_NSS, SAI1_SD_B, UART7_RX, QUADSPI_BK1_IO3, EVENTOUT	ADC3_IN4

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	-	-	-	60	L6	-	-	60	L6	VSS	S	-	-	-	-
34	46	R5	56	61	R5	P10	56	61	R5	PB0	I/O	FT	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, DFSDM1_CKOUT, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, LCD_G1, EVENTOUT	ADC1_IN8, ADC2_IN8
35	47	R4	57	62	R4	J8	57	62	R4	PB1	I/O	FT	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN1, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, LCD_G0, EVENTOUT	ADC1_IN9, ADC2_IN9
36	48	M6	58	63	M5	J7	58	63	M5	PB2	I/O	FT	-	SAI1_SD_A, SPI3_MOSI/I2S3_SD, QUADSPI_CLK, DFSDM1_CKIN1, EVENTOUT	-
-	-	-	-	64	G4	NC	-	64	G4	PI15	I/O	FT	-	LCD_G2, LCD_R0, EVENTOUT	-
-	-	-	-	65	R6	NC	-	65	R6	PJ0	I/O	FT	-	LCD_R7, LCD_R1, EVENTOUT	-
-	-	-	-	66	R7	NC	-	66	R7	PJ1	I/O	FT	-	LCD_R2, EVENTOUT	-
-	-	-	-	67	P7	NC	-	67	P7	PJ2	I/O	FT	-	DSI_TE, LCD_R3, EVENTOUT	-
-	-	-	-	68	N8	NC	-	68	N8	PJ3	I/O	FT	-	LCD_R4, EVENTOUT	-
-	-	-	-	69	M9	NC	-	69	M9	PJ4	I/O	FT	-	LCD_R5, EVENTOUT	-
-	49	R6	59	70	P8	N9	59	70	P8	PF11	I/O	FT	-	SPI5_MOSI, SAI2_SD_B, FMC_SDNRAS, DCMI_D12, EVENTOUT	-
-	50	P6	60	71	M6	K7	60	71	M6	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-

Table 12. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM1/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port D	PD8	-	-	-	DFSDM1_CKIN3	-	-	-	USART3_TX	SPDIF_RX1	-	-	-	FMC_D13	-	-	EVENTOUT
	PD9	-	-	-	DFSDM1_DATAIN3	-	-	-	USART3_RX	-	-	-	-	FMC_D14	-	-	EVENTOUT
	PD10	-	-	-	DFSDM1_CKOUT	-	-	-	USART3_CK	-	-	-	-	FMC_D15	-	LCD_B3	EVENTOUT
	PD11	-	-	-	-	I2C4_SMBA	-	-	USART3_CTS	-	QUADSPI_BK1_IO0	SAI2_SD_A	-	FMC_A16/FMC_CLE	-	-	EVENTOUT
	PD12	-	-	TIM4_CH1	LPTIM1_IN1	I2C4_SCL	-	-	USART3_RTS	-	QUADSPI_BK1_IO1	SAI2_FS_A	-	FMC_A17/FMC_ALE	-	-	EVENTOUT
	PD13	-	-	TIM4_CH2	LPTIM1_OUT	I2C4_SDA	-	-	-	-	QUADSPI_BK1_IO3	SAI2_SCK_A	-	FMC_A18	-	-	EVENTOUT
	PD14	-	-	TIM4_CH3	-	-	-	-	-	UART8_CTS	-	-	-	FMC_D0	-	-	EVENTOUT
	PD15	-	-	TIM4_CH4	-	-	-	-	-	UART8_RTS	-	-	-	FMC_D1	-	-	EVENTOUT
Port E	PE0	-	-	TIM4_ETR	LPTIM1_ETR	-	-	-	-	UART8_Rx	-	SAI2_MCK_A	-	FMC_NBL0	DCMI_D2	-	EVENTOUT
	PE1	-	-	-	LPTIM1_IN2	-	-	-	-	UART8_Tx	-	-	-	FMC_NBL1	DCMI_D3	-	EVENTOUT
	PE2	TRACECLK	-	-	-	-	SPI4_SCK	SAI1_MCLK_A	-	-	QUADSPI_BK1_IO2	-	ETH_MII_TXD3	FMC_A23	-	-	EVENTOUT
	PE3	TRACED0	-	-	-	-	-	SAI1_SD_B	-	-	-	-	-	FMC_A19	-	-	EVENTOUT

7. The over-drive mode is not supported when the internal regulator is OFF.
8. To sustain a voltage higher than VDD+0.3, the internal Pull-up and Pull-Down resistors must be disabled
9. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
10. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

Table 18. Limitations depending on the operating power supply range

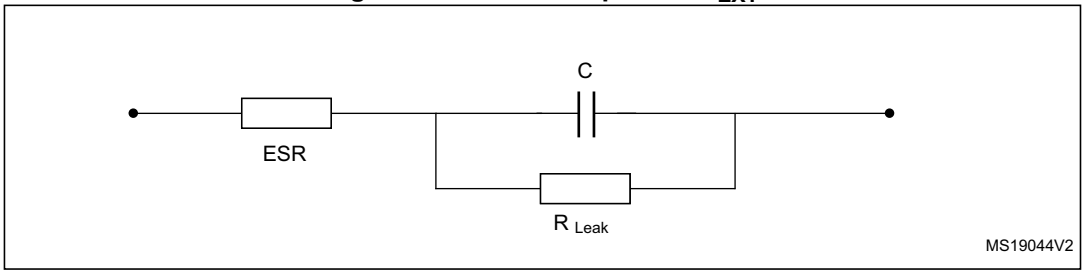
Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$)	Maximum HCLK frequency vs Flash memory wait states (1)(2)	I/O operation	Possible Flash memory operations
V_{DD} =1.7 to 2.1 V(3)	Conversion time up to 1.2 Msps	20 MHz	180 MHz with 8 wait states and over-drive OFF	No I/O compensation	8-bit erase and program operations only
V_{DD} = 2.1 to 2.4 V	Conversion time up to 1.2 Msps	22 MHz	216 MHz with 9 wait states and over-drive ON	No I/O compensation	16-bit erase and program operations
V_{DD} = 2.4 to 2.7 V	Conversion time up to 2.4 Msps	24 MHz	216 MHz with 8 wait states and over-drive ON	I/O compensation works	16-bit erase and program operations
V_{DD} = 2.7 to 3.6 V(4)	Conversion time up to 2.4 Msps	30 MHz	216 MHz with 6 wait states and over-drive ON	I/O compensation works	32-bit erase and program operations

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator on ITCM interface and L1-cache on AXI interface, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator or L1-cache allows to achieve a performance equivalent to 0-wait state program execution.
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 2.18.2: Internal reset OFF*).
4. The voltage range for USB full speed PHYs can drop down to 2.7 V. However the electrical characteristics of D- and D+ pins will be degraded between 2.7 and 3 V.

5.3.2 VCAP1/VCAP2 external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the VCAP1/VCAP2 pins. C_{EXT} is specified in *Table 19*.

Figure 27. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted both to f_{HCLK} frequency and V_{DD} range (see *Table 18: Limitations depending on the operating power supply range*).
- When the regulator is ON, the voltage scaling and over-drive mode are adjusted to f_{HCLK} frequency as follows:
  - Scale 3 for $f_{HCLK} \leq$ 144 MHz
  - Scale 2 for 144 MHz < $f_{HCLK} \leq$ 168 MHz
  - Scale 1 for 168 MHz < $f_{HCLK} \leq$ 216 MHz. The over-drive is only ON at 216 MHz.
- When the regulator is OFF, the V12 is provided externally as described in *Table 17: General operating conditions*:
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- External clock frequency is 25 MHz and PLL is ON when f_{HCLK} is higher than 25 MHz.
- The typical current consumption values are obtained for 1.7 V $\leq V_{DD} \leq$ 3.6 V voltage range and for T_A= 25 °C unless otherwise specified.
- The maximum values are obtained for 1.7 V $\leq V_{DD} \leq$ 3.6 V voltage range and a maximum ambient temperature (T_A) unless otherwise specified.
- For the voltage range 1.7 V $\leq V_{DD} \leq$ 3.6 V, the maximum frequency is 180 MHz.

Table 24. Typical and maximum current consumption in Run mode, code with data processing running from ITCM RAM, regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in RUN mode	All peripherals enabled(2)(3)	216	193	221(4)	258(4)	-	mA
			200	179	207	244	279	
			180	159	176(4)	210(4)	238(4)	
			168	142	156	187	211	
			144	122	135	167	190	
			60	49	55	81	103	
			25	23	28	54	76	
		All peripherals disabled(3)	216	95	107(4)	153(4)	-	
			200	88	100	146	180	
			180	78	88(4)	122(4)	147(4)	
			168	70	78	109	133	
			144	60	68	99	123	
			60	24	29	55	76	
			25	12	16	42	63	

1. Guaranteed by characterization results, unless otherwise specified.

5.3.9 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 65: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 28*.

The characteristics given in *Table 41* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 17*.

Table 41. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External user clock source frequency(1)	-	1	-	50	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	10	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 65: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 29*.

The characteristics given in *Table 42* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 17*.

Table 53. DSI-PLL characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(PLL)}$	PLL power consumption on V_{DD12}	f_{VCO_OUT} = 500 MHz	-	0.55	0.70	mA
		f_{VCO_OUT} = 600 MHz	-	0.65	0.80	
		f_{VCO_OUT} = 1000 MHz	-	0.95	1.20	

1. Based on test during characterization.

5.3.15 MIPI D-PHY regulator characteristics

The parameters given in *Table 54* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 54. DSI regulator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD12DSI}$	1.2 V internal voltage on $V_{DD12DSI}$	-	1.15	1.20	1.30	V
C_{EXT}	External capacitor on V_{CAPDSI}	-	1.1	2.2	3.3	µF
ESR	External Serial Resistor	-	0	25	600	mΩ
$I_{DDDSIREG}$	Regulator power consumption	-	100	120	125	µA
I_{DDDSI}	DSI system (regulator, PLL and D-PHY) current consumption on V_{DDDSI}	Ultra Low Power Mode (Reg. ON + PLL OFF)	-	290	600	µA
		Stop State (Reg. ON + PLL OFF)	-	290	600	
$I_{DDDSILP}$	DSI system current consumption on V_{DDDSI} in LP mode communication(2)	10 MHz escape clock (Reg. ON + PLL OFF)	-	4.3	5.0	mA
		20 MHz escape clock (Reg. ON + PLL OFF)	-	4.3	5.0	
$I_{DDDSIHS}$	DSI system (regulator, PLL and D-PHY) current consumption on V_{DDDSI} in HS mode communication(3)	300 Mbps - 1 data lane (Reg. ON + PLL ON)	-	8.0	8.8	mA
		300 Mbps - 2data lane (Reg. ON + PLL ON)	-	11.4	12.5	
		500 Mbps - 1 data lane (Reg. ON + PLL ON)	-	13.5	14.7	
		500 Mbps - 2data lane (Reg. ON + PLL ON)	-	18.0	19.6	
	DSI system (regulator, PLL and D-PHY) current consumption on V_{DDDSI} in HS mode with CLK like payload	500 Mbps - 2data lane (Reg. ON + PLL ON)	-	21.4	23.3	
t_{WAKEUP}	Startup delay	C_{EXT} = 2.2 µF	-	110	-	µs
		C_{EXT} = 3.3 µF	-	-	160	
I_{INRUSH}	Inrush current on V_{DDDSI}	External capacitor load at start	-	60	200	mA

1. Based on test during characterization.
2. Values based on an average traffic in LP Command Mode.
3. Values based on an average traffic (3/4 HS traffic & 1/4 LP) in Video Mode.

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

5.3.17 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 60*. They are based on the EMS levels and classes defined in application note AN1709.

Table 60. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 216 MHz, conforms to IEC 61000-4-2	2B
V_{FTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A =+25 °C, f_{HCLK} = 168 MHz, conforms to IEC 61000-4-2	5A

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Table 66. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin except PC14	CMOS port(2) I_{IO} = -8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} − 0.4	-	
V_{OH}(3)	Output high level voltage for PC14	CMOS port(2) I_{IO} = -2 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} − 0.4		
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} =+8mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin except PC14	TTL port(2) I_{IO} =-8mA 2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.3(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin except PC14	I_{IO} = -20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}−1.3(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 1.8 V ≤ V_{DD} ≤ 3.6 V	-	0.4(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin except PC14	I_{IO} = -6 mA 1.8 V ≤ V_{DD} ≤ 3.6 V	V_{DD}−0.4(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.7 V ≤ V_{DD} ≤ 3.6V	-	0.4(5)	V
V_{OH}(3)	Output high level voltage for an I/O pin except PC14	I_{IO} = -4 mA 1.7 V ≤ V_{DD} ≤ 3.6V	V_{DD}−0.4(5)	-	
V_{OH}(3)	Output high level voltage for PC14	I_{IO} = -1 mA 1.7 V ≤ V_{DD} ≤ 3.6V	V_{DD}−0.4(5)	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 15*. and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 15* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Based on characterization data.
5. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 39* and *Table 67*, respectively.

Table 71. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 30 MHz, 12-bit resolution	-	-	1764	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* for details	-	-	50	kΩ
R_{ADC}(2)(4)	Sampling switch resistance	-	-	-	6	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	4	7	pF
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.100	µs
			-	-	3(5)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.067	µs
			-	-	2(5)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 30 MHz	0.100	-	16	µs
		-	3	-	480	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	-	2	3	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 30 MHz 12-bit resolution	0.50	-	16.40	µs
		f_{ADC} = 30 MHz 10-bit resolution	0.43	-	16.34	µs
		f_{ADC} = 30 MHz 8-bit resolution	0.37	-	16.27	µs
		f_{ADC} = 30 MHz 6-bit resolution	0.30	-	16.20	µs
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$
f_S(2)	Sampling rate (f_{ADC} = 36 MHz, and t_S = 3 ADC cycles)	12-bit resolution Single ADC	-	-	2.4	Msps
		12-bit resolution Interleave Dual ADC mode	-	-	4.5	Msps
		12-bit resolution Interleave Triple ADC mode	-	-	7.2	Msps

Table 71. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{VREF+}(2)	ADC V_{REF} DC current consumption in conversion mode	-	-	300	500	µA
I_{VDDA}(2)	ADC V_{DDA} DC current consumption in conversion mode	-	-	1.6	1.8	mA

1. V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 2.18.2: Internal reset OFF*).
2. Guaranteed by characterization results.
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. R_{ADC} maximum value is given for V_{DD}=1.7 V, and minimum value for V_{DD}=3.3 V.
5. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 71*.

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

Table 72. ADC static accuracy at f_{ADC} = 18 MHz

Symbol	Parameter	Test conditions	Typ	Max(1)	Unit
ET	Total unadjusted error	f_{ADC} =18 MHz V_{DDA} = 1.7 to 3.6 V V_{REF} = 1.7 to 3.6 V $V_{DDA} - V_{REF}$ < 1.2 V	±3	±4	LSB
EO	Offset error		±2	±3	
EG	Gain error		±1	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±2	±3	

1. Guaranteed by characterization results.

Table 73. ADC static accuracy at f_{ADC} = 30 MHz

Symbol	Parameter	Test conditions	Typ	Max(1)	Unit
ET	Total unadjusted error	f_{ADC} = 30 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V, $V_{DDA} - V_{REF}$ < 1.2 V	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±4	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. Guaranteed by characterization results.

Table 97. Dynamics characteristics: Ethernet MAC signals for RMII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	1	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	2	-	-	
$t_{su(CRS)}$	Carrier sense setup time	2	-	-	
$t_{ih(CRS)}$	Carrier sense hold time	2	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	7.5	8	12	
$t_{d(TXD)}$	Transmit data valid delay time	7	7.5	12.5	

1. Guaranteed by characterization results.

Table 98 gives the list of Ethernet MAC signals for MII and *Figure 58* shows the corresponding timing diagram.

Figure 59. Ethernet MII timing diagram

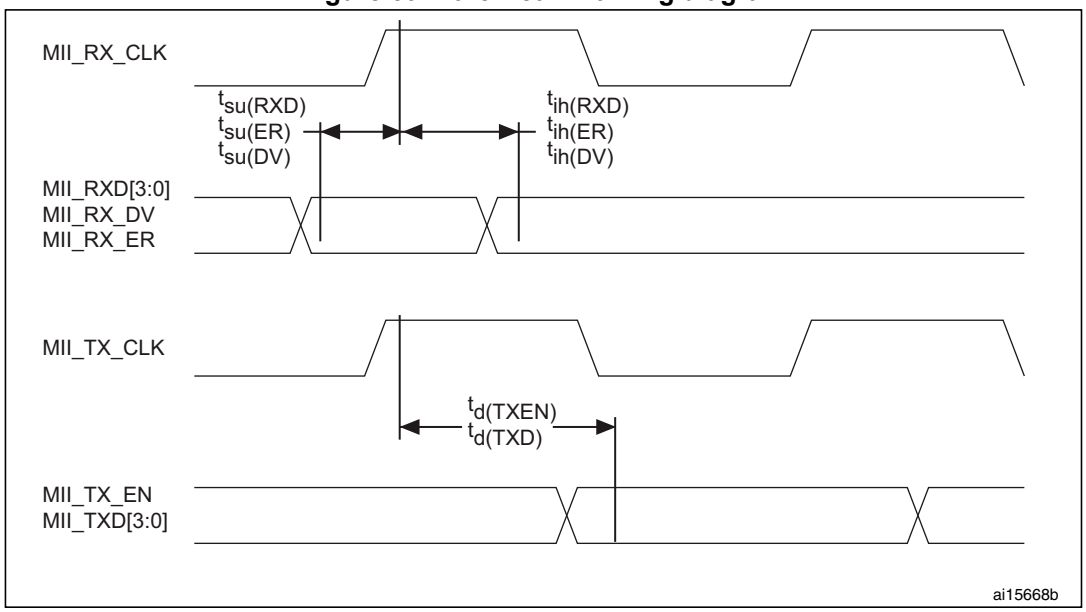


Table 98. Dynamics characteristics: Ethernet MAC signals for MII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	1	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	2.5	-	-	
$t_{su(DV)}$	Data valid setup time	1.5	-	-	
$t_{ih(DV)}$	Data valid hold time	0.5	-	-	
$t_{su(ER)}$	Error setup time	2.5	-	-	
$t_{ih(ER)}$	Error hold time	0.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	10	8	13	
$t_{d(TXD)}$	Transmit data valid delay time	9	7.5	13	

Figure 75. Quad-SPI timing diagram - SDR mode

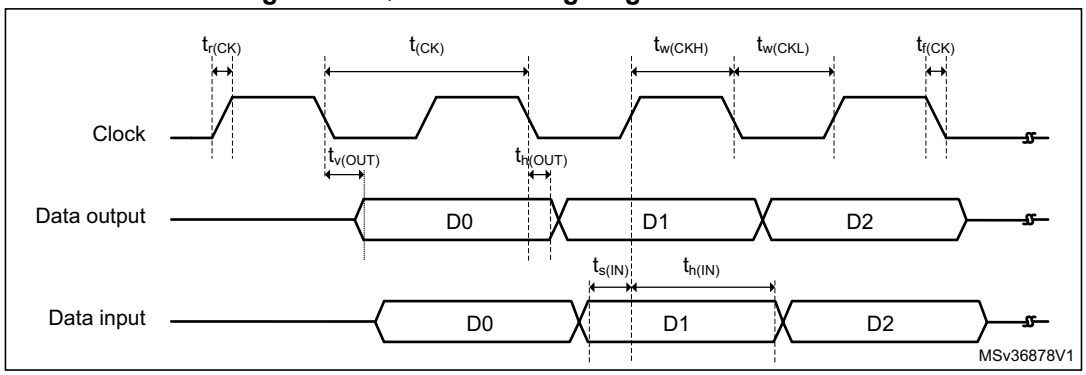
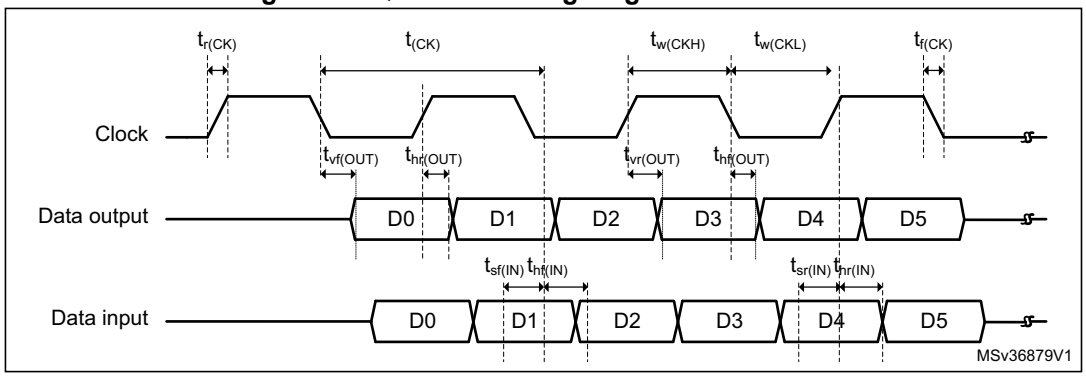


Figure 76. Quad-SPI timing diagram - DDR mode



5.3.32 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 120* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 17*, with the following configuration:

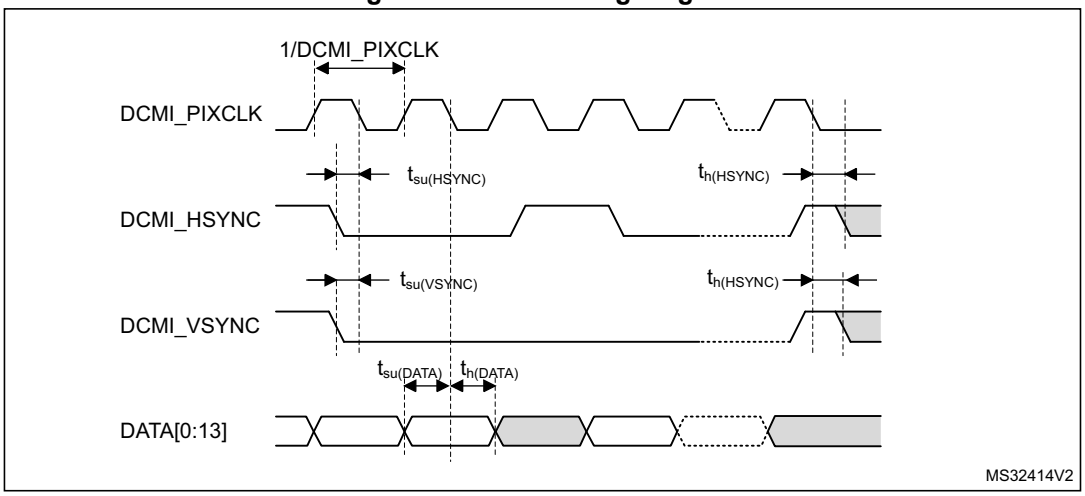
- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits

Table 120. DCMI characteristics(1)

Symbol	Parameter	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	0.4	
DCMI_PIXCLK	Pixel clock input	-	54	MHz
D_{Pixel}	Pixel clock input duty cycle	30	70	%
$t_{su(DATA)}$	Data input setup time	2	-	ns
$t_{h(DATA)}$	Data input hold time	0.5	-	
$t_{su(HSYNC)}$ $t_{su(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input setup time	2.5	-	
$t_{h(HSYNC)}$ $t_{h(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input hold time	3	-	

1. Guaranteed by characterization results.

Figure 77. DCMI timing diagram



5.3.33 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in *Table 121* for LCD-TFT are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 17*, with the following configuration:

- LCD_CLK polarity: high
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits

Table 121. LTDC characteristics (1)

Symbol	Parameter	Min	Max	Unit
f_{CLK}	LTDC clock output frequency	-	65	MHz
D_{CLK}	LTDC clock output duty cycle	45	55	%
$t_{w(CLKH)}$, $t_{w(CLKL)}$	Clock High time, low time	tw(CLK)/2−0.5	tw(CLK)/2+0.5	ns
$t_{v(DATA)}$	Data output valid time	-	6	
$t_{h(DATA)}$	Data output hold time	0	-	
$t_{v(HSYNC)}$, $t_{v(VSYNC)}$, $t_{v(DE)}$	HSYNC/VSYNC/DE output valid time	-	3.5	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$, $t_{h(DE)}$	HSYNC/VSYNC/DE output hold time	0.5	-	

1. Guaranteed by characterization results.

5.3.34 Digital filter for Sigma-Delta Modulators (DFSDM) characteristics

Unless otherwise specified, the parameters given in *Table 122* for DFSDM are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DD} supply voltage summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30pF
- Measurement points are done at CMOS levels: 0.5 x VDD

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (DFSDM1_CKINx, DFSDM1_DATINx, DFSDM1_CKOUT for DFSDM1).

Table 122. DFSDM measured timing 1.71-3.6V

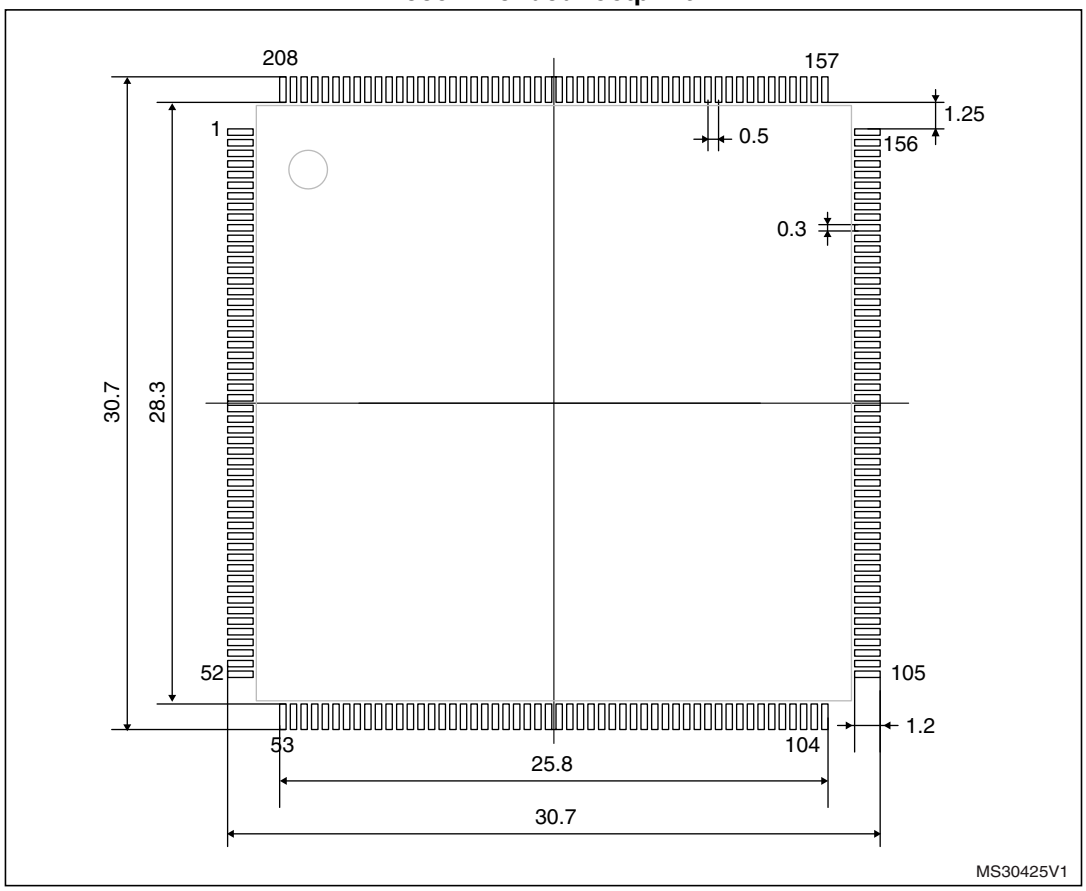
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	1.71 < V_{DD} < 3.6 V	-	-	f_{SYSCLK}	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < V_{DD} < 3.6 V	-	-	20 ($f_{DFSDMCLK}$/4)	
		SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 2.7 < V_{DD} < 3.6 V	-	-	20 ($f_{DFSDMCLK}$/4)	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), 1.71 < V_{DD} < 3.6 V	-	-	20 ($f_{DFSDMCLK}$/4)	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), 2.7 < V_{DD} < 3.6 V	-	-	20 ($f_{DFSDMCLK}$/4)	
f_{CKOUT}	Output clock frequency	1.71 < V_{DD} < 3.6 V	-	-	20	
$DuCy_{CKOUT}$	Output clock frequency duty cycle	1.71 < V_{DD} < 3.6 V	45	50	55	%

Table 128. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	--	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	29.800	30.000	30.200	1.1732	1.1811	1.1890
D1	27.800	28.000	28.200	1.0945	1.1024	1.1102
D3	-	25.500	-	-	1.0039	-
E	29.800	30.000	30.200	1.1732	1.1811	1.1890
E1	27.800	28.000	28.200	1.0945	1.1024	1.1102
E3	-	25.500	-	-	1.0039	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7.0°	0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 93. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Revision history

Table 138. Document revision history

Date	Revision	Changes
21-Mar-2016	1	Initial release.
26-Apr-2016	2	DFSDM replaced by DFSDM1 in: – *Table 10: STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions*. – *Table 12: STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping*. – *Table 13: STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx register boundary addresses*. – *Section 5.3.34: Digital filter for Sigma-Delta Modulators (DFSDM) characteristics*. Updated *Table 2: STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx features and peripheral counts* adding DFSDM1 features. Updated *Table 39: Peripheral current consumption* adding DFSDM1 current consumption. Updated cover in 2 pages. Update cover replacing for SPI ‘up to 50 Mbit/s’ by ‘up to 54 Mbit/s’.
06-May-2016	3	Updated *Table 2: STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx features and peripheral counts* GPIO number. Updated *Table 12: STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping* adding CAN3_RX alternate function on PA8/AF11.
22-Dec-2016	4	Updated *Table 97: Dynamics characteristics: Ethernet MAC signals for RMII*. Updated *Table 71: ADC characteristics* sampling rate. Updated all the notes removing ‘not tested in production’. Updated *Figure 46: SPI timing diagram - slave mode and CPHA = 0* and *Figure 47: SPI timing diagram - slave mode and CPHA = 1(1)* with modified NSS timing waveforms (among other changes). Updated *Table 121: LTDC characteristics* clock output frequency at 65 MHz. Updated *Section 5.2: Absolute maximum ratings*. Updated *Section 6: Package information* adding information about other optional marking or inset/upset marks.