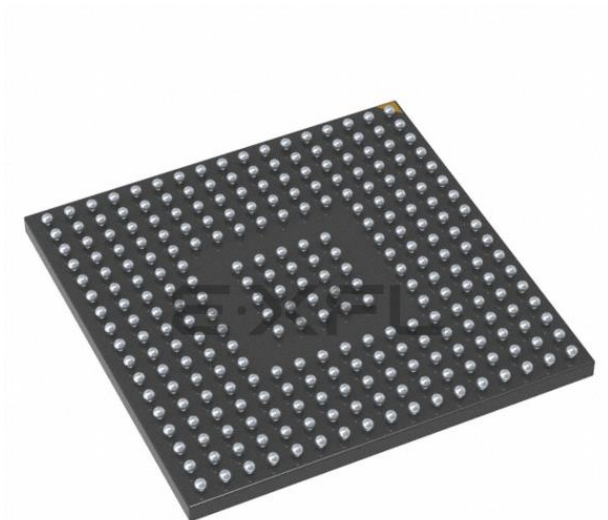




Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex® -M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	140
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	201-UF BGA
Supplier Device Package	176+25UF BGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f765iik7

5.3.25	Temperature sensor characteristics	175
5.3.26	V _{BAT} monitoring characteristics	175
5.3.27	Reference voltage	175
5.3.28	DAC electrical characteristics	176
5.3.29	Communications interfaces	178
5.3.30	FMC characteristics	195
5.3.31	Quad-SPI interface characteristics	215
5.3.32	Camera interface (DCMI) timing specifications	217
5.3.33	LCD-TFT controller (LTDC) characteristics	218
5.3.34	Digital filter for Sigma-Delta Modulators (DFSDM) characteristics	220
5.3.35	DFSDM timing diagrams	222
5.3.36	SD/SDIO MMC card host interface (SDMMC) characteristics	223
6	Package information	225
6.1	LQFP100 14x 14 mm, low-profile quad flat package information	225
6.2	LQFP144 20 x 20 mm, low-profile quad flat package information	229
6.3	LQFP176 24 x 24 mm, low-profile quad flat package information	233
6.4	LQFP208 28 x 28 mm low-profile quad flat package information	237
6.5	WLCSP 180-bump, 5.5 x 6 mm, wafer level chip scale package information	241
6.6	UFBGA176+25, 10 x 10, 0.65 mm ultra thin fine-pitch ball grid array package information	245
6.7	TFBGA216, 13 x 13 x 0.8 mm thin fine-pitch ball grid array package information	248
6.8	Thermal characteristics	251
7	Ordering information	252
	Appendix A Recommendations when using internal reset OFF	253
A.1	Operating conditions	253
	Revision history	254

List of figures

Figure 1.	Compatible board design for LQFP100 package	18
Figure 2.	STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx block diagram	19
Figure 3.	STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx AXI-AHB bus matrix architecture ⁽¹⁾	22
Figure 4.	VDDUSB connected to VDD power supply.	28
Figure 5.	VDDUSB connected to external power supply	29
Figure 6.	Power supply supervisor interconnection with internal reset OFF	30
Figure 7.	PDR_ON control with internal reset OFF	31
Figure 8.	Regulator OFF	33
Figure 9.	Startup in regulator OFF: slow V_{DD} slope	
	- power-down reset risen after V_{CAP_1} , V_{CAP_2} stabilization	34
Figure 10.	Startup in regulator OFF mode: fast V_{DD} slope	
	- power-down reset risen before V_{CAP_1} , V_{CAP_2} stabilization.	34
Figure 11.	STM32F76xxx LQFP100 pinout	54
Figure 12.	STM32F76xxx LQFP144 pinout	55
Figure 13.	STM32F76xxx LQFP176 pinout	56
Figure 14.	STM32F769xx LQFP176 pinout	57
Figure 15.	STM32F769Ax/STM32F768Ax WLCSP180 ballout	58
Figure 16.	STM32F76xxx LQFP208 pinout	59
Figure 17.	STM32F769xx LQFP208 pinout	60
Figure 18.	STM32F76xxx UFBGA176 ballout	61
Figure 19.	STM32F76xxx TFBGA216 ballout	62
Figure 20.	STM32F769xx TFBGA216 ballout	63
Figure 21.	Memory map	106
Figure 22.	Pin loading conditions	111
Figure 23.	Pin input voltage	111
Figure 24.	STM32F769xx/STM32F779xx power supply scheme	112
Figure 25.	STM32F767xx/STM32F777xx power supply scheme	113
Figure 26.	Current consumption measurement scheme	114
Figure 27.	External capacitor C_{EXT}	118
Figure 28.	High-speed external clock source AC timing diagram	141
Figure 29.	Low-speed external clock source AC timing diagram	142
Figure 30.	Typical application with an 8 MHz crystal	143
Figure 31.	Typical application with a 32.768 kHz crystal	144
Figure 32.	ACCHSI versus temperature	145
Figure 33.	LSI deviation versus temperature	146
Figure 34.	PLL output clock waveforms in center spread mode	150
Figure 35.	PLL output clock waveforms in down spread mode	151
Figure 36.	MIPI D-PHY HS/LP clock lane transition timing diagram	154
Figure 37.	MIPI D-PHY HS/LP data lane transition timing diagram	154
Figure 38.	FT I/O input characteristics	164
Figure 39.	I/O AC characteristics definition	167
Figure 40.	Recommended NRST pin protection	168
Figure 41.	ADC accuracy characteristics	173
Figure 42.	Typical connection diagram using the ADC	173
Figure 43.	Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})	174
Figure 44.	Power supply and reference decoupling (V_{REF+} connected to V_{DDA})	174
Figure 45.	12-bit buffered /non-buffered DAC	178

Figure 46.	SPI timing diagram - slave mode and CPHA = 0	181
Figure 47.	SPI timing diagram - slave mode and CPHA = 1 ⁽¹⁾	182
Figure 48.	SPI timing diagram - master mode ⁽¹⁾	182
Figure 49.	I ² S slave timing diagram (Philips protocol) ⁽¹⁾	184
Figure 50.	I ² S master timing diagram (Philips protocol) ⁽¹⁾	184
Figure 51.	JTAG timing diagram	186
Figure 52.	SWD timing diagram	187
Figure 53.	SAI master timing waveforms	188
Figure 54.	SAI slave timing waveforms	189
Figure 55.	USB OTG full speed timings: definition of data signal rise and fall time	190
Figure 56.	ULPI timing diagram	192
Figure 57.	Ethernet SMI timing diagram	193
Figure 58.	Ethernet RMII timing diagram	193
Figure 59.	Ethernet MII timing diagram	194
Figure 60.	MDIO Slave timing diagram	195
Figure 61.	Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms	196
Figure 62.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms	198
Figure 63.	Asynchronous multiplexed PSRAM/NOR read waveforms	199
Figure 64.	Asynchronous multiplexed PSRAM/NOR write waveforms	201
Figure 65.	Synchronous multiplexed NOR/PSRAM read timings	203
Figure 66.	Synchronous multiplexed PSRAM write timings	205
Figure 67.	Synchronous non-multiplexed NOR/PSRAM read timings	207
Figure 68.	Synchronous non-multiplexed PSRAM write timings	208
Figure 69.	NAND controller waveforms for read access	210
Figure 70.	NAND controller waveforms for write access	210
Figure 71.	NAND controller waveforms for common memory read access	211
Figure 72.	NAND controller waveforms for common memory write access	211
Figure 73.	SDRAM read access waveforms (CL = 1)	212
Figure 74.	SDRAM write access waveforms	214
Figure 75.	Quad-SPI timing diagram - SDR mode	217
Figure 76.	Quad-SPI timing diagram - DDR mode	217
Figure 77.	DCMI timing diagram	218
Figure 78.	LCD-TFT horizontal timing diagram	219
Figure 79.	LCD-TFT vertical timing diagram	219
Figure 80.	Channel transceiver timing diagrams	222
Figure 81.	SDIO high-speed mode	223
Figure 82.	SD default mode	223
Figure 83.	LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline	225
Figure 84.	LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package recommended footprint	227
Figure 85.	LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package top view example	228
Figure 86.	LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline	229
Figure 87.	LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package recommended footprint	231
Figure 88.	LQFP144, 20 x 20mm, 144-pin low-profile quad flat package top view example	232
Figure 89.	LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package outline	233
Figure 90.	LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package recommended footprint	235
Figure 91.	LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package top view example	236

2.10 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 display layers with dedicated FIFO (64x32-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events

2.11 Chrom-ART Accelerator™ (DMA2D)

The Chrom-Art Accelerator™ (DMA2D) is a graphic accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion

Various image format codings are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

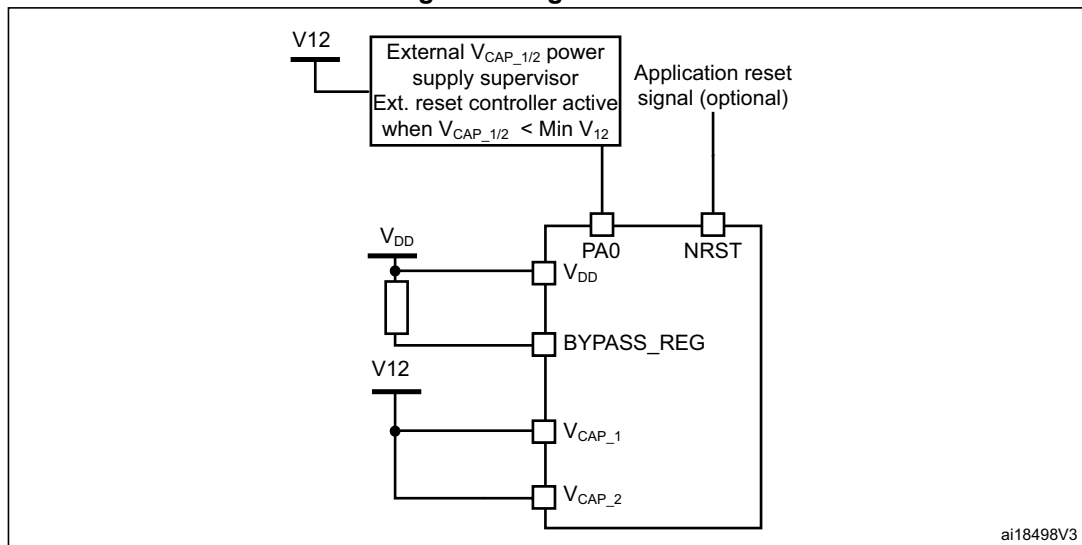
2.12 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 110 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M7 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

Figure 8. Regulator OFF



The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is faster than the time for V_{DD} to reach 1.7 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach V_{12} minimum value and until V_{DD} reaches 1.7 V (see [Figure 9](#)).
- Otherwise, if the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is slower than the time for V_{DD} to reach 1.7 V, then PA0 could be asserted low externally (see [Figure 10](#)).
- If V_{CAP_1} and V_{CAP_2} go below V_{12} minimum value and V_{DD} is higher than 1.7 V, then a reset must be asserted on PA0 pin.

Note: The minimum value of V_{12} depends on the maximum frequency targeted in the application.

2.19.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal reset ON/OFF availability

Package	Regulator ON	Regulator OFF	Internal reset ON	Internal reset OFF
LQFP100	Yes	No	Yes	No
LQFP144, LQFP208			Yes PDR_ON set to V _{DD}	Yes PDR_ON set to V _{SS}
LQFP176, UFBGA176, TFBGA216	Yes BYPASS_REG set to V _{SS}	Yes BYPASS_REG set to V _{DD}		
WLCSP180	Yes ⁽¹⁾			

1. Available only on dedicated part number. Refer to [Section 7: Ordering information](#).

2.20 Real-time clock (RTC), backup SRAM and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

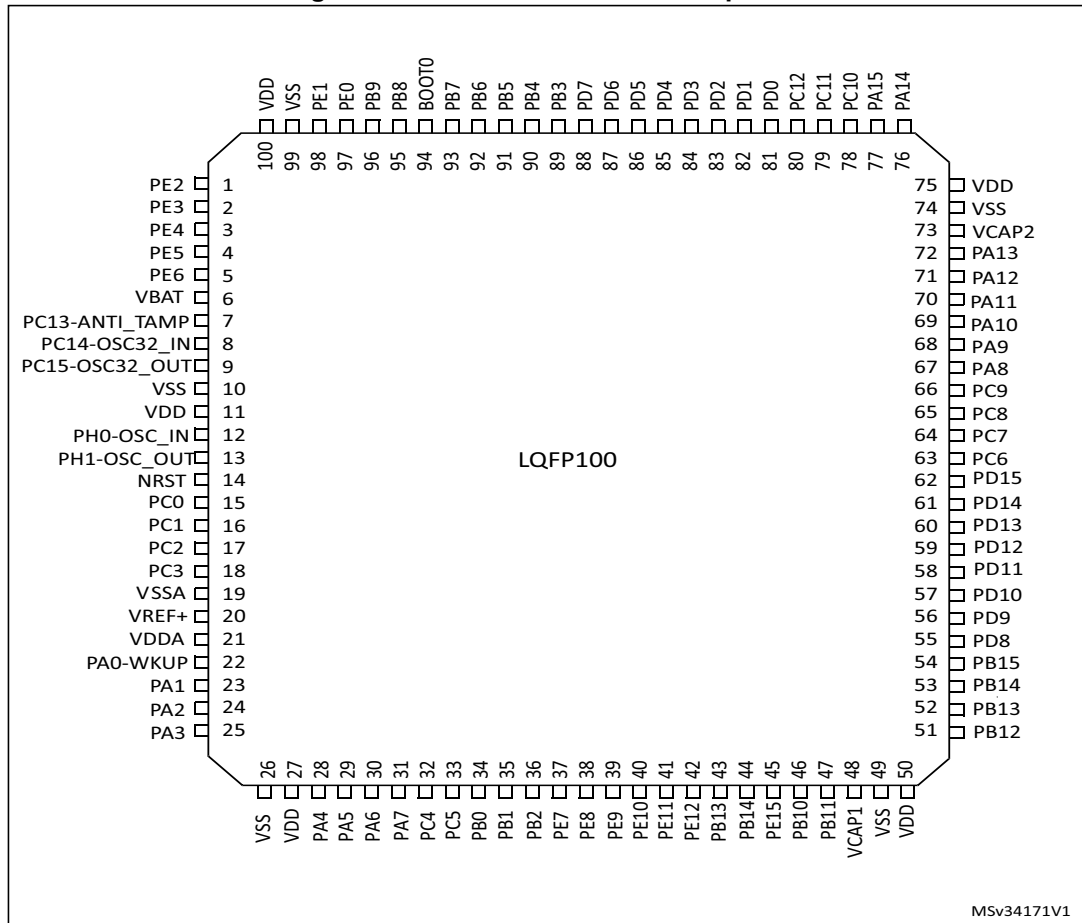
- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to V_{BAT} mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the V_{BAT} pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

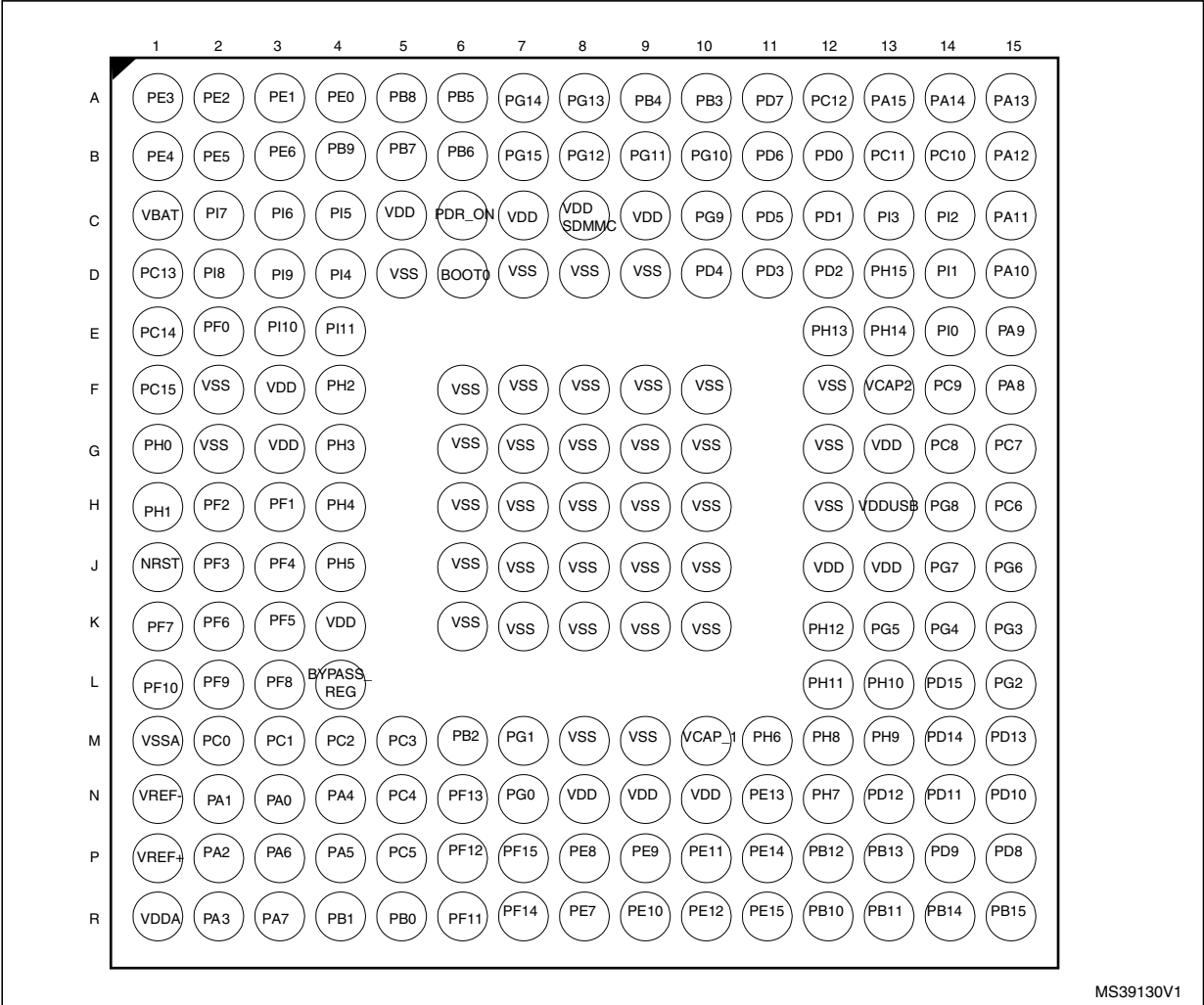
3 Pinouts and pin description

Figure 11. STM32F76xxx LQFP100 pinout



1. The above figure shows the package top view.

Figure 18. STM32F76xxx UFBGA176 ballout



MS39130V1

1. The above figure shows the package top view.

Table 12. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF	SPI6/SAI2/USART6/USART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM1/OTG_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port G	PG8	-	-	-	-	-	SPI6_NS	-	SPDIF_RX2	USART6_RTS	-	-	ETH_PPS_OUT	FMC_SD_CLK	-	LCD_G7	EVEN TOUT
	PG9	-	-	-	-	-	SPI1_MI	-	SPDIF_RX3	USART6_RX	QUADSPI_BK2_IO2	SAI2_FS_B	SDMMC2_D0	FMC_NE2/FMC_NCE	DCMI_V_SYNC	-	EVEN TOUT
	PG10	-	-	-	-	-	SPI1_NS	-	-	-	LCD_G3	SAI2_SD_B	SDMMC2_D1	FMC_NE3	DCMI_D2	LCD_B2	EVEN TOUT
	PG11	-	-	-	-	-	SPI1_SC	-	SPDIF_RX0	-	-	SDMMC2_D2	ETH_MII_TX_EN/ETH_RMII_TX_EN	-	DCMI_D3	LCD_B3	EVEN TOUT
	PG12	-	-	-	LPTIM1_IN1	-	SPI6_MI	-	SPDIF_RX1	USART6_RTS	LCD_B4	-	SDMMC2_D3	FMC_NE4	-	LCD_B1	EVEN TOUT
	PG13	TRACED0	-	-	LPTIM1_OUT	-	SPI6_SC	-	-	USART6_CTS	-	-	ETH_MII_TXD0/ETH_RMII_TXD0	FMC_A24	-	LCD_R0	EVEN TOUT
	PG14	TRACED1	-	-	LPTIM1_ETR	-	SPI6_MOSI	-	-	USART6_TX	QUADSPI_BK2_IO3	-	ETH_MII_TXD1/ETH_RMII_TXD1	FMC_A25	-	LCD_B0	EVEN TOUT
	PG15	-	-	-	-	-	-	-	-	USART6_CTS	-	-	-	FMC_SD_NCAS	DCMI_D13	-	EVEN TOUT

Table 27. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (Single bank mode) or SRAM on AXI (L1-cache disabled), regulator ON

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ	Max ⁽¹⁾			Unit
					TA= 25 °C	TA=85 °C	TA=105 °C	
I _{DD}	Supply current in RUN mode	All peripherals enabled ⁽²⁾⁽³⁾	216	190	209	255	-	mA
			200	177	194	241	268	
			180	160	175	211	232	
			168	144	156	189	209	
			144	115	125	152	170	
			60	56	62	89	107	
			25	27	32	59	79	
		All peripherals disabled ⁽³⁾	216	92	103	150	-	
			200	86	96	243	171	
			180	79	87	123	144	
			168	71	79	111	131	
			144	60	65	92	110	
			60	32	36	63	80	
			25	16	20	46	64	

1. Guaranteed by characterization results, unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 33. Typical and maximum current consumption in Sleep mode, regulator ON

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ	Max ⁽¹⁾			Unit
					T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	
I _{DD}	Supply current in Sleep mode	All peripherals enabled ⁽²⁾	216	128	144 ⁽³⁾	190 ⁽³⁾	-	mA
			200	119	134	180	214	
			180	105	118 ⁽³⁾	153 ⁽³⁾	178 ⁽³⁾	
			168	93	105	136	156	
			144	72	80	107	124	
			60	33	39	65	82	
			25	17	21	47	65	
		All peripherals disabled	216	18	25 ⁽³⁾	71 ⁽³⁾	-	
			200	17	24	70	112	
			180	14	20 ⁽³⁾	54 ⁽³⁾	75 ⁽³⁾	
			168	13	18	49	69	
			144	10	14	40	58	
			60	6	10	36	53	
			25	4	8	34	51	

1. Guaranteed by characterization results, unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. Guaranteed by test in production.

5.3.9 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the [Table 65: I/O static characteristics](#). However, the recommended clock input waveform is shown in [Figure 28](#).

The characteristics given in [Table 41](#) result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 17](#).

Table 41. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External user clock source frequency ⁽¹⁾	-	1	-	50	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time ⁽¹⁾		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time ⁽¹⁾		-	-	10	
$C_{in(HSE)}$	OSC_IN input capacitance ⁽¹⁾	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1	μA

1. Guaranteed by design.

Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the [Table 65: I/O static characteristics](#). However, the recommended clock input waveform is shown in [Figure 29](#).

The characteristics given in [Table 42](#) result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 17](#).

5.3.11 PLL characteristics

The parameters given in [Table 47](#) and [Table 48](#) are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in [Table 17](#).

Table 47. Main PLL characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f _{PLL_IN}	PLL input clock ⁽¹⁾	-		0.95 ⁽²⁾	1	2.10	MHz
f _{PLL_OUT}	PLL multiplier output clock	-		24	-	216	
f _{PLL48_OUT}	48 MHz PLL multiplier output clock	-		-	48	75	
f _{VCO_OUT}	PLL VCO output	-		100	-	432	
t _{LOCK}	PLL lock time	VCO freq = 192 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter ⁽³⁾	Cycle-to-cycle jitter	System clock 216 MHz	RMS	-	25	-	ps
			peak to peak	-	±150	-	
	Period Jitter		RMS	-	15	-	
			peak to peak	-	±200	-	
	Main clock output (MCO) for RMII Ethernet	Cycle to cycle at 50 MHz on 1000 samples		-	32	-	
	Main clock output (MCO) for MII Ethernet	Cycle to cycle at 25 MHz on 1000 samples		-	40	-	
	Bit Time CAN jitter	Cycle to cycle at 1 MHz on 1000 samples		-	330	-	
I _{DD(PLL)} ⁽⁴⁾	PLL power consumption on V _{DD}	VCO freq = 192 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
I _{DDA(PLL)} ⁽⁴⁾	PLL power consumption on V _{DDA}	VCO freq = 192 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design.
3. The use of 2 PLLs in parallel could degraded the Jitter up to +30%.
4. Guaranteed by characterization results.

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

5.3.17 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 60](#). They are based on the EMS levels and classes defined in application note AN1709.

Table 60. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ °C}$, $f_{HCLK} = 216\text{ MHz}$, conforms to IEC 61000-4-2	2B
V_{FTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ °C}$, $f_{HCLK} = 168\text{ MHz}$, conforms to IEC 61000-4-2	5A

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

5.3.25 Temperature sensor characteristics

Table 77. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	V_{SENSE} linearity with temperature	-	± 1	± 2	$^{\circ}\text{C}$
Avg_Slope ⁽¹⁾	Average slope	-	2.5	-	mV/ $^{\circ}\text{C}$
$V_{25}^{(1)}$	Voltage at 25 $^{\circ}\text{C}$	-	0.76	-	V
$t_{START}^{(2)}$	Startup time	-	6	10	μs
$T_{S_temp}^{(2)}$	ADC sampling time when reading the temperature (1 $^{\circ}\text{C}$ accuracy)	10	-	-	μs

1. Guaranteed by characterization results.

2. Guaranteed by design.

Table 78. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 $^{\circ}\text{C}$, $V_{DDA} = 3.3\text{ V}$	0x1FF0 F44C - 0x1FF0 F44D
TS_CAL2	TS ADC raw data acquired at temperature of 110 $^{\circ}\text{C}$, $V_{DDA} = 3.3\text{ V}$	0x1FF0 F44E - 0x1FF0 F44F

5.3.26 V_{BAT} monitoring characteristics

Table 79. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	K Ω
Q	Ratio on V_{BAT} measurement	-	4	-	
$E_r^{(1)}$	Error on Q	-1	-	+1	%
$T_{S_vbat}^{(2)(2)}$	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	μs

1. Guaranteed by design.

2. Shortest sampling time can be determined in the application by multiple iterations.

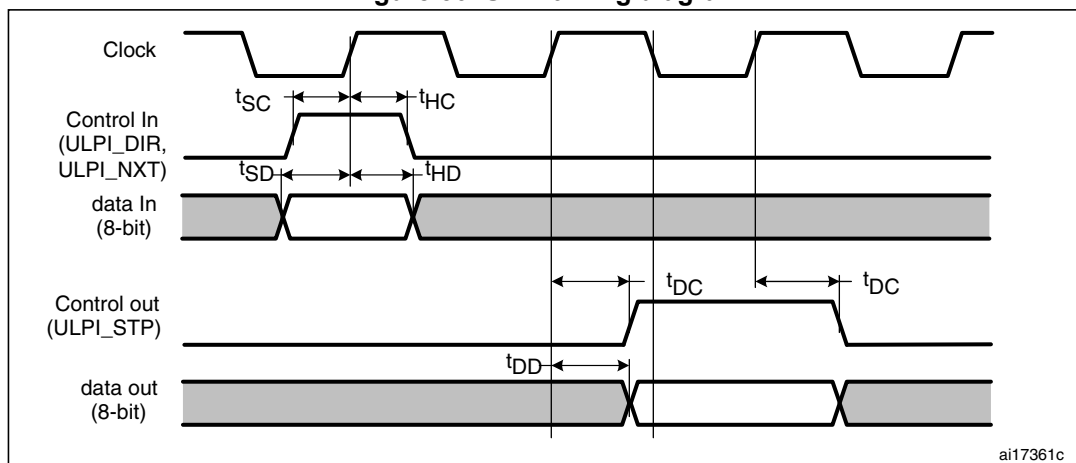
5.3.27 Reference voltage

The parameters given in [Table 80](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 17](#).

Table 80. internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	$-40\text{ }^{\circ}\text{C} < T_A < +105\text{ }^{\circ}\text{C}$	1.18	1.21	1.24	V
$T_{S_vrefint}^{(1)}$	ADC sampling time when reading the internal reference voltage	-	10	-	-	μs
$V_{RERINT_s}^{(2)}$	Internal reference voltage spread over the temperature range	$V_{DD} = 3\text{ V} \pm 10\text{ mV}$	-	3	5	mV

Figure 56. ULPI timing diagram

Table 95. Dynamic characteristics: USB ULPI⁽¹⁾

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{SC}	Control in (ULPI_DIR, ULPI_NXT) setup time	-	2	-	-	ns
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	-	1.5	-	-	
t_{SD}	Data in setup time	-	2	-	-	
t_{HD}	Data in hold time	-	1	-	-	
t_{DC}/t_{DD}	Data/control output delay	$2.7\text{ V} < V_{DD} < 3.6\text{ V}$, $C_L = 20\text{ pF}$	-	6.5	8	
		-	-	-	-	
		$1.7\text{ V} < V_{DD} < 3.6\text{ V}$, $C_L = 15\text{ pF}$	-	6.5	11	

1. Guaranteed by characterization results.

Ethernet characteristics

Unless otherwise specified, the parameters given in [Table 96](#), [Table 97](#) and [Table 98](#) for SMI, RMII and MII are derived from tests performed under the ambient temperature, f_{HCLK} frequency summarized in [Table 17](#), with the following configuration:

- Output speed is set to $OSPEEDR[1:0] = 10$
- Capacitive load $C = 20\text{ pF}$
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to [Section 5.3.20: I/O port characteristics](#) for more details on the input/output characteristics.

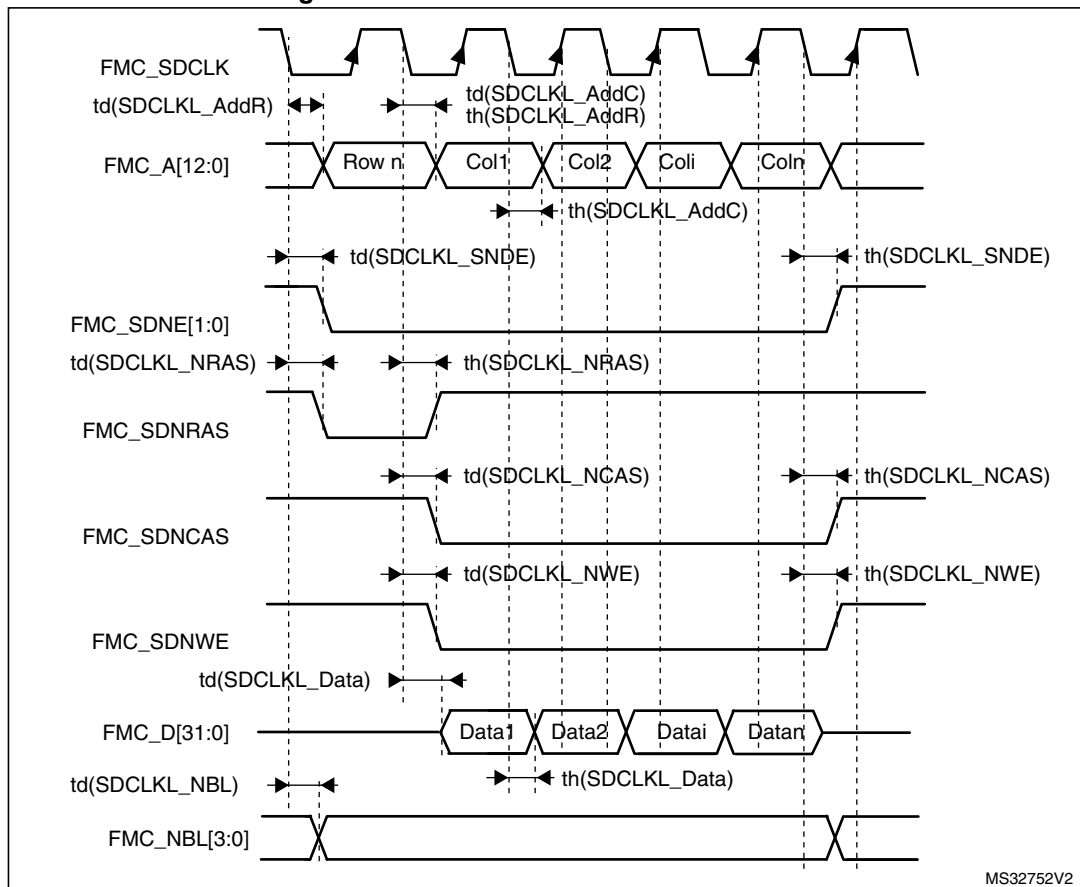
[Table 96](#) gives the list of Ethernet MAC signals for the SMI (station management interface) and [Figure 57](#) shows the corresponding timing diagram.

Table 108. Synchronous multiplexed NOR/PSRAM read timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK} - 0.5$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low ($x=0..2$)	-	2	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high ($x=0..2$)	$T_{HCLK} + 0.5$	-	
$t_{d(CLKL-NADV_L)}$	FMC_CLK low to FMC_NADV low	-	1.	
$t_{d(CLKL-NADV_H)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid ($x=16..25$)	-	2.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid ($x=16..25$)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{HCLK} - 0.5$	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	1.5	-	
$t_h(CLKH-ADV)$	FMC_A/D[15:0] valid data after FMC_CLK high	3.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_h(CLKH-NWAIT)$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. Guaranteed by characterization results.

Figure 74. SDRAM write access waveforms



MS32752V2

Table 116. SDRAM write timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK} + 0.5$	ns
$t_{d(SDCLKL_Data)}$	Data output valid time	-	3	
$t_{h(SDCLKL_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	3.5	
$t_{d(SDCLKL_SDNWE)}$	SDNWE valid time	-	1.5	
$t_{h(SDCLKL_SDNWE)}$	SDNWE hold time	0.5	-	
$t_{d(SDCLKL_SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	0.5	-	
$t_{d(SDCLKL_SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0.5	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	1	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS hold time	0.5	-	

1. Guaranteed by characterization results.

Table 117. LPSDR SDRAM write timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK} + 0.5$	ns
$t_{d(SDCLKL_Data)}$	Data output valid time	-	2.5	
$t_{h(SDCLKL_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	2.5	
$t_{d(SDCLKL-SDNWE)}$	SDNWE valid time	-	2.5	
$t_{h(SDCLKL-SDNWE)}$	SDNWE hold time	0	-	
$t_{d(SDCLKL-SDNE)}$	Chip select valid time	-	0.5	
$t_{h(SDCLKL-SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL-SDNRAS)}$	SDNRAS valid time	-	1.5	
$t_{h(SDCLKL-SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

5.3.31 Quad-SPI interface characteristics

Unless otherwise specified, the parameters given in [Table 118](#) and [Table 119](#) for Quad-SPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in [Table 17: General operating conditions](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

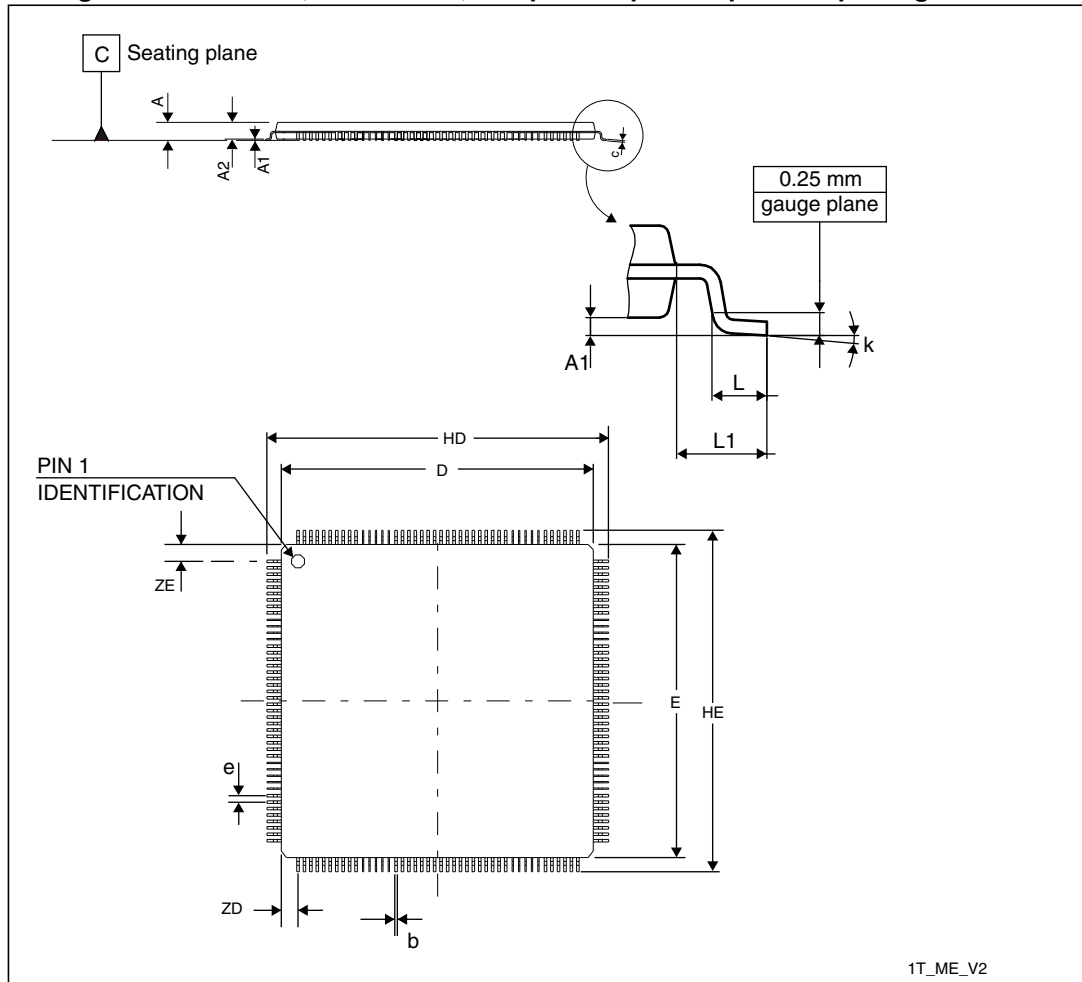
Refer to [Section 5.3.20: I/O port characteristics](#) for more details on the input/output alternate function characteristics.

Table 118. Quad-SPI characteristics in SDR mode⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Fck1/t(CK)	Quad-SPI clock frequency	$2.7 V \leq V_{DD} < 3.6 V$ CL=20 pF	-	-	108	MHz
		$1.71 V < V_{DD} < 3.6 V$ CL=15 pF	-	-	100	

6.3 LQFP176 24 x 24 mm, low-profile quad flat package information

Figure 89. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package outline



1. Drawing is not to scale.