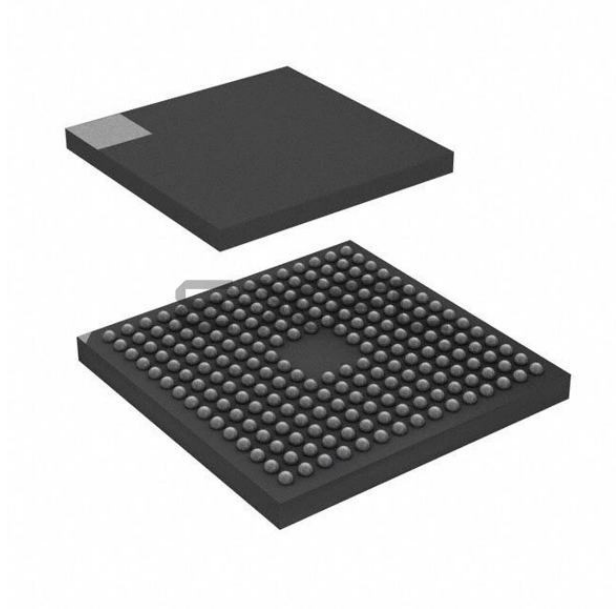

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	168
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	216-TFBGA
Supplier Device Package	216-TFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f765ngh6

2.7 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. The configuration is made by software and the transfer sizes between the source and the destination are independent.

The DMA can be used with the main peripherals:

- SPI and I^2S
- I^2C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDMMC
- Camera interface (DCMI)
- ADC
- SAI
- SPDIFRX
- Quad-SPI
- HDMI-CEC
- JPEG codec
- DFSDM1

2.23.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

2.23.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F76xxx devices (see *Table 6* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The STM32F76xxx include 4 full-featured general-purpose timers: TIM2, TIM5, TIM3, and TIM4.The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

  The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10, TIM11, TIM12, TIM13, and TIM14**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

2.23.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

2.25 Universal synchronous/asynchronous receiver transmitters (USART)

The devices embed USART. Refer to *Table 8: USART implementation* for the features implementation.

The universal synchronous asynchronous receiver transmitter (USART) offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format.

The USART peripheral supports:

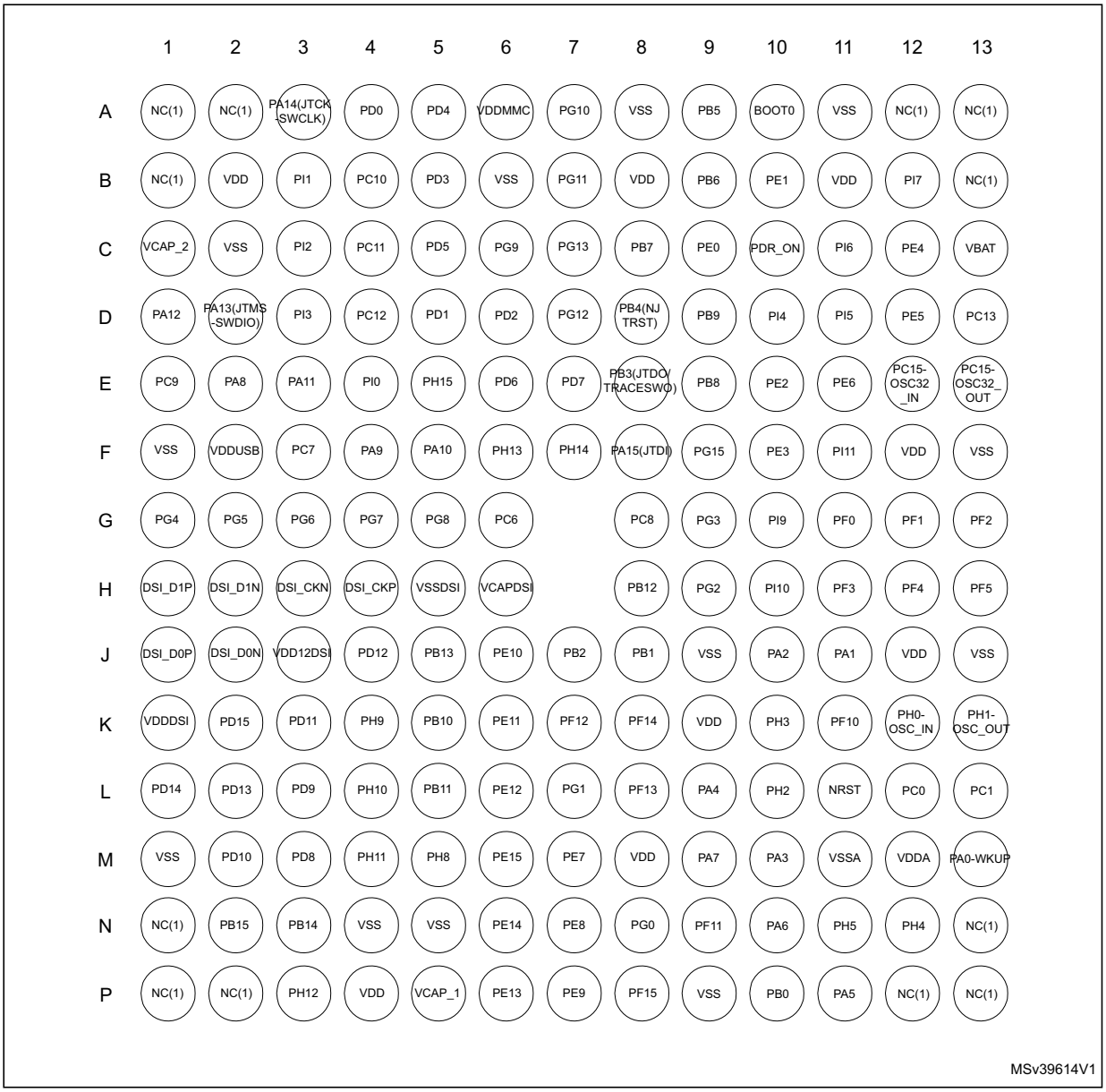
- Full-duplex asynchronous communications
- Configurable oversampling method by 16 or 8 to give flexibility between speed and clock tolerance
- Dual clock domain allowing convenient baud rate programming independent from the PCLK reprogramming
- A common programmable transmit and receive baud rate of up to 27 Mbit/s when the USART clock source is system clock frequency (max is 216 MHz) and oversampling by 8 is used.
- Auto baud rate detection
- Programmable data word length (7 or 8 or 9 bits) word length
- Programmable data order with MSB-first or LSB-first shifting
- Progarmmable parity (odd, even, no parity)
- Configurable stop bits (1 or 1.5 or 2 stop bits)
- Synchronous mode and clock output for synchronous communications
- Single-wire half-duplex communications
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Multiprocessor communications
- LIN master synchronous break send capability and LIN slave break detection capability
- IrDA SIR encoder decoder supporting 3/16 bit duration for normal mode
- Smartcard mode (T=0 and T=1 asynchronous protocols for Smartcards as defined in the ISO/IEC 7816-3 standard)
- Support for Modbus communication

Table 8 summarizes the implementation of all U(S)ARTs instances

Table 8. USART implementation

features(1)	USART1/2/3/6	UART4/5/7/8
Data Length	7, 8 and 9 bits	
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode	X	-

Figure 15. STM32F769Ax/STM32F768Ax WLCSP180 ballout



1. NC ball must not be connected to GND nor to VDD.
2. The above figure shows the package top view.

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	-	-	-	120	H12	-	-	-	-	PJ8	I/O	FT	-	LCD_G1, EVENTOUT	-
-	-	-	-	121	J13	-	-	-	-	PJ9	I/O	FT	-	LCD_G2, EVENTOUT	-
-	-	-	-	122	H13	-	-	-	-	PJ10	I/O	FT	-	LCD_G3, EVENTOUT	-
-	-	-	-	123	G12	-	-	-	-	PJ11	I/O	FT	-	LCD_G4, EVENTOUT	-
-	-	-	-	124	H11	-	-	-	-	VDD	S	-	-	-	-
-	-	-	-	-	-	K1	99	118	H11	VDDDSI	S	-	-	-	-
-	-	-	-	125	H10	-	-	-	H10	VSS	S	-	-	-	-
-	-	-	-	-	-	H6	100	119	K12	VCAPDSI	S	-	-	-	-
-	-	-	-	-	-	J3	-	-	G13	VDD12DSI	S	-	-	-	-
-	-	-	-	-	-	J1	101	120	J12	DSI_D0P	I/O	-	-	-	-
-	-	-	-	-	-	J2	102	121	J13	DSI_D0N	I/O	-	-	-	-
-	-	-	-	-	-	H5	103	122	G12	VSSDSI	S	-	-	-	-
-	-	-	-	-	-	H4	104	123	H12	DSI_CKP	I/O	-	-	-	-
-	-	-	-	-	-	H3	105	124	H13	DSI_CKN	I/O	-	-	-	-
-	-	-	-	-	-	-	106	125	-	VDD12DSI	S			-	-
-	-	-	-	-	-	H1	107	126	F12	DSI_D1P	I/O		-	-	-
-	-	-	-	-	-	H2	108	127	F13	DSI_D1N	I/O		-	-	-
-	-	-	-	-	-	-	109	128	-	VSSDSI	S		-	-	-
-	-	-	-	126	G13	-	-	-	-	PK0	I/O	FT	-	LCD_G5, EVENTOUT	-
-	-	-	-	127	F12	-	-	-	-	PK1	I/O	FT	-	LCD_G6, EVENTOUT	-
-	-	-	-	128	F13	-	-	-	-	PK2	I/O	FT	-	LCD_G7, EVENTOUT	-
-	87	L15	106	129	M13	H9	110	129	M13	PG2	I/O	FT	-	FMC_A12, EVENTOUT	-
-	88	K15	107	130	M12	G9	111	130	M12	PG3	I/O	FT	-	FMC_A13, EVENTOUT	-

Table 11. FMC pin definition

Pin name	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PF0	A0	-	-	A0
PF1	A1	-	-	A1
PF2	A2	-	-	A2
PF3	A3	-	-	A3
PF4	A4	-	-	A4
PF5	A5	-	-	A5
PF12	A6	-	-	A6
PF13	A7	-	-	A7
PF14	A8	-	-	A8
PF15	A9	-	-	A9
PG0	A10	-	-	A10
PG1	A11	-	-	A11
PG2	A12	-	-	A12
PG3	A13	-	-	-
PG4	A14	-	-	BA0
PG5	A15	-	-	BA1
PD11	A16	A16	CLE	-
PD12	A17	A17	ALE	-
PD13	A18	A18	-	-
PE3	A19	A19	-	-
PE4	A20	A20	-	-
PE5	A21	A21	-	-
PE6	A22	A22	-	-
PE2	A23	A23	-	-
PG13	A24	A24	-	-
PG14	A25	A25	-	-
PD14	D0	DA0	D0	D0
PD15	D1	DA1	D1	D1
PD0	D2	DA2	D2	D2
PD1	D3	DA3	D3	D3
PE7	D4	DA4	D4	D4
PE8	D5	DA5	D5	D5
PE9	D6	DA6	D6	D6
PE10	D7	DA7	D7	D7

Table 12. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM1/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port D	PD8	-	-	-	DFSDM1_CKIN3	-	-	-	USART3_TX	SPDIF_RX1	-	-	-	FMC_D13	-	-	EVENTOUT
	PD9	-	-	-	DFSDM1_DATAIN3	-	-	-	USART3_RX	-	-	-	-	FMC_D14	-	-	EVENTOUT
	PD10	-	-	-	DFSDM1_CKOUT	-	-	-	USART3_CK	-	-	-	-	FMC_D15	-	LCD_B3	EVENTOUT
	PD11	-	-	-	-	I2C4_SMBA	-	-	USART3_CTS	-	QUADSPI_BK1_IO0	SAI2_SD_A	-	FMC_A16/FMC_CLE	-	-	EVENTOUT
	PD12	-	-	TIM4_CH1	LPTIM1_IN1	I2C4_SCL	-	-	USART3_RTS	-	QUADSPI_BK1_IO1	SAI2_FS_A	-	FMC_A17/FMC_ALE	-	-	EVENTOUT
	PD13	-	-	TIM4_CH2	LPTIM1_OUT	I2C4_SDA	-	-	-	-	QUADSPI_BK1_IO3	SAI2_SCK_A	-	FMC_A18	-	-	EVENTOUT
	PD14	-	-	TIM4_CH3	-	-	-	-	-	UART8_CTS	-	-	-	FMC_D0	-	-	EVENTOUT
	PD15	-	-	TIM4_CH4	-	-	-	-	-	UART8_RTS	-	-	-	FMC_D1	-	-	EVENTOUT
Port E	PE0	-	-	TIM4_ETR	LPTIM1_ETR	-	-	-	-	UART8_Rx	-	SAI2_MCK_A	-	FMC_NBL0	DCMI_D2	-	EVENTOUT
	PE1	-	-	-	LPTIM1_IN2	-	-	-	-	UART8_Tx	-	-	-	FMC_NBL1	DCMI_D3	-	EVENTOUT
	PE2	TRACECLK	-	-	-	-	SPI4_SCK	SAI1_MCLK_A	-	-	QUADSPI_BK1_IO2	-	ETH_MII_TXD3	FMC_A23	-	-	EVENTOUT
	PE3	TRACED0	-	-	-	-	-	SAI1_SD_B	-	-	-	-	-	FMC_A19	-	-	EVENTOUT

Table 12. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM1/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port I	PI12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_HSYNC	EVENTOUT
	PI13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_VSYNC	EVENTOUT
	PI14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_CLK	EVENTOUT
	PI15	-	-	-	-	-	-	-	-	-	LCD_G2	-	-	-	-	LCD_R0	EVENTOUT
Port J	PJ0	-	-	-	-	-	-	-	-	-	LCD_R7	-	-	-	-	LCD_R1	EVENTOUT
	PJ1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R2	EVENTOUT
	PJ2	-	-	-	-	-	-	-	-	-	-	-	-	-	DSI_TE	LCD_R3	EVENTOUT
	PJ3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R4	EVENTOUT
	PJ4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R5	EVENTOUT
	PJ5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R6	EVENTOUT
	PJ6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R7	EVENTOUT
	PJ7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G0	EVENTOUT
	PJ8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G1	EVENTOUT
	PJ9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G2	EVENTOUT
	PJ10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G3	EVENTOUT

Table 34. Typical and maximum current consumption in Sleep mode, regulator OFF

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ		Max(1)						Unit
						TA= 25 °C		TA= 85 °C		TA= 105 °C		
				IDD12	IDD	IDD12	IDD	IDD12	IDD	IDD12	IDD	
IDD12/ IDD	Supply current in RUN mode from V12 and V_{DD} supply	All Peripherals Enabled(2)	180	102	1	114	2	148	2	168	2	mA
			168	91	1	101	2	132	2	152	2	
			144	71	1	78	2	105	2	122	2	
			60	32	1	37	2	64	2	81	2	
			25	16	1	20	2	46	2	64	2	
		All Peripherals Disabled	180	13	1	18	2	53	2	73	2	
			168	12	1	16	2	47	2	67	2	
			144	9	1	13	2	39	2	56	2	
			60	5	1	9	2	35	2	52	2	
			25	3	1	7	2	33	2	50	2	

1. Guaranteed by characterization results, unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.

Table 35. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max(1)			Unit
				V_{DD} = 3.6 V			
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
$I_{DD\_STOP\_NM}$ (normal mode)	Supply current in Stop mode, main regulator in Run mode	Flash memory in Stop mode, all oscillators OFF, no IWDG	0.55	3	18	27	mA
		Flash memory in Deep power down mode, all oscillators OFF	0.5	3	18	27	
	Supply current in Stop mode, main regulator in Low-power mode	Flash memory in Stop mode, all oscillators OFF, no IWDG	0.42	2.5	15	24	
		Flash memory in Deep power down mode, all oscillators OFF, no IWDG	0.37	2.5	15	24	
$I_{DD\_STOP\_UDM}$ (under-drive mode)	Supply current in Stop mode, main regulator in Low voltage and under-drive modes	Regulator in Run mode, Flash memory in Deep power down mode, all oscillators OFF, no IWDG	0.18	1.2	6	10	
		Regulator in Low-power mode, Flash memory in Deep power down mode, all oscillators OFF, no IWDG	0.13	1.1	6	10	

1. Data based on characterization, tested in production.

Table 38. Switching output I/O current consumption(1) (continued)

Symbol	Parameter	Conditions	I/O toggling frequency (fsw) MHz	Typ V_{DD} = 3.3 V	Typ V_{DD} = 1.8 V	Unit
I_{DDIO}	I/O switching Current	C_{EXT} = 22 pF $C = C_{INT} + C_S + C_{EXT}$	2	0.3	0.1	mA
			8	1.0	0.5	
			25	3.5	1.6	
			50	5.9	4.2	
			60	10.0	4.4	
			84	19.12	5.8	
			90	19.6	-	
		C_{EXT} = 33 pF $C = C_{INT} + C_S + C_{EXT}$	2	0.3	0.2	
			8	1.3	0.7	
			25	3.5	2.3	
			50	10.26	5.19	
			60	16.53	-	

1. CINT + C_S, PCB board capacitance including the pad pin is estimated to15 pF.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- I/O compensation cell enabled.
- The ART/L1-cache is ON.
- Scale 1 mode selected, internal digital voltage V12 = 1.32 V.
- HCLK is the system clock. $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
  - f_{HCLK} = 216 MHz (Scale 1 + over-drive ON), f_{HCLK} = 168 MHz (Scale 2), f_{HCLK} = 144 MHz (Scale 3)
- Ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Table 39. Peripheral current consumption

Peripheral		I_{DD}(Typ)[1]			Unit
		Scale 1	Scale 2	Scale 3	
AHB1 (up to 216 MHz)	GPIOA	2.9	2.8	2.2	µA/MHz
	GPIOB	3.0	2.9	2.2	
	GPIOC	2.9	2.8	2.2	
	GPIOD	3.1	3.0	2.3	
	GPIOE	3.1	3.0	2.3	
	GPIOF	2.9	2.8	2.2	
	GPIOG	2.9	2.8	2.2	
	GPIOH	3.1	3.1	2.4	
	GPIOI	3.0	2.9	2.2	
	GPIOJ	2.9	2.9	2.2	
	GPIOK	2.8	2.8	2.4	
	CRC	1.0	0.9	0.8	
	BKPSRAM	0.9	0.9	0.7	
	DMA1	3.17 x N + 11.63	3.08 x N + 11.39	2.6 x N + 9.64	
	DMA2	3.33 x N + 12.84	3.27 x N + 11.84	2.75 x N + 10.10	
	DMA2D	77.7	76.3	63.5	
	ETH_MAC ETH_MAC_TX ETH_MAC_RX ETH_MAC_PTP	40.1	39.5	32.8	
	OTG_HS	58.5	57.4	48.1	
	OTG_HS+ULPI	58.5	57.4	48.1	
AHB2 (up to 216 MHz)	DCMI	2.9	2.8	2.1	µA/MHz
	JPEG	74.8	73.4	61.9	
	RNG	6.7	6.7	5.4	
	USB_OTG_FS	32.4	31.9	26.7	
AHB3 (up to 216 MHz)	FMC	18.6	18.2	15.1	µA/MHz
	QSPI	22.3	21.8	18.1	
Bus matrix[2]		3.94	3.25	2.12	µA/MHz

Table 39. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ)(1)			Unit
		Scale 1	Scale 2	Scale 3	
APB2 (up to 108 MHz)	TIM1	24.1	23.8	19.6	µA/MHz
	TIM8	24.5	24.2	20.0	
	USART1	17.7	17.4	14.3	
	USART6	11.9	11.8	9.4	
	ADC1(5)	4.5	4.7	3.5	
	ADC2(5)	4.5	4.7	3.3	
	ADC3(5)	4.5	4.6	3.3	
	SDMMC1	8.4	8.3	6.9	
	SDMMC2	8.2	8.2	6.4	
	SPI1/I2S1(3)	3.9	3.6	3.1	
	SPI4	3.9	3.6	3.1	
	SYSCFG	2.5	2.2	1.9	
	TIM9	8.0	8.0	6.2	
	TIM10	5.0	5.1	3.7	
	TIM11	6.9	6.9	5.3	
	SPI5	2.7	2.8	1.8	
	SPI6	3.1	3.2	2.2	
	SAI1	3.2	3.3	2.2	
	DFSDM1	10.9	10.7	9.0	
	SAI2	3.9	3.9	2.8	
	MDIO	7.1	7.0	5.8	
	LTDC	51.2	50.3	41.8	
	DSI	8.5	8.4	8.1	

1. When the I/O compensation cell is ON, I_{DD} typical value increases by 0.22 mA.
2. The BusMatrix is automatically active when at least one master is ON.
3. To enable an I2S peripheral, first set the I2SMOD bit and then the I2SE bit in the SPI_I2SCFGR register.
4. When the DAC is ON and EN1/2 bits are set in DAC_CR register, add an additional power consumption of 0.75 mA per DAC channel for the analog part.
5. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

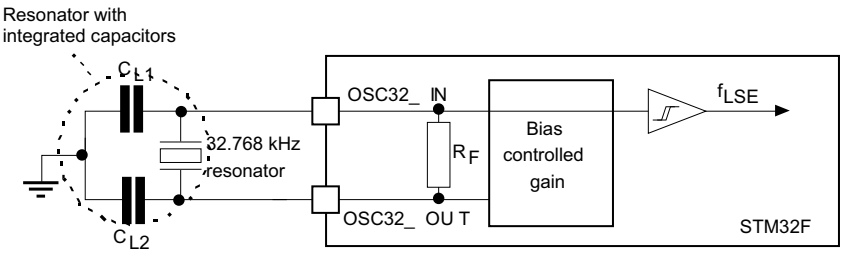
Table 44. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_m_crit_max	Maximum critical crystal g_m	LSEDRV[1:0]=00 Low drive capability	-	-	0.48	µA/V
		LSEDRV[1:0]=10 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0]=01 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0]=11 High drive capability	-	-	2.7	
t_{SU}(2)	start-up time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Guaranteed by characterization results. t_{SU} is the start-up time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 31. Typical application with a 32.768 kHz crystal



5.3.21 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 65: I/O static characteristics*).

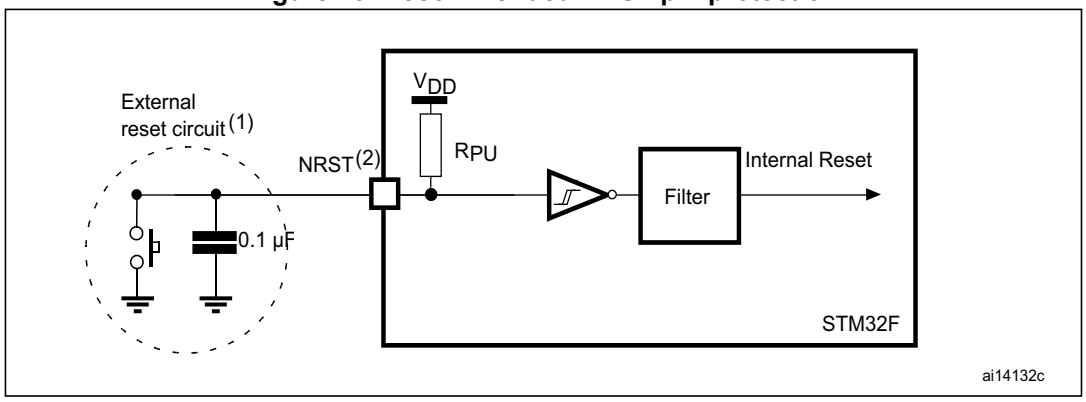
Unless otherwise specified, the parameters given in *Table 68* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 68. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(2)	NRST Input not filtered pulse	$V_{DD} > 2.7$ V	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	µs

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

Figure 40. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 68*. Otherwise the reset is not taken into account by the device.

Table 74. ADC static accuracy at f_{ADC} = 36 MHz

Symbol	Parameter	Test conditions	Typ	Max(1)	Unit
ET	Total unadjusted error	f_{ADC} =36 MHz, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V $V_{DDA} - V_{REF} < 1.2$ V	±4	±7	LSB
EO	Offset error		±2	±3	
EG	Gain error		±3	±6	
ED	Differential linearity error		±2	±3	
EL	Integral linearity error		±3	±6	

1. Guaranteed by characterization results.

Table 75. ADC dynamic accuracy at f_{ADC} = 18 MHz - limited test conditions(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} =18 MHz $V_{DDA} = V_{REF+}$= 1.7 V Input Frequency = 20 KHz Temperature = 25 °C	10.3	10.4	-	bits
SINAD	Signal-to-noise and distortion ratio		64	64.2	-	dB
SNR	Signal-to-noise ratio		64	65	-	
THD	Total harmonic distortion		− 67	− 72	-	

1. Guaranteed by characterization results.

Table 76. ADC dynamic accuracy at f_{ADC} = 36 MHz - limited test conditions(1)

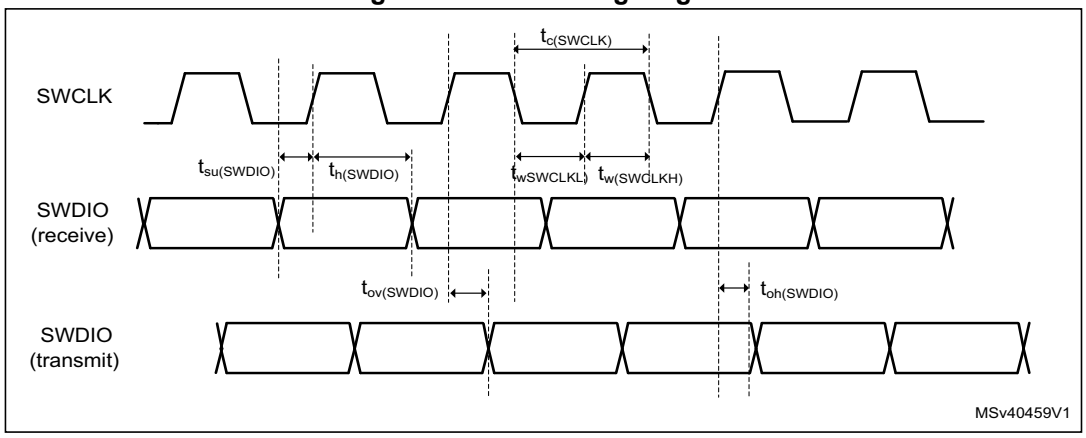
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} =36 MHz $V_{DDA} = V_{REF+}$ = 3.3 V Input Frequency = 20 KHz Temperature = 25 °C	10.6	10.8	-	bits
SINAD	Signal-to noise and distortion ratio		66	67	-	dB
SNR	Signal-to noise ratio		64	68	-	
THD	Total harmonic distortion		− 70	− 72	-	

1. Guaranteed by characterization results.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.20* does not affect the ADC accuracy.

Figure 52. SWD timing diagram



SAI characteristics:

Unless otherwise specified, the parameters given in *Table 89* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: $0.5V_{DD}$

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 89. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	SAI Main clock output	-	256 x 8K	256xFs	MHz
F_{CK}	SAI clock frequency(2)	Master data: 32 bits	-	128xFs(3)	MHz
		Slave data: 32 bits	-	128xFs	
$t_{v(FS)}$	FS valid time	Master mode 2.7≤VDD≤3.6V	-	15	ns
		Master mode 1.71≤VDD≤3.6V	-	20	
$t_{su(FS)}$	FS setup time	Slave mode	7	-	
$t_{h(FS)}$	FS hold time	Master mode	1	-	
		Slave mode	1	-	
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	3	-	
$t_{su(SD\_B\_SR)}$		Slave receiver	3.5	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	5	-	
$t_{h(SD\_B\_SR)}$		Slave receiver	1	-	

Table 100. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$2T_{HCLK} - 1$	$2 T_{HCLK} +1$	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	0.5	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{HCLK} - 1$	$2T_{HCLK} + 1$	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL\_NOE)}$	FMC_BL hold time after FMC_NOE high	0	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	$T_{HCLK} - 1$	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	$T_{HCLK} - 1$	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{HCLK} + 1$	

1. C_L = 30 pF.
2. Guaranteed by characterization results.

Table 101. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$7T_{HCLK} +1$	$7T_{HCLK} +1$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK} -1$	$5T_{HCLK} +1$	
$t_{w(NWAIT)}$	FMC_NWAIT low time	$T_{HCLK} -0.5$		
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK} +1.5$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}+1$	-	

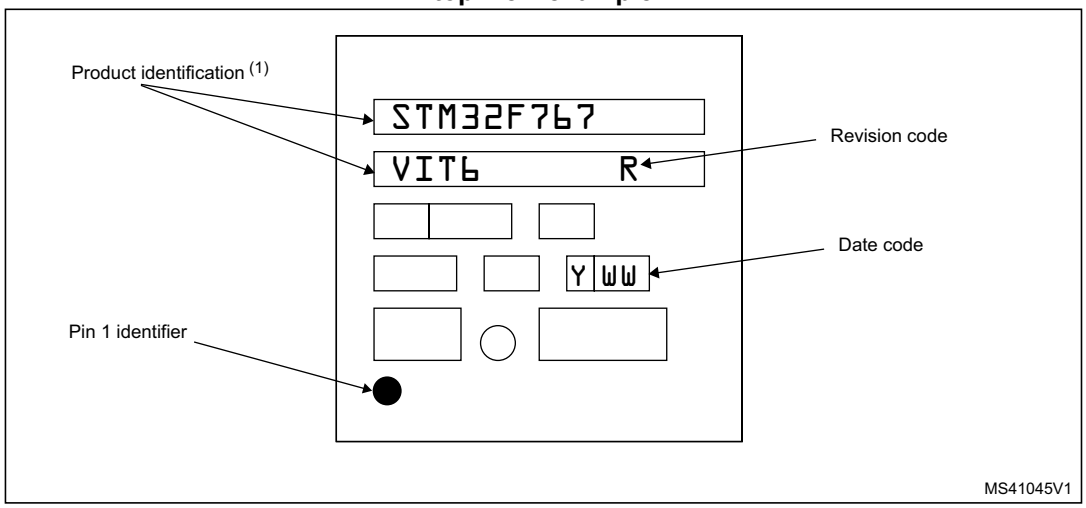
1. Guaranteed by characterization results.

LQFP100 device making

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

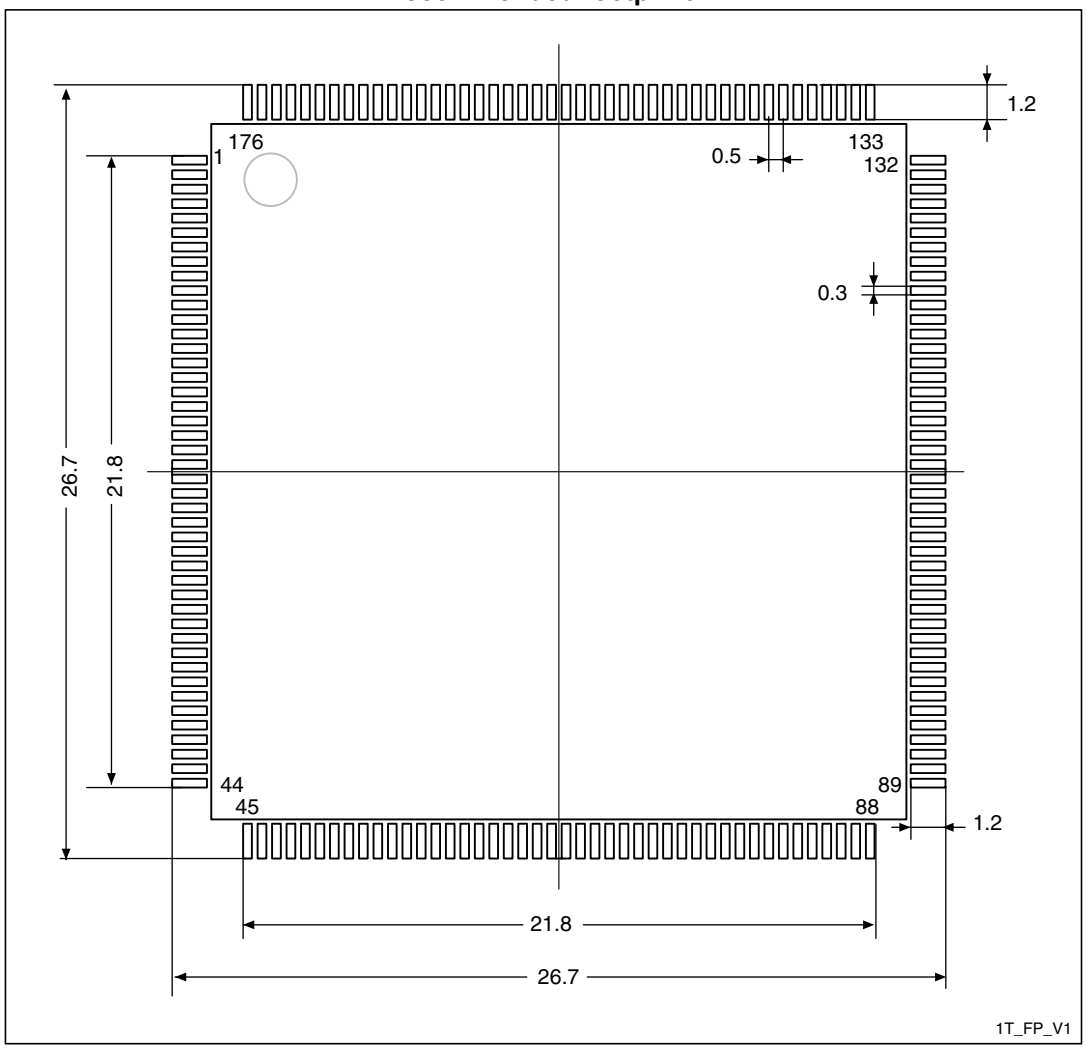
Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 85. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Figure 90. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.