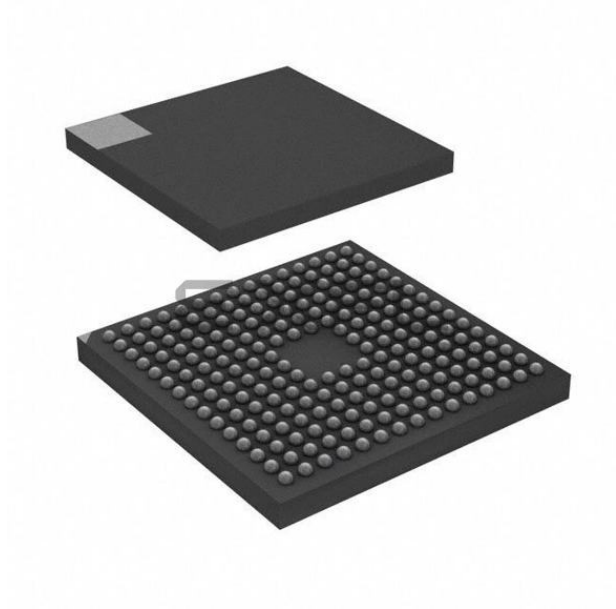

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	168
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	216-TFBGA
Supplier Device Package	216-TFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f765ngh7

The STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx devices offer devices in 10 packages ranging from 100 pins to 216 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile applications, Internet of Things
- Wearable devices: smartwatches.

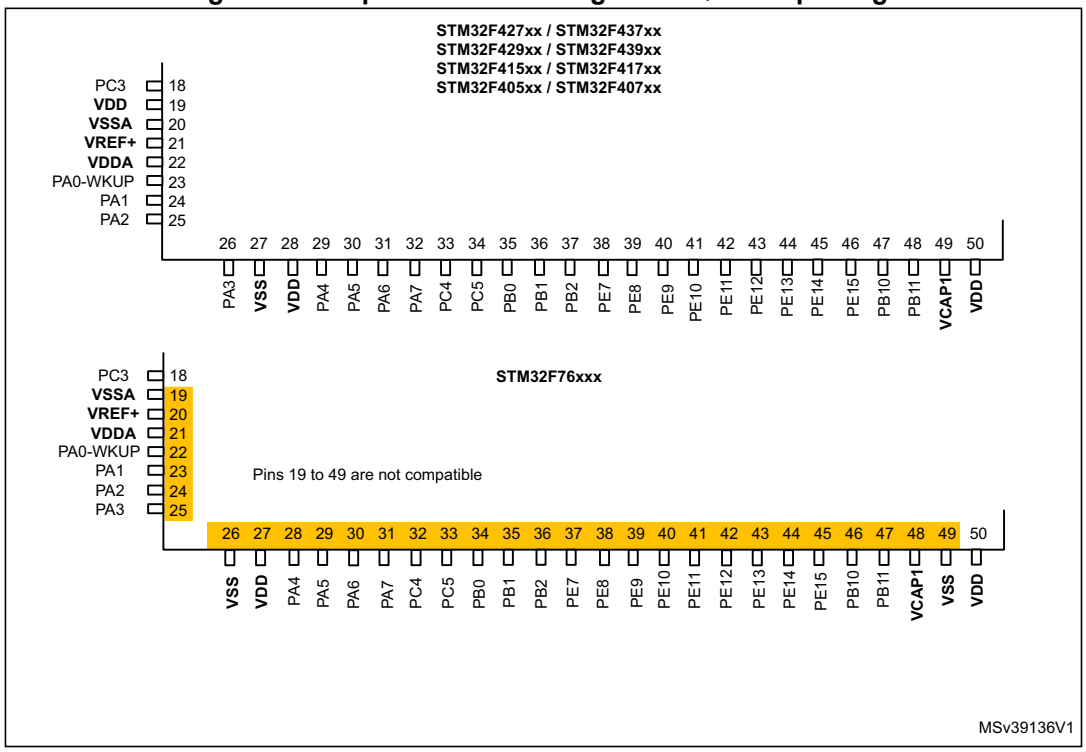
Figure 2 shows the general block diagram of the device family

1.1 Full compatibility throughout the family

The STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx devices are fully pin-to-pin, compatible with the STM32F4xxxx devices, allowing the user to try different peripherals, and reaching higher performances (higher frequency) for a greater degree of freedom during the development cycle.

Figure 1 gives compatible board designs between the STM32F7xx and STM32F4xx families.

Figure 1. Compatible board design for LQFP100 package



The STM32F76x LQFP144, LQFP176, LQFP208, TFBGA216, UFBGA176 packages are fully pin to pin compatible with STM32F4xx devices.

The devices embed two dedicated PLL (PLLI2S and PLLSAI) which allow to achieve audio class performance. In this case, the I^2S and SAI master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

2.16 Boot modes

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDx option bytes, allowing to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF which includes:

- All Flash address space mapped on ITCM or AXIM interface
- All RAM address space: ITCM, DTCM RAMs and SRAMs mapped on AXIM interface
- The System memory bootloader

The boot loader is located in system memory. It is used to reprogram the Flash memory through a serial interface. Refer to *STM32 microcontroller system memory boot mode* application note (AN2606) for details.

2.17 Power supply schemes

- V_{DD} = 1.7 to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.7 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Note: V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the internal reset is OFF (refer to Section 2.18.2: Internal reset OFF). Refer to Table 3: Voltage regulator configuration mode versus device operating mode to identify the packages supporting this option.

- $V_{DDSDMMC}$ can be connected either to V_{DD} or an external independent power supply (1.8 to 3.6V) for SDMMC2 pins (clock, command, and 4-bit data). For example, when the device is powered at 1.8V, an independent power supply 2.7V can be connected to $V_{DDSDMMC}$.When the $V_{DDSDMMC}$ is connected to a separated power supply, it is independent from V_{DD} or V_{DDA} but it must be the last supply to be provided and the first to disappear. The following conditions $V_{DDSDMMC}$ must be respected:
  - During the power-on phase ($V_{DD} < V_{DD\_MIN}$), $V_{DDSDMMC}$ should be always lower than V_{DD}
  - During the power-down phase ($V_{DD} < V_{DD\_MIN}$), $V_{DDSDMMC}$ should be always lower than V_{DD}
  - The $V_{DDSDMMC}$ rising and falling time rate specifications must be respected (see *Table 20* and *Table 21*)
  - In operating mode phase, $V_{DDSDMMC}$ could be lower or higher than V_{DD}: All associated GPIOs powered by $V_{DDSDMMC}$ are operating between $V_{DDSDMMC\_MIN}$ and $V_{DDSDMMC\_MAX}$.
- V_{DDUSB} can be connected either to V_{DD} or an external independent power supply (3.0 to 3.6V) for USB transceivers (refer to *Figure 4* and *Figure 5*). For example, when the device is powered at 1.8V, an independent power supply 3.3V can be connected to V_{DDUSB}. When the V_{DDUSB} is connected to a separated power supply, it is independent from V_{DD} or V_{DDA} but it must be the last supply to be provided and the first to

2.31 SD/SDIO/MMC card host interface (SDMMC)

SDMMC host interfaces are available, that support the MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 50 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDMMC Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDMMC/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

The SDMMC can be served by the DMA controller

2.32 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

2.44 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- Two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

2.45 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.46 Embedded Trace Macrocell™

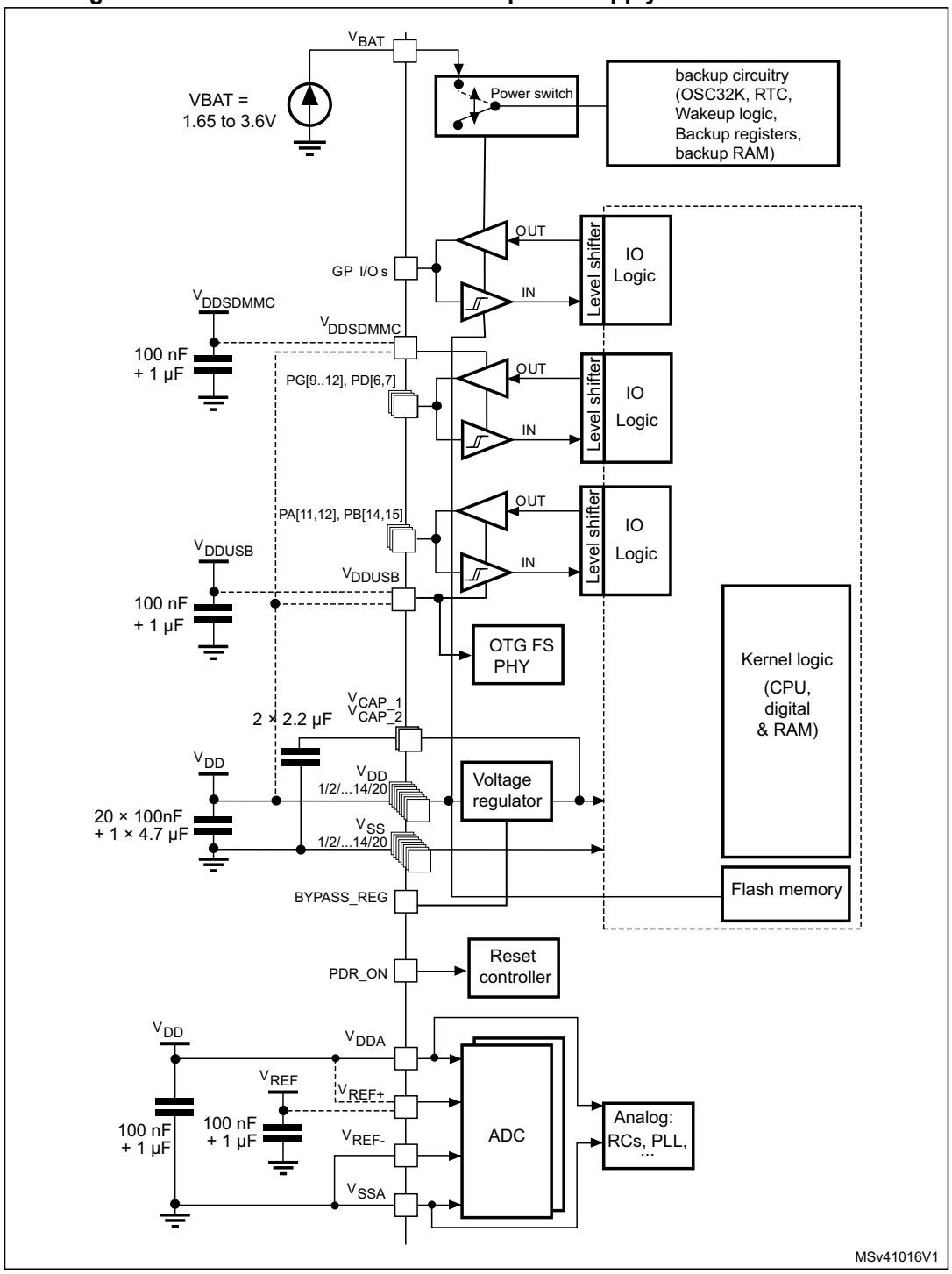
The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F76xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	-	K12	89	102	M15	P3	-	102	M15	PH12	I/O	FT	-	TIM5_CH3, I2C4_SDA, FMC_D20, DCMI_D3, LCD_R6, EVENTOUT	-
-	-	H12	90	-	K10	N4	-	-	K10	VSS	S		-	-	-
-	-	J12	91	103	K11	-	-	103	K11	VDD	S		-	-	-
51	73	P12	92	104	L13	H8	85	104	L13	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, DFSDM1_DATIN1, USART3_CK, UART5_RX, CAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_RMII_TXD0, OTG_HS_ID, EVENTOUT	-
52	74	P13	93	105	K14	J5	86	105	K14	PB13	I/O	FT	-	TIM1_CH1N, SPI2_SCK/I2S2_CK, DFSDM1_CKIN1, USART3_CTS, UART5_TX, CAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, EVENTOUT	OTG_HS_VBUS
53	75	R14	94	106	R14	N3	87	106	R14	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, USART1_TX, SPI2_MISO, DFSDM1_DATIN2, USART3_RTS, UART4_RTS, TIM12_CH1, SDMMC2_D0, OTG_HS_DM, EVENTOUT	-
54	76	R15	95	107	R15	N2	88	107	R15	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, USART1_RX, SPI2_MOSI/I2S2_SD, DFSDM1_CKIN2, UART4_CTS, TIM12_CH2, SDMMC2_D1, OTG_HS_DP, EVENTOUT	-

Figure 25. STM32F767xx/STM32F777xx power supply scheme



1. To connect BYPASS_REG and PDR_ON pins, refer to *Section 2.18: Power supply supervisor* and *Section 2.19: Voltage regulator*.
2. The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors when the voltage regulator is OFF.
3. The 4.7 µF ceramic capacitor must be connected to one of the V_{DD} pin.
4. V_{DDA}=V_{DD} and V_{SSA}=V_{SS}.

Table 22. Reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	V
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	V
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	V
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	V
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	V
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	V
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	V
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	V
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	V
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	V
		PLS[2:0]=101 (falling edge)	2.65	2.84	2.92	V
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	V
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	V
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	V
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	V
$V_{PVDhyst}$(1)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.60	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	V
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	40	-	mV
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	V
V_{BOR2}	Brownout level 2 threshold	Falling edge	2.44	2.50	2.56	V
		Rising edge	2.53	2.59	2.63	V
V_{BOR3}	Brownout level 3 threshold	Falling edge	2.75	2.83	2.88	V
		Rising edge	2.85	2.92	2.97	V
$V_{BORhyst}$(1)	BOR hysteresis	-	-	100	-	mV
$T_{RSTTEMPO}$(1)(2)	POR reset temporization	-	0.5	1.5	3.0	ms
I_{RUSH}(1)	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	-	160	250	mA
E_{RUSH}(1)	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	V_{DD} = 1.7 V, T_A = 105 °C, I_{RUSH} = 171 mA for 31 µs	-	-	5.4	µC

Table 27. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (Single bank mode) or SRAM on AXI (L1-cache disabled), regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					TA= 25 °C	TA=85 °C	TA=105 °C	
I_{DD}	Supply current in RUN mode	All peripherals enabled(2)(3)	216	190	209	255	-	mA
			200	177	194	241	268	
			180	160	175	211	232	
			168	144	156	189	209	
			144	115	125	152	170	
			60	56	62	89	107	
			25	27	32	59	79	
		All peripherals disabled(3)	216	92	103	150	-	
			200	86	96	243	171	
			180	79	87	123	144	
			168	71	79	111	131	
			144	60	65	92	110	
			60	32	36	63	80	
			25	16	20	46	64	

1. Guaranteed by characterization results, unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 30. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (Dual bank mode) on ITCM interface (ART disabled), regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					TA= 25 °C	TA=85 °C	TA=105 °C	
I_{DD}	Supply current in RUN mode	All peripherals enabled(2)(3)	216	191	218	255	-	mA
			200	178	195	241	269	
			180	164	179	214	236	
			168	147	160	192	212	
			144	121	130	157	175	
			60	60	66	93	111	
			25	28	33	59	77	
		All peripherals disabled(3)	216	93	104	150	-	
			200	87	97	144	171	
			180	83	92	126	148	
			168	75	82	114	134	
			144	65	71	97	115	
			60	35	40	66	84	
			25	16	20	47	64	

1. Guaranteed by characterization results, unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

5.3.10 Internal clock source characteristics

The parameters given in *Table 45* and *Table 46* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

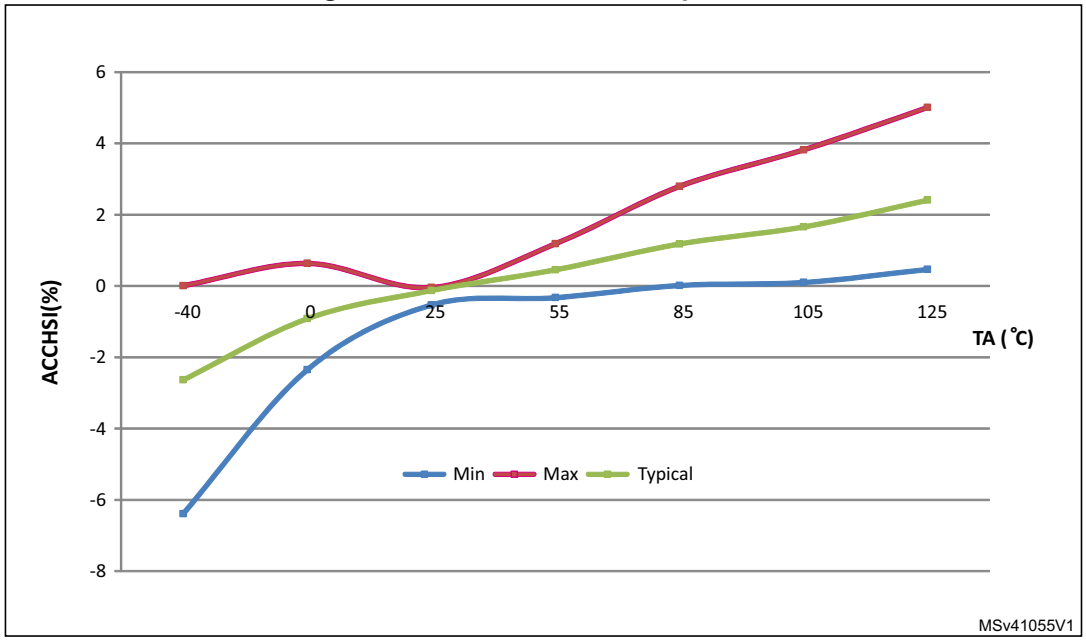
High-speed internal (HSI) RC oscillator

Table 45. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	HSI user trimming step(2)	-	-	-	1	%
	Accuracy of the HSI oscillator	T_A = –40 to 105 °C(3)	− 8	-	4.5	%
		T_A = –10 to 85 °C(3)	− 4	-	4	%
		T_A = 25 °C(4)	− 1	-	1	%
$t_{su(HSI)}$(2)	HSI oscillator startup time	-	-	2.2	4	µs
$I_{DD(HSI)}$(2)	HSI oscillator power consumption	-	-	60	80	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Factory calibrated, parts not soldered.

Figure 32. ACCHSI versus temperature



1. Guaranteed by characterization results.

Table 51. MIPI D-PHY characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Output low level voltage	-	1.1	1.2	1.2	V
$V_{IL-ULPS}$	Output high level voltage	-	-50	-	50	mV
V_{IH}	Output impedance of LP transmitter	-	110	-	-	Ω
V_{hys}	15%-85% rise and fall time	-	-	-	25	ns
LP Contention Detector Characteristics						
V_{ILCD}	Logic 0 contention threshold	-	-	-	200	mV
V_{IHCD}	Logic 0 contention threshold	-	450	-	-	

1. Guaranteed based on test during characterization.

Table 52. MIPI D-PHY AC characteristics LP mode and HS/LP transitions(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{LPX}	Transmitted length of any Low-Power state period	-	50	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	-	38	-	95	
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Time that the transmitter drives the HS-0 state prior to starting the clock.	-	300	-	-	
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	-	8	-	-	UI

Table 56. Flash memory programming (single bank configuration nDBANK=1) (continued)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{prog}	Programming voltage	32-bit program operation	2.7	-	3	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.7	-	3.6	V

1. Guaranteed by characterization results.
2. The maximum programming time is measured after 100K erase operations.

Table 57. Flash memory programming (dual bank configuration nDBANK=0)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	250	600	
		Program/erase parallelism (PSIZE) = x 32	-	200	500	
$t_{ERASE64KB}$	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1100	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	800	1400	
		Program/erase parallelism (PSIZE) = x 32	-	500	1100	
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2.1	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.5	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t_{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	16	32	s
		Program/erase parallelism (PSIZE) = x 16	-	11	22	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 61. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}] 8/200 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, TFBGA216 package, conforming to IEC61967-2 ART/L1-cache ON, over-drive ON, all peripheral clocks enabled, clock dithering disabled.	0.1 to 30 MHz	5	dBµV
			30 to 130 MHz	10	
			130 MHz to 1 GHz	18	
			1 GHz to 2 GHz	10	
			EMI Level	3.5	-
		V_{DD} = 3.6 V, T_A = 25 °C, TFBGA216 package, conforming to IEC61967-2 ART/L1-cache ON, over-drive ON, all peripheral clocks enabled, clock dithering enabled.	0.1 to 30 MHz	2	dBµV
			30 to 130 MHz	9	
			130 MHz to 1 GHz	14	
			1 GHz to 2 GHz	9	
			EMI Level	3	-

5.3.18 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/ESDA/JEDEC JS-001-2012 and ANSI/ESD S5.3.1-2009 standards.

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 85* for the SPI interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 85. SPI dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode SPI1,4,5,6 2.7≤VDD≤3.6	-	-	54(2)	MHz
		Master mode SPI1,4,5,6 1.71≤VDD≤3.6			27	
		Master transmitter mode SPI1,4,5,6 1.71≤VDD≤3.6			54	
		Slave receiver mode SPI1,4,5,6 1.71≤VDD≤3.6			54	
		Slave mode transmitter/full duplex SPI1,4,5,6 2.7≤VDD≤3.6			50(3)	
		Slave mode transmitter/full duplex SPI1,4,5,6 1.71≤VDD≤3.6			37(3)	
		Master & Slave mode SPI2,3 1.71≤VDD≤3.6			27	
tsu(NSS)	NSS setup time	Slave mode, SPI presc = 2	$4*T_{PLCK}$	-	-	ns
th(NSS)	NSS hold time	Slave mode, SPI presc = 2	$2*T_{PLCK}$	-	-	
tw(SCKH) tw(SCKL)	SCK high and low time	Master mode	$T_{PLCK} - 2$	T_{PLCK}	$T_{PLCK} + 2$	

Table 89. SAI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge) 2.7≤VDD≤3.6V	-	12	ns
		Slave transmitter (after enable edge) 1.71≤VDD≤3.6V	-	20	
$t_{h(SD\_B\_MT)}$	Data output hold time	Slave transmitter (after enable edge)	5	-	
$t_{v(SD\_MT)\_A}$	Data output valid time	Master transmitter (after enable edge) 2.7≤VDD≤3.6V	-	15	
		Master transmitter (after enable edge) 1.71≤VDD≤3.6V	-	20	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	5	-	

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.
3. With F_S=192kHz.

Figure 53. SAI master timing waveforms

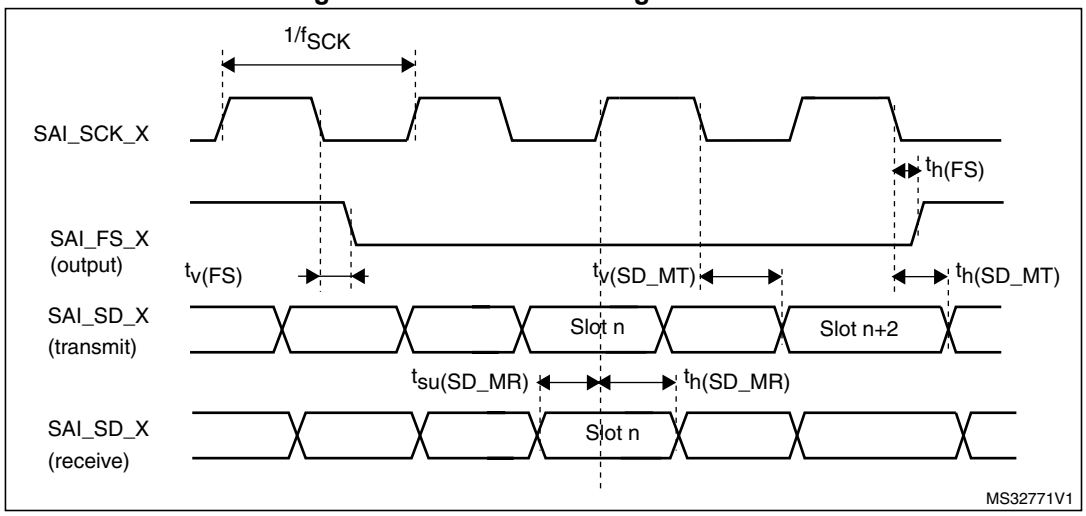


Table 118. Quad-SPI characteristics (continued)in SDR mode(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tw(CKH)	Quad-SPI clock high and low time	-	t(CK)/2 - 1	-	t(CK)/2	ns
tw(CKL)			t(CK)/2	-	t(CK)/2 + 1	
ts(IN)	Data input setup time	-	0.5	-	-	
th(IN)	Data input hold time		3	-	-	
tv(OUT)	Data output valid time	2.7 V<V_{DD}<3.6 V	-	1.5	3.5	
		1.71 V<V_{DD}<3.6 V	-	1.5	2	
th(OUT)	Data output hold time	-	0.5	-	-	

1. Guaranteed by characterization results.

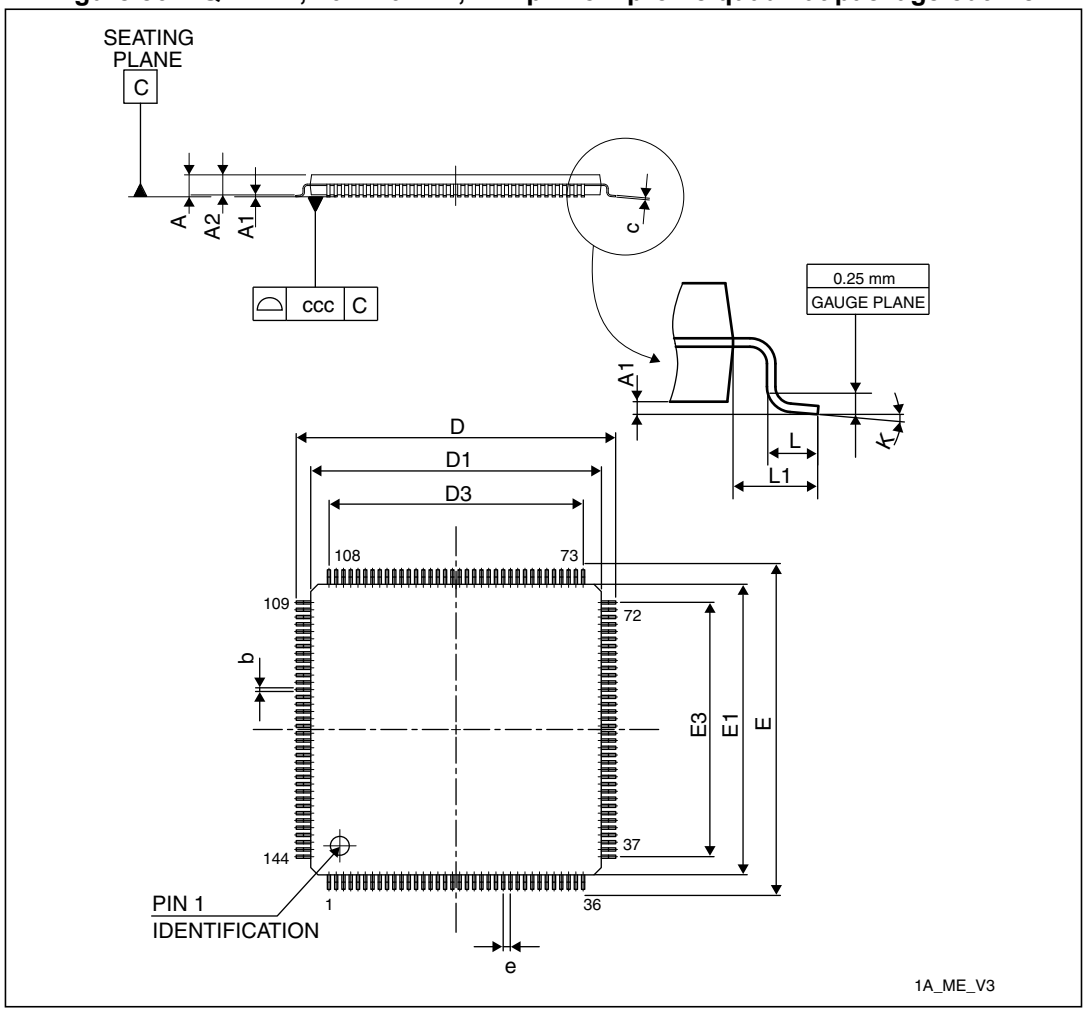
Table 119. Quad SPI characteristics in DDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Fck1/t(CK)	Quad-SPI clock frequency	2.7 V<V_{DD}<3.6 V CL=20 pF	-	-	80	MHz
		1.8 V<V_{DD}<3.6 V CL=15 pF	-	-	80	
		1.71 V<V_{DD}<3.6 V CL=10 pF	-	-	80	
tw(CKH)	Quad-SPI clock high and low time	-	t(CK)/2 - 1	-	t(CK)/2	ns
tw(CKL)			t(CK)/2	-	t(CK)/2 + 1	
ts(IN), tsf(IN)	Data input setup time	2.7 V<V_{DD}<3.6 V	0.75	-	-	
		1.71 V<V_{DD}<2 V	0.5	-	-	
thr(IN), thf(IN)	Data input hold time	2.7 V<V_{DD}<3.6 V	2	-	-	
		1.71 V<V_{DD}<2 V	3	-	-	
tvr(OUT), tvf(OUT)	Data output valid time	2.7 V<V_{DD}<3.6 V	-	8.5	10	
		1.71 V<V_{DD}<3.6 V DHHC=0	-	8	12	
		DHHC=1 Pres=1, 2...	-	T_{HCLK}/2 + 1.5	T_{HCLK}/2 + 2.5	
thr(OUT), thf(OUT)	Data output hold time	DHHC=0	7.5	-	-	
		DHHC=1 Pres=1, 2...	T_{HCLK}/2 + 0.5	-	-	

1. Guaranteed by characterization results.

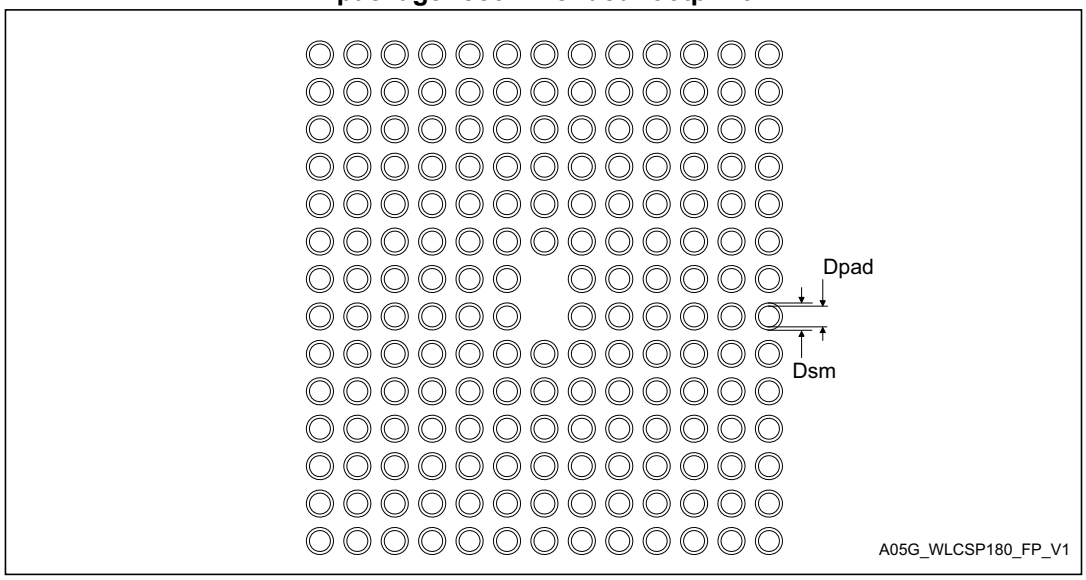
6.2 LQFP144 20 x 20 mm, low-profile quad flat package information

Figure 86. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline



1. Drawing is not to scale.

Figure 96. WLCSP 180-bump, 5.5 x 6 mm, 0.4 mm pitch wafer level chip scale package recommended footprint



1. Dimensions are expressed in millimeters.

Table 130. WLCSP 180-bump, 5.5 x 6 mm, recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.1 mm