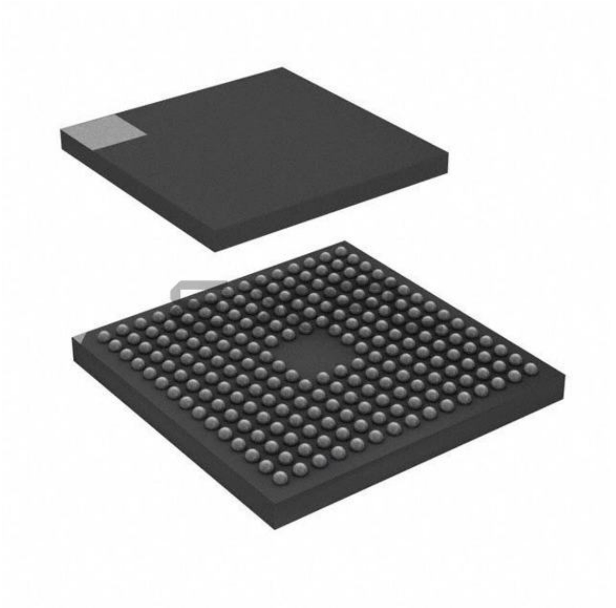

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	168
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	216-TFBGA
Supplier Device Package	216-TFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f765ngh7tr

- LPR is used in the Stop modes:
  The LP regulator mode is configured by software when entering Stop mode.
  Like the MR mode, the LPR can be configured in two ways during stop mode:
  - LPR operates in normal mode (default mode when LPR is ON)
  - LPR operates in under-drive mode (reduced leakage mode).
- Power-down is used in Standby mode.
  The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Refer to *Table 3* for a summary of voltage regulator modes versus device operating modes.

Two external ceramic capacitors should be connected on V_{CAP_1} and V_{CAP_2} pin.

All packages have the regulator ON feature.

Table 3. Voltage regulator configuration mode versus device operating mode(1)

Voltage regulator configuration	Run mode	Sleep mode	Stop mode	Standby mode
Normal mode	MR	MR	MR or LPR	-
Over-drive mode(2)	MR	MR	-	-
Under-drive mode	-	-	MR or LPR	-
Power-down mode	-	-	-	Yes

1. '-' means that the corresponding configuration is not available.
2. The over-drive mode is not available when V_{DD} = 1.7 to 2.1 V.

2.19.2 Regulator OFF

This feature is available only on packages featuring the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a V_{12} voltage source through V_{CAP_1} and V_{CAP_2} pins.

Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency.The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors.

When the regulator is OFF, there is no more internal monitoring on V_{12}. An external power supply supervisor should be used to monitor the V_{12} of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V_{12} power domain.

In the regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V_{12} logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The over-drive and under-drive modes are not available.
- The Standby mode is not available.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator(LSE)
- The internal low power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32

The RTC is functional in V_{BAT} mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in V_{BAT} mode, but is functional in all low-power modes.

All RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

2.21 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

  The voltage regulator can be put either in main regulator mode (MR) or in low-power mode (LPR). Both modes can be configured as follows (see *Table 5: Voltage regulator modes in stop mode*):

  – Normal mode (default mode when MR or LPR is enabled)

  – Under-drive mode.

  The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup and LPTIM1 asynchronous interrupt).

Table 5. Voltage regulator modes in stop mode

Voltage regulator configuration	Main regulator (MR)	Low-power regulator (LPR)
Normal mode	MR ON	LPR ON
Under-drive mode	MR in under-drive mode	LPR in under-drive mode

- **Standby mode**

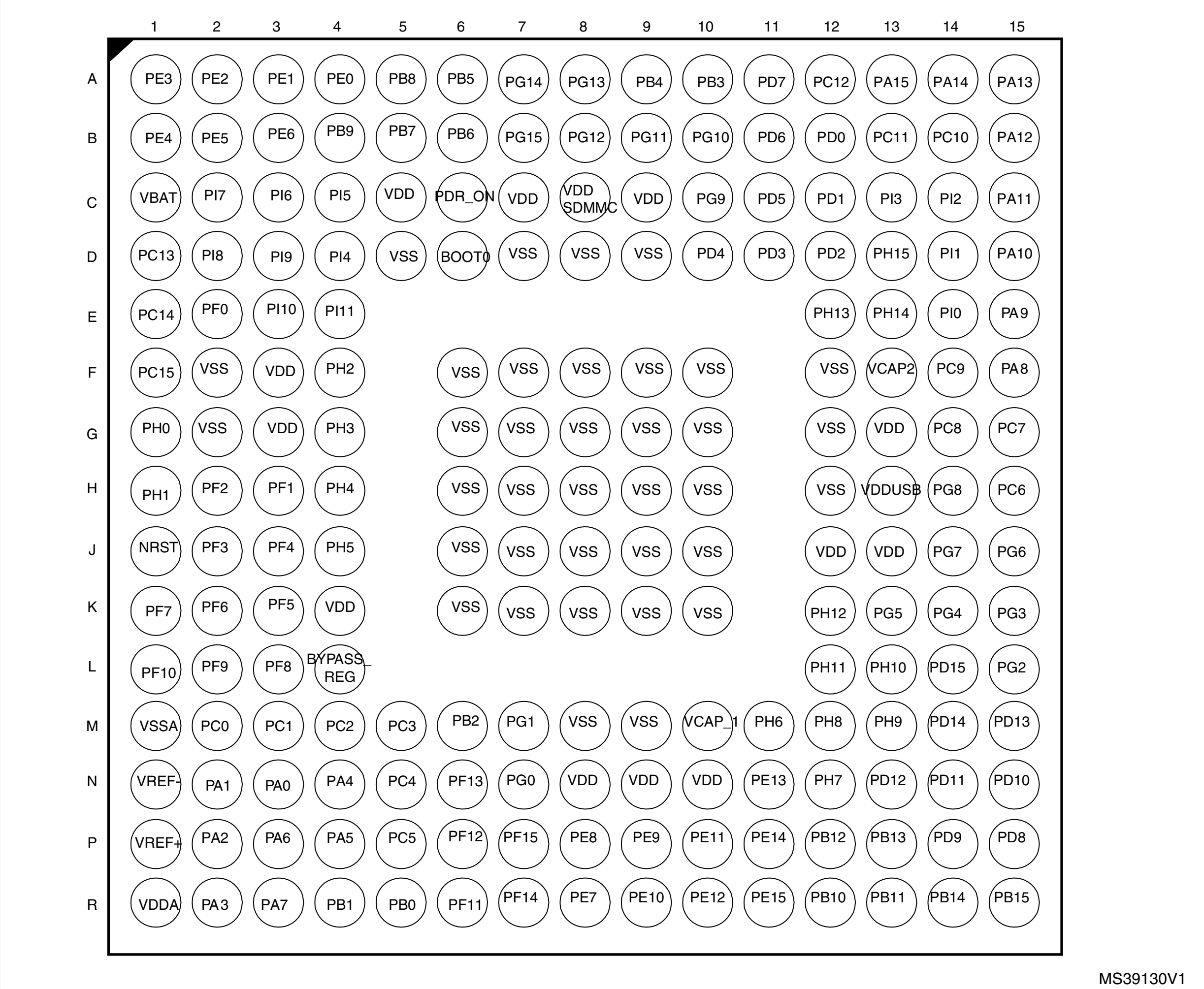
  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering

Table 6. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complem entary output	Max interface clock (MHz)	Max timer clock (MHz)(1)
Advanced -control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	108	216
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	54	108/216
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	54	108/216
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	108	216
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	108	216
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	54	108/216
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	54	108/216
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	54	108/216

1. The maximum timer clock is either 108 or 216 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

Figure 18. STM32F76xxx UFBGA176 ballout



1. The above figure shows the package top view.

Table 9. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TTa	3.3 V tolerant I/O directly connected to ADC
	B	Dedicated BOOT pin
	RST	Bidirectional reset pin with weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[(1)]	LQFP176	LQFP208	TFBGA216						
1	1	A2	1	1	A3	E10	1	1	A3	PE2	I/O	FT	-	TRACECLK, SPI4_SCK, SAI1_MCLK_A, QUADSPI_BK1_IO2, ETH_MII_TXD3, FMC_A23, EVENTOUT	-
2	2	A1	2	2	A2	F10	2	2	A2	PE3	I/O	FT	-	TRACED0, SAI1_SD_B, FMC_A19, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180(1)	LQFP176	LQFP208	TFBGA216						
17	28	M4	34	37	M4	NC	34	37	M4	PC2	I/O	FT	-	DFSDM1_CKIN1, SPI2_MISO, DFSDM1_CKOUT, OTG_HS_ULPI_DIR, ETH_MII_TXD2, FMC_SDNE0, EVENTOUT	ADC1_IN12, ADC2_IN12, ADC3_IN12
18	29	M5	35	38	L4	NC	35	38	L4	PC3	I/O	FT	-	DFSDM1_DATIN1, SPI2_MOSI/I2S2_SD, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, FMC_SDCKE0, EVENTOUT	ADC1_IN13, ADC2_IN13, ADC3_IN13
-	30	-	36	39	J5	-	36	39	J5	VDD	S	-	-	-	-
-	-	-	-	-	J6	-	-	-	J6	VSS	S	-	-	-	-
19	31	M1	37	40	M1	M11	37	40	M1	VSSA	S	-	-	-	-
-	-	N1	-	-	N1	-	-	-	N1	VREF-	S	-	-	-	-
20	32	P1	38	41	P1	-	38	41	P1	VREF+	S	-	-	-	-
21	33	R1	39	42	R1	M12	39	42	R1	VDDA	S	-	-	-	-
22	34	N3	40	43	N3	M13	40	43	N3	PA0-WKUP	I/O	FT	(4)	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, SAI2_SD_B, ETH_MII_CRS, EVENTOUT	ADC1_IN0, ADC2_IN0, ADC3_IN0, WKUP1
23	35	N2	41	44	N2	J11	41	44	N2	PA1	I/O	FT	-	TIM2_CH2, TIM5_CH2, USART2_RTS, UART4_RX, QUADSPI_BK1_IO3, SAI2_MCLK_B, ETH_MII_RX_CLK/ETH_RMII_REF_CLK, LCD_R2, EVENTOUT	ADC1_IN1, ADC2_IN1, ADC3_IN1

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
65	98	G14	117	140	G14	G8	121	140	G14	PC8	I/O	FT	-	TRACED1, TIM3_CH3, TIM8_CH3, UART5_RTS, USART6_CK, FMC_NE2/FMC_NCE, SDMMC1_D0, DCMI_D2, EVENTOUT	
66	99	F14	118	141	F14	E1	122	141	F14	PC9	I/O	FT	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, LCD_G3, SDMMC1_D1, DCMI_D3, LCD_B2, EVENTOUT	--
67	100	F15	119	142	F15	E2	123	142	F15	PA8	I/O	FT	-	MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, CAN3_RX, UART7_RX, LCD_B3, LCD_R6, EVENTOUT	-
68	101	E15	120	143	E15	F4	124	143	E15	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, DCMI_D0, LCD_R5, EVENTOUT	OTG_FS_VBUS
69	102	D15	121	144	D15	F5	125	144	D15	PA10	I/O	FT	-	TIM1_CH3, USART1_RX, LCD_B4, OTG_FS_ID, MDIOS_MDIO, DCMI_D1, LCD_B1, EVENTOUT	-
70	103	C15	122	145	C15	E3	126	145	C15	PA11	I/O	FT	-	TIM1_CH4, SPI2_NSS/I2S2_WS, UART4_RX, USART1_CTS, CAN1_RX, OTG_FS_DM, LCD_R4, EVENTOUT	-

Table 12. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM1/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port A	PA11	-	TIM1_CH4	-	-	-	SPI2_NSS/I2S2_WS	UART4_RX	USART1_CTS	-	CAN1_RX	OTG_FS_DM	-	-	-	LCD_R4	EVENTOUT
	PA12	-	TIM1_ETR	-	-	-	SPI2_SCK/I2S2_CK	UART4_TX	USART1_RTS	SAI2_FS_B	CAN1_TX	OTG_FS_DP	-	-	-	LCD_R5	EVENTOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM2_CH1/TIM2_ETR	-	-	HDMI-CEC	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	SPI6_NSS	UART4_RTS	-	-	CAN3_TX	UART7_TX	-	-	EVENTOUT
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	DFSDM1_CKOUT	-	UART4_CTS	LCD_R3	OTG_HS_ULPI_D1	ETH_MII_RXD2	-	-	LCD_G1	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	DFSDM1_DATIN1	-	-	LCD_R6	OTG_HS_ULPI_D2	ETH_MII_RXD3	-	-	LCD_G0	EVENTOUT
	PB2	-	-	-	-	-	-	SAI1_SD_A	SPI3_MOSI/I2S3_SD		QUADSPI_CLK	DFSDM1_CKIN1	-	-	-	-	EVENTOUT
	PB3	JTDO/TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	-	SPI6_SCK	-	SDMMC2_D2	CAN3_RX	UART7_RX	-	-	EVENTOUT
	PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	SPI2_NSS/I2S2_WS	SPI6_MISO	-	SDMMC2_D3	CAN3_TX	UART7_TX	-	-	EVENTOUT
	PB5	-	UART5_RX	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI/I2S1_SD	SPI3_MOSI/I2S3_SD	-	SPI6_MOSI	CAN2_RX	OTG_HS_ULPI_D7	ETH_PPS_OUT	FMC_SDCKE1	DCMI_D10	LCD_G7	EVENTOUT
	PB6	-	UART5_TX	TIM4_CH1	HDMI-CEC	I2C1_SCL	-	DFSDM1_DATIN5	USART1_TX	-	CAN2_TX	QUADSPI_BK1_NCS	I2C4_SCL	FMC_SDNE1	DCMI_D5	-	EVENTOUT

Table 13. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx register boundary addresses[(1)] (continued)

Bus	Boundary address	Peripheral
	0x4000 8000- 0x4000 FFFF	Reserved
APB1	0x4000 7C00 - 0x4000 7FFF	UART8
	0x4000 7800 - 0x4000 7BFF	UART7
	0x4000 7400 - 0x4000 77FF	DAC
	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6C00 - 0x4000 6FFF	HDMI-CEC
	0x4000 6800 - 0x4000 6BFF	CAN2
	0x4000 6400 - 0x4000 67FF	CAN1
	0x4000 6000 - 0x4000 63FF	I2C4
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 5000 - 0x4000 53FF	UART5
	0x4000 4C00 - 0x4000 4FFF	UART4
	0x4000 4800 - 0x4000 4BFF	USART3
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	SPDIFRX
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	CAN3
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 2400 - 0x4000 27FF	LPTIM1
	0x4000 2000 - 0x4000 23FF	TIM14
	0x4000 1C00 - 0x4000 1FFF	TIM13
	0x4000 1800 - 0x4000 1BFF	TIM12
	0x4000 1400 - 0x4000 17FF	TIM7
	0x4000 1000 - 0x4000 13FF	TIM6
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2

1. The gray color is used for reserved Flash memory addresses.

Table 28. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (Dual bank mode), regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					TA= 25 °C	TA=85 °C	TA=105 °C	
I_{DD}	Supply current in RUN mode	All peripherals enabled(2)(3)	216	176	194	240	-	mA
			200	164	181	227	255	
			180	149	163	198	220	
			168	133	145	178	198	
			144	106	116	143	161	
			60	54	60	87	105	
			25	27	31	58	76	
		All peripherals disabled(3)	216	77	88	135	-	
			200	72	82	129	157	
			180	67	75	110	131	
			168	60	67	99	120	
			144	50	56	83	101	
			60	29	34	60	78	
			25	15	19	45	63	

1. Guaranteed by characterization results, unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 36. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions	Typ(1)			Max(2)			Unit
			T_A = 25 °C			T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
			V_{DD} = 1.7 V	V_{DD}= 2.4 V	V_{DD} = 3.3 V	V_{DD} = 3.3 V			
I_{DD_STBY}	Supply current in Standby mode	Backup SRAM OFF, RTC and LSE OFF	1.1	1.9	2.4	5(3)	18(3)	38(3)	µA
		Backup SRAM ON, RTC and LSE OFF	1.9	2.7	3.2	6(3)	23(3)	48(3)	
		Backup SRAM OFF, RTC ON and LSE in low drive mode	1.7	2.7	3.5	7	26	55	
		Backup SRAM OFF, RTC ON and LSE in medium low drive mode	1.7	2.7	3.5	7	26	56	
		Backup SRAM OFF, RTC ON and LSE in medium high drive mode	1.8	2.8	3.6	8	28	57	
		Backup SRAM OFF, RTC ON and LSE in high drive mode	1.9	2.9	3.7	8	28	59	
		Backup SRAM ON, RTC ON and LSE in low drive mode	2.4	3.4	4.3	8	31	65	
		Backup SRAM ON, RTC ON and LSE in Medium low drive mode	2.4	3.5	4.3	8	31	65	
		Backup SRAM ON, RTC ON and LSE in Medium high drive mode	2.6	3.7	4.5	8	33	68	
		Backup SRAM ON, RTC ON and LSE in High drive mode	2.6	3.7	4.5	9	33	68	

1. The typical current consumption values are given with PDR OFF (internal reset OFF). When the PDR is OFF (internal reset OFF), the typical current consumption is reduced by additional 1.2 µA.
2. Guaranteed by characterization results, unless otherwise specified.
3. Guaranteed by test in production.

Table 51. MIPI D-PHY characteristics[(1)] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Output low level voltage	-	1.1	1.2	1.2	V
$V_{IL-ULPS}$	Output high level voltage	-	-50	-	50	mV
V_{IH}	Output impedance of LP transmitter	-	110	-	-	Ω
V_{hys}	15%-85% rise and fall time	-	-	-	25	ns
LP Contention Detector Characteristics						
V_{ILCD}	Logic 0 contention threshold	-	-	-	200	mV
V_{IHCD}	Logic 0 contention threshold	-	450	-	-	

1. Guaranteed based on test during characterization.

Table 52. MIPI D-PHY AC characteristics LP mode and HS/LP transitions[(1)]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{LPX}	Transmitted length of any Low-Power state period	-	50	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	-	38	-	95	
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Time that the transmitter drives the HS-0 state prior to starting the clock.	-	300	-	-	
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	-	8	-	-	UI

Table 85. SPI dynamic characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tsu(MI)	Data input setup time	Master mode	4 9[4]	-	-	ns
tsu(SI)		Slave mode	4.5	-	-	
th(MI)	Data input hold time	Master mode	3 0[4]	-	-	
th(SI)		Slave mode	2	-	-	
ta(SO)	Data output access time	Slave mode	7	-	21	
tdis(SO)	Data output disable time	Slave mode	5	-	12	
tv(SO)	Data output valid time	Slave mode 2.7≤VDD≤3.6V	-	6.5	10	
		Slave mode 1.71≤VDD≤3.6V	-	6.5	13.5	
tv(MO)		Master mode	-	2	6	
th(SO)	Data output hold time	Slave mode 1.71≤VDD≤3.6V	4.5	-	-	
th(MO)		Master mode	0	-	-	

1. Guaranteed by characterization results.
2. Excepting SPI1 with SCK IO pin mapped on PA5. In this configuration, Maximum achievable frequency is 40MHz.
3. Maximum Frequency of Slave Transmitter is determined by sum of Tv(SO) and Tsu(MI) intervals which has to fit into SCK level phase preceding the SCK sampling edge.This value can be achieved when it communicates with a Master having Tsu(MI)=0 while signal Duty(SCK)=50%.
4. Only for SPI6.

Figure 46. SPI timing diagram - slave mode and CPHA = 0

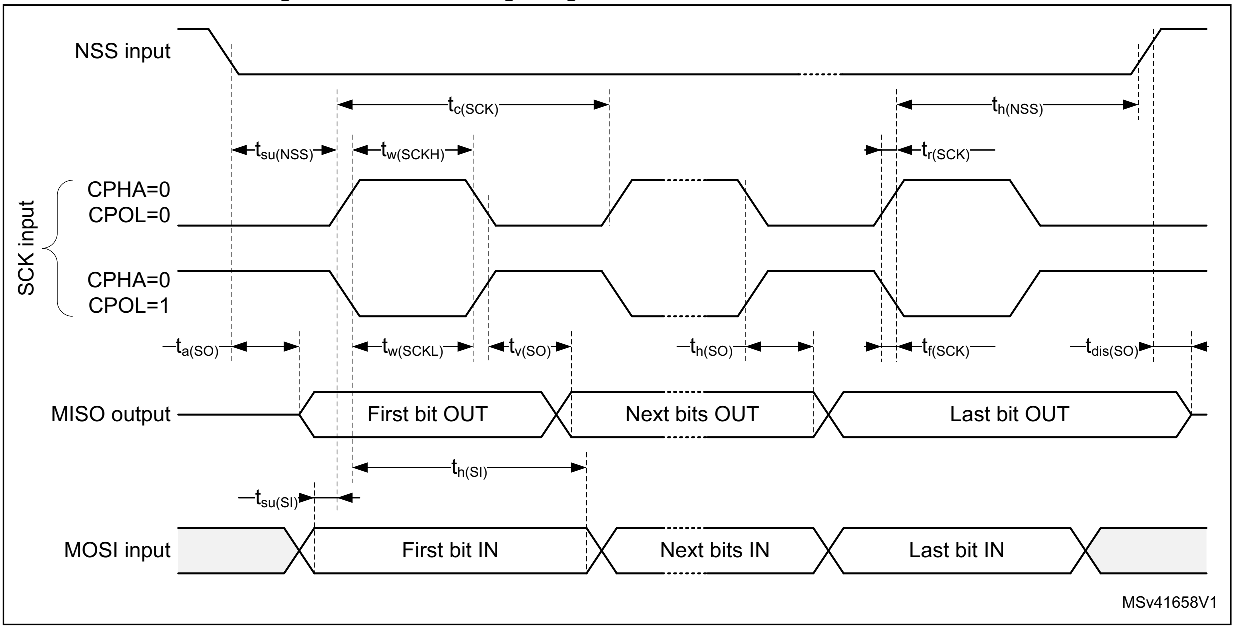


Table 91. USB OTG full speed DC electrical characteristics (continued)

Symbol	Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
R_{PD}	PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM)	$V_{IN} = V_{DD}$	17	21	24	kΩ
	PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)		2.4	5.2	8	
R_{PU}	PA12, PB15 (USB_FS_DP, USB_HS_DP)	$V_{IN} = V_{SS}$	1.5	1.8	2.1	
	PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	$V_{IN} = V_{SS}$	0.55	0.95	1.35	

1. All the voltages are measured from the local ground potential.
2. The USB OTG full speed transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DDUSB} voltage range.
3. Guaranteed by design.
4. R_L is the load connected on the USB OTG full speed drivers.

Note: When VBUS sensing feature is enabled, PA9 and PB13 should be left at their default state (floating input), not as alternate function. A typical 200 µA current consumption of the sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 and PB13 when the feature is enabled.

Figure 55. USB OTG full speed timings: definition of data signal rise and fall time

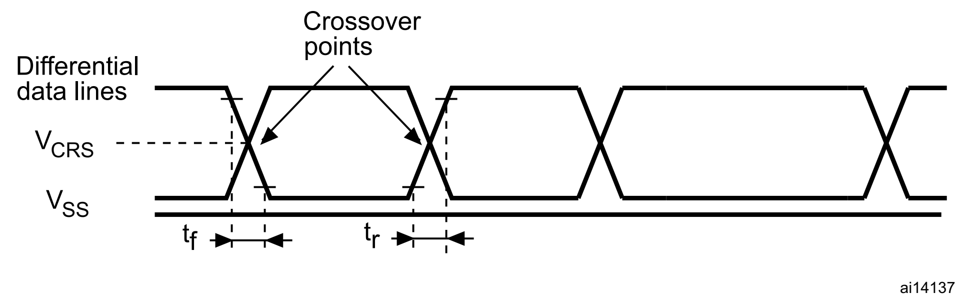


Table 92. USB OTG full speed electrical characteristics(1)

Driver characteristics					
Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V
Z_{DRV}	Output driver impedance(3)	Driving high or low	28	44	Ω

Table 97. Dynamics characteristics: Ethernet MAC signals for RMII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	1	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	2	-	-	
$t_{su(CRS)}$	Carrier sense setup time	2	-	-	
$t_{ih(CRS)}$	Carrier sense hold time	2	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	7.5	8	12	
$t_{d(TXD)}$	Transmit data valid delay time	7	7.5	12.5	

1. Guaranteed by characterization results.

Table 98 gives the list of Ethernet MAC signals for MII and *Figure 58* shows the corresponding timing diagram.

Figure 59. Ethernet MII timing diagram

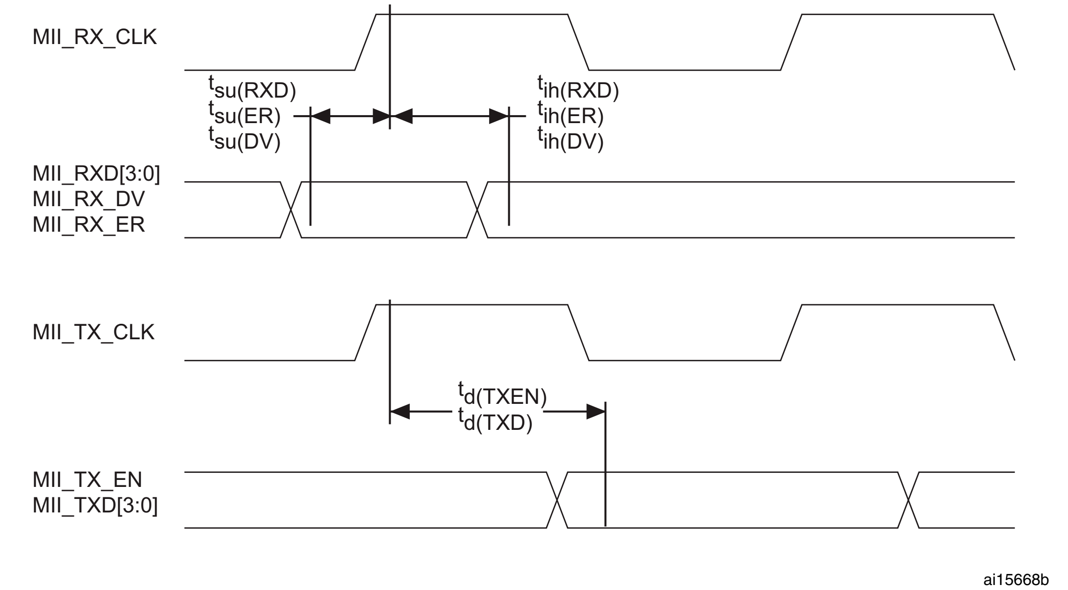


Table 98. Dynamics characteristics: Ethernet MAC signals for MII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	1	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	2.5	-	-	
$t_{su(DV)}$	Data valid setup time	1.5	-	-	
$t_{ih(DV)}$	Data valid hold time	0.5	-	-	
$t_{su(ER)}$	Error setup time	2.5	-	-	
$t_{ih(ER)}$	Error hold time	0.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	10	8	13	
$t_{d(TXD)}$	Transmit data valid delay time	9	7.5	13	

Table 111. Synchronous non-multiplexed PSRAM write timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{(CLK)}$	FMC_CLK period	$2T_{HCLK} - 0.5$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{HCLK} + 0.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{HCLK} + 1$	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{HCLK} + 1$	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. Guaranteed by characterization results.

NAND controller waveforms and timings

Figure 69 through *Figure 72* represent synchronous waveforms, and *Table 112* and *Table 113* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01;
- COM.FMC_WaitSetupTime = 0x03;
- COM.FMC_HoldSetupTime = 0x02;
- COM.FMC_HiZSetupTime = 0x01;
- ATT.FMC_SetupTime = 0x01;
- ATT.FMC_WaitSetupTime = 0x03;
- ATT.FMC_HoldSetupTime = 0x02;
- ATT.FMC_HiZSetupTime = 0x01;
- Bank = FMC_Bank_NAND;
- MemoryDataWidth = FMC_MemoryDataWidth_16b;
- ECC = FMC_ECC_Enable;
- ECCPageSize = FMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the T_{HCLK} is the HCLK clock period.

Table 118. Quad-SPI characteristics (continued)in SDR mode[(1)] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tw(CKH)	Quad-SPI clock high and low time	-	t(CK)/2 - 1	-	t(CK)/2	ns
tw(CKL)			t(CK)/2	-	t(CK)/2 + 1	
ts(IN)	Data input setup time	-	0.5	-	-	
th(IN)	Data input hold time		3	-	-	
tv(OUT)	Data output valid time	2.7 V<V_{DD}<3.6 V	-	1.5	3.5	
		1.71 V<V_{DD}<3.6 V	-	1.5	2	
th(OUT)	Data output hold time	-	0.5	-	-	

1. Guaranteed by characterization results.

Table 119. Quad SPI characteristics in DDR mode[(1)]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Fck1/t(CK)	Quad-SPI clock frequency	2.7 V<V_{DD}<3.6 V CL=20 pF	-	-	80	MHz
		1.8 V<V_{DD}<3.6 V CL=15 pF	-	-	80	
		1.71 V<V_{DD}<3.6 V CL=10 pF	-	-	80	
tw(CKH)	Quad-SPI clock high and low time	-	t(CK)/2 - 1	-	t(CK)/2	ns
tw(CKL)			t(CK)/2	-	t(CK)/2 + 1	
ts(IN), tsf(IN)	Data input setup time	2.7 V<V_{DD}<3.6 V	0.75	-	-	
		1.71 V<V_{DD}<2 V	0.5	-	-	
thr(IN), thf(IN)	Data input hold time	2.7 V<V_{DD}<3.6 V	2	-	-	
		1.71 V<V_{DD}<2 V	3	-	-	
tvr(OUT), tvf(OUT)	Data output valid time	2.7 V<V_{DD}<3.6 V	-	8.5	10	
		1.71 V<V_{DD}<3.6 V DHHC=0	-	8	12	
		DHHC=1 Pres=1, 2...	-	$T_{HCLK}/2$ + 1.5	$T_{HCLK}/2$ + 2.5	
thr(OUT), thf(OUT)	Data output hold time	DHHC=0	7.5	-	-	
		DHHC=1 Pres=1, 2...	$T_{HCLK}/2$ + 0.5	-	-	

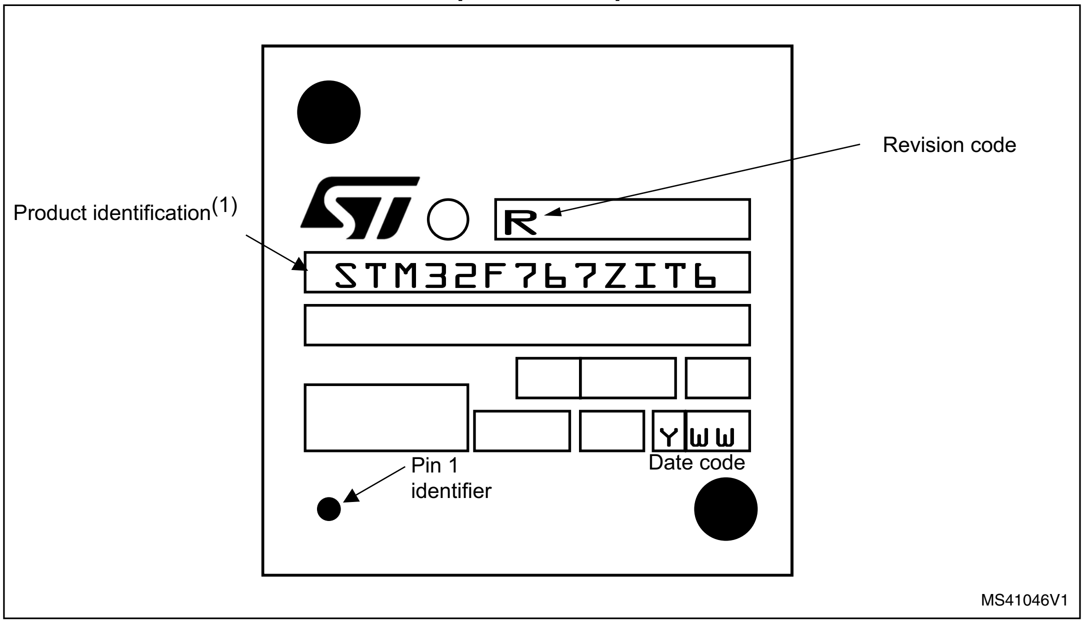
1. Guaranteed by characterization results.

LQFP144 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

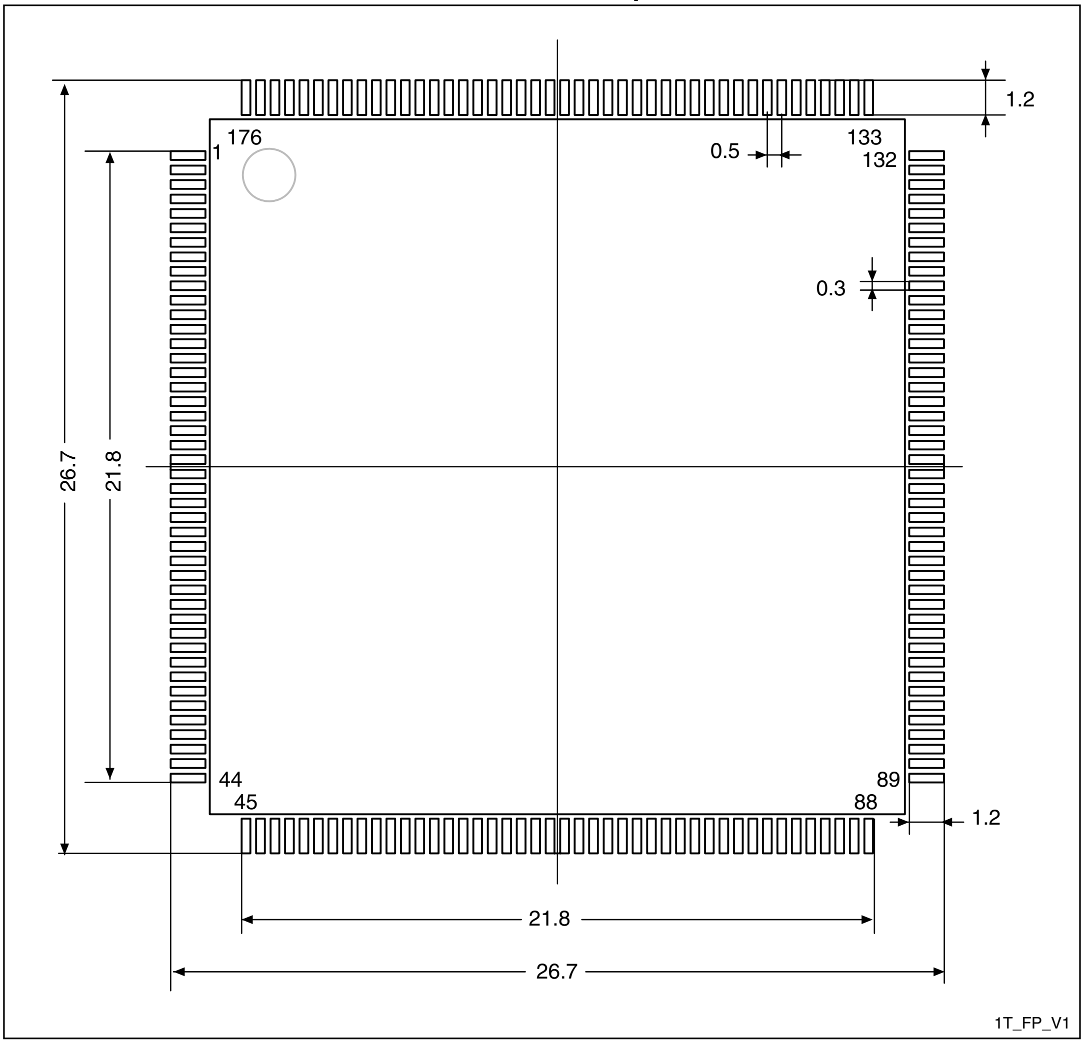
Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 88. LQFP144, 20 x 20mm, 144-pin low-profile quad flat package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Figure 90. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package recommended footprint



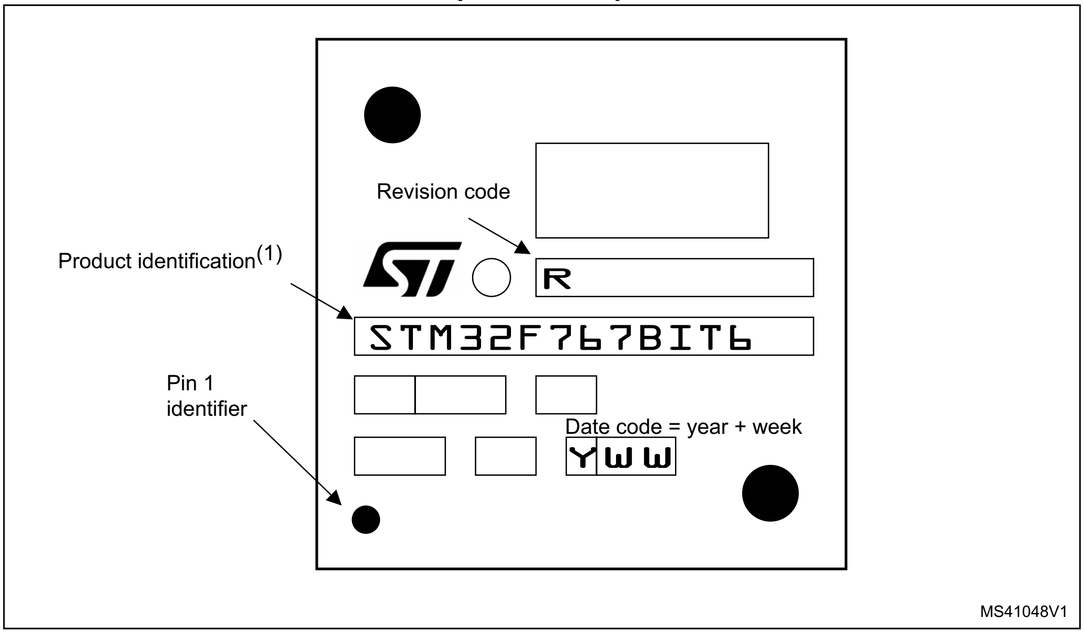
1. Dimensions are expressed in millimeters.

LQFP208 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 94. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.