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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

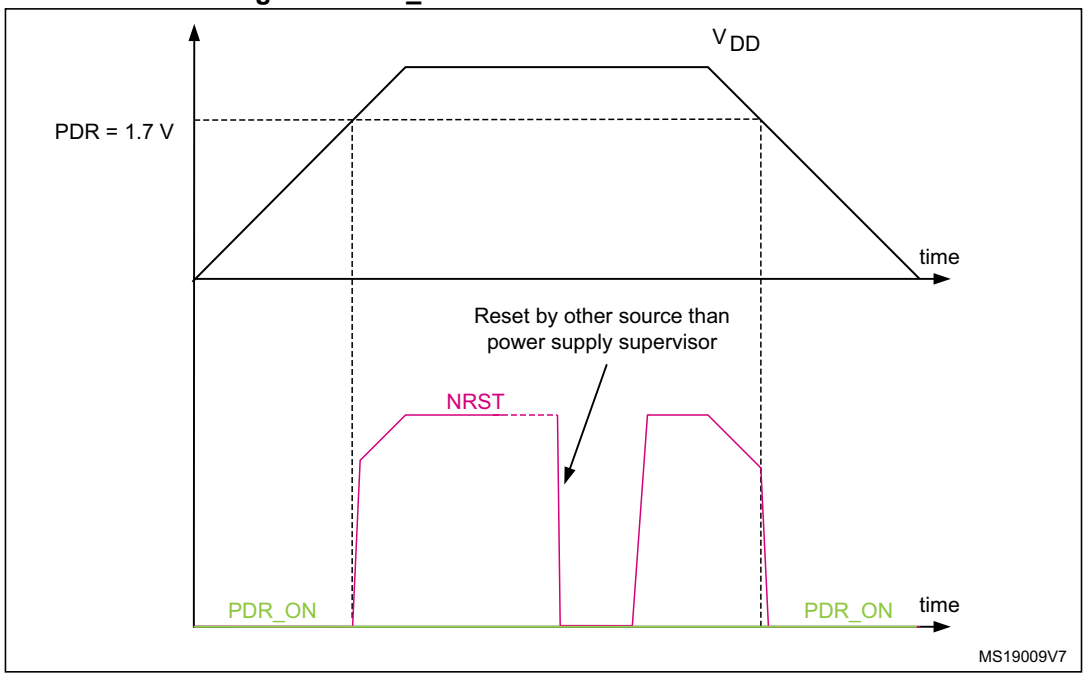
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f765vgt7

Table 2. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx features and peripheral counts

Peripherals		STM32F 765Vx		STM32F767 /769Vx		STM32F 765Zx		STM32F767 /769Zx		STM32F 769Ax		STM32F 768Ax	STM32F 765Ix		STM32F767 /769Ix		STM32F 765Bx		STM32F767 /769Bx		STM32F 765Nx		STM32F767 /769Nx	
Flash memory in Kbytes		1024	2048	1024	2048	1024	2048	1024	2048	1024	2048	2048	1024	2048	1024	2048	1024	2048	1024	2048	1024	2048	1024	2048
SRAM in Kbytes	System	512(368+16+128)																						
	Instruction	16																						
	Backup	4																						
FMC memory controller		Yes(1)																						
Quad-SPI		Yes																						
Ethernet		Yes								No		Yes												
Timers	General-purpose	10																						
	Advanced-control	2																						
	Basic	2																						
	Low-power	1																						
Random number generator		Yes																						
Communication interfaces	SPI / I^2S	4/3 (simplex)(2)				6/3 (simplex)(2)																		
	I^2C	4																						
	USART/UART	4/4																						
	USB OTG FS	Yes																						
	USB OTG HS	Yes																						
	CAN	3																						
	SAI	2																						
	SPDIFRX	4 inputs																						
	SDMMC1	Yes																						
	SDMMC2	Yes(3)																						
Camera interface		Yes																						
MIPI-DSI Host(4)		No								Yes			No		Yes		No		Yes		No		Yes	
LCD-TFT		No		Yes		No		Yes					No		Yes		No		Yes		No		Yes	

Figure 7. PDR_ON control with internal reset OFF



2.19 Voltage regulator

The regulator has four operating modes:

- Regulator ON
  - Main regulator mode (MR)
  - Low power regulator (LPR)
  - Power-down
- Regulator OFF

2.19.1 Regulator ON

On packages embedding the BYPASS_REG pin, the regulator is enabled by holding BYPASS_REG low. On all other packages, the regulator is always enabled.

There are three power modes configured by software when the regulator is ON:

- MR mode used in Run/sleep modes or in Stop modes
  - In Run/Sleep modes

    The MR mode is used either in the normal mode (default mode) or the over-drive mode (enabled by software). Different voltages scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption. The over-drive mode allows operating at a higher frequency than the normal mode for a given voltage scaling.
  - In Stop modes

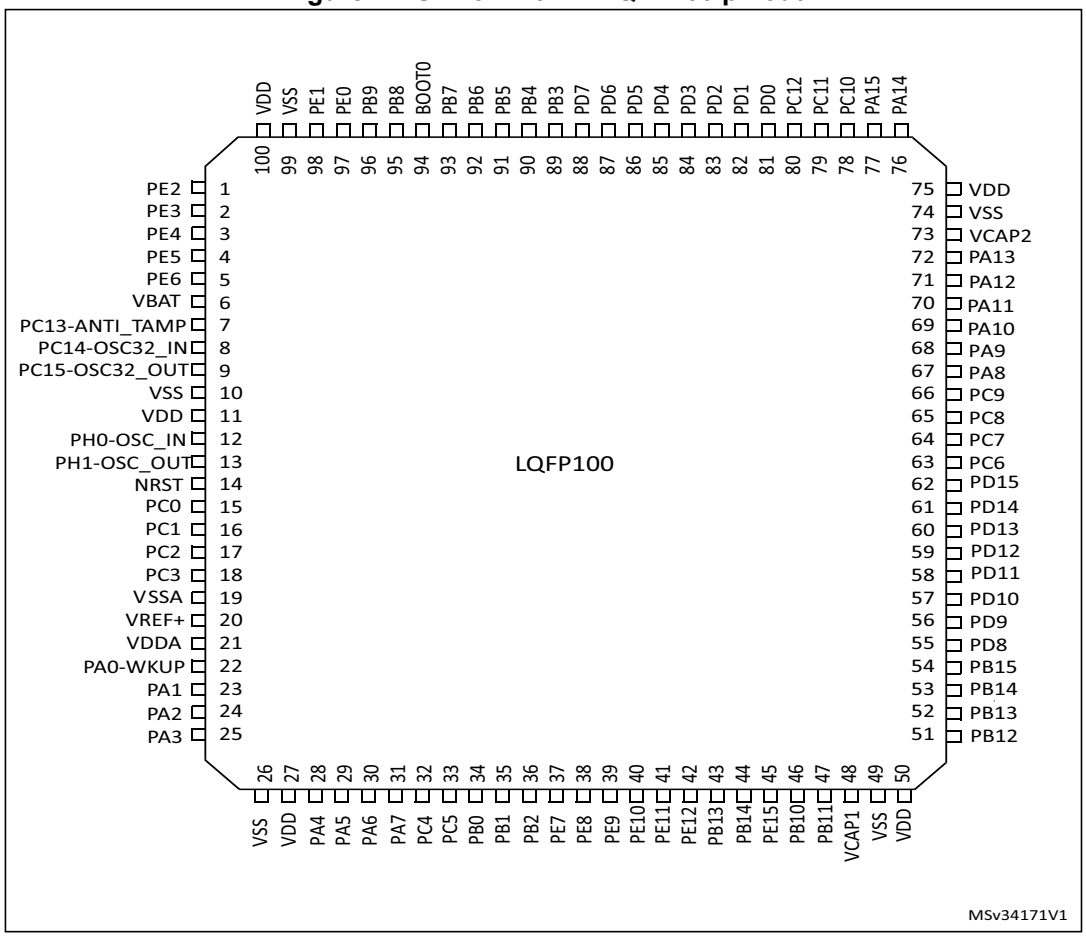
    The MR can be configured in two ways during stop mode:

    MR operates in normal mode (default mode of MR in stop mode)

    MR operates in under-drive mode (reduced leakage mode).

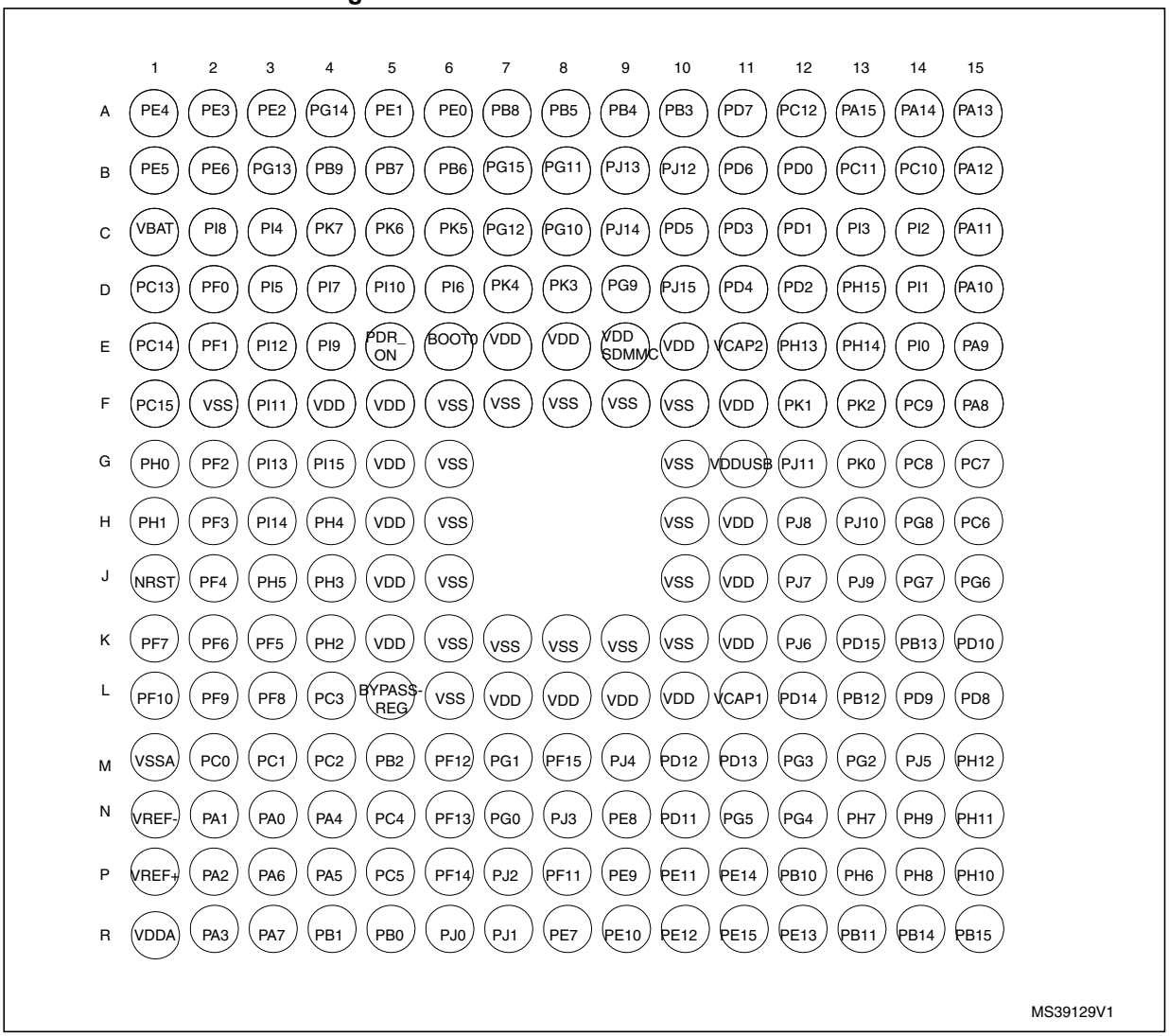
3 Pinouts and pin description

Figure 11. STM32F76xxx LQFP100 pinout



1. The above figure shows the package top view.

Figure 19. STM32F76xxx TFBGA216 ballout



1. The above figure shows the package top view.

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	19	K1	25	28	K1	NC	25	28	K1	PF7	I/O	FT	-	TIM11_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_TX, QUADSPI_BK1_IO2, EVENTOUT	ADC3_IN5
-	20	L3	26	29	L3	NC	26	29	L3	PF8	I/O	FT	-	SPI5_MISO, SAI1_SCK_B, UART7_RTS, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT	ADC3_IN6
-	21	L2	27	30	L2	NC	27	30	L2	PF9	I/O	FT	-	SPI5_MOSI, SAI1_FS_B, UART7_CTS, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT	ADC3_IN7
-	22	L1	28	31	L1	K11	28	31	L1	PF10	I/O	FT	-	QUADSPI_CLK, DCMI_D11, LCD_DE, EVENTOUT	ADC3_IN8
12	23	G1	29	32	G1	K12	29	32	G1	PH0-OSC_IN	I/O	FT	(3)	EVENTOUT	OSC_IN
13	24	H1	30	33	H1	K13	30	33	H1	PH1-OSC_OUT	I/O	FT	(3)	EVENTOUT	OSC_OUT
14	25	J1	31	34	J1	L11	31	34	J1	NRST	I/O	RST	-	-	-
15	26	M2	32	35	M2	L12	32	35	M2	PC0	I/O	FT	-	DFSDM1_CKIN0, DFSDM1_DATIN4, SAI2_FS_B, OTG_HS_ULPI_STP, FMC_SDNWE, LCD_R5, EVENTOUT	ADC1_IN10, ADC2_IN10, ADC3_IN10
16	27	M3	33	36	M3	L13	33	36	M3	PC1	I/O	FT	-	TRACED0, DFSDM1_DATIN0, SPI2_MOSI/I2S2_SD, SAI1_SD_A, DFSDM1_CKIN4, ETH_MDC, MDIOS_MDC, EVENTOUT	ADC1_IN11, ADC2_IN11, ADC3_IN11, RTC_TAMP3/WKUP3

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
47	70	R13	80	91	R13	L5	80	91	R13	PB11	I/O	FT	-	TIM2_CH4, I2C2_SDA, DFSDM1_CKIN7, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_RMII_TX_EN, DSI_TE, LCD_G5, EVENTOUT	-
48	71	M10	81	92	L11	P5	81	92	L11	VCAP_1	S	-	-	-	-
49	-	-	-	93	K9	N5	-	93	K9	VSS	S	-	-	-	-
50	72	N10	82	94	L10	P4	82	94	L10	VDD	S	-	-	-	-
-	-	-	-	95	M14	NC	-	95	M14	PJ5	I/O	FT	-	LCD_R6, EVENTOUT	-
-	-	M11	83	96	P13	NC	83	96	P13	PH6	I/O	FT	-	I2C2_SMBA, SPI5_SCK, TIM12_CH1, ETH_MII_RXD2, FMC_SDNE1, DCMI_D8, EVENTOUT	-
-	-	N12	84	97	N13	NC	84	97	N13	PH7	I/O	FT	-	I2C3_SCL, SPI5_MISO, ETH_MII_RXD3, FMC_SDCKE1, DCMI_D9, EVENTOUT	-
-	-	M12	85	98	P14	M5	-	98	P14	PH8	I/O	FT	-	I2C3_SDA, FMC_D16, DCMI_HSYNC, LCD_R2, EVENTOUT	-
-	-	M13	86	99	N14	K4	-	99	N14	PH9	I/O	FT	-	I2C3_SMBA, TIM12_CH2, FMC_D17, DCMI_D0, LCD_R3, EVENTOUT	-
-	-	L13	87	100	P15	L4	-	100	P15	PH10	I/O	FT	-	TIM5_CH1, I2C4_SMBA, FMC_D18, DCMI_D1, LCD_R4, EVENTOUT	-
-	-	L12	88	101	N15	M4	-	101	N15	PH11	I/O	FT	-	TIM5_CH2, I2C4_SCL, FMC_D19, DCMI_D2, LCD_R5, EVENTOUT	-

1. NC (not-connected) pins are not bonded. They must be configured by software to output push-pull and forced to 0 in the output data register to avoid an extra current consumption in low-power modes. list of pins: PI8, PI12, PI13, PI14, PF6, PF7, PF8, PF9, PC2, PC3, PC4, PC5, PI15, PJ0, PJ1, PJ2, PJ3, PJ4, PJ5, PH6, PH7, PJ12, PJ13, PJ14, PJ15, PG14, PK3, PK4, PK5, PK6 and PK7.
2. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: - The speed should not exceed 2 MHz with a maximum load of 30 pF. - These I/Os must not be used as a current source (e.g. to drive an LED).
3. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
4. If the device is in regulator OFF/internal reset ON mode (BYPASS_REG pin is set to VDD), then PA0 is used as an internal reset (active low).
5. Internally connected to VDD or VSS depending on part number.

Table 12. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM1/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port B	PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	DFSDM1_CKIN5	USART1_RX	-	-	-	I2S4_SDA	FMC_NL	DCMI_VSYNC	-	EVENTOUT
	PB8	-	I2C4_SCL	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	DFSDM1_CKIN7	UART5_RX	-	CAN1_RX	SDMMC2_D4	ETH_MII_TXD3	SDMMC_D4	DCMI_D6	LCD_B6	EVENTOUT
	PB9	-	I2S4_SDA	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS/I2S2_WS	DFSDM1_DATIN7	UART5_TX	-	CAN1_TX	SDMMC2_D5	I2C4_SMBA	SDMMC_D5	DCMI_D7	LCD_B7	EVENTOUT
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK/I2S2_CK	DFSDM1_DATIN7	USART3_TX	-	- QUADSPI_BK1_NCS	OTG_HS_ULPI_D3	ETH_MII_RX_ER	-	-	LCD_G4	EVENTOUT
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	DFSDM1_CKIN7	USART3_RX	-	-	OTG_HS_ULPI_D4	ETH_MII_TX_EN/ETH_RMII_TX_EN	-	DSI_TE	LCD_G5	EVENTOUT
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS/I2S2_WS	DFSDM1_DATIN1	USART3_CK	UART5_RX	CAN2_RX	OTG_HS_ULPI_D5	ETH_MII_TXD0/ETH_RMII_TXD0	OTG_HS_ID	-	-	EVENTOUT
	PB13	-	TIM1_CH1N	-	-	-	SPI2_SCK/I2S2_CK	DFSDM1_CKIN1	USART3_CTS	UART5_TX	CAN2_TX	OTG_HS_ULPI_D6	ETH_MII_TXD1/ETH_RMII_TXD1	-	-	-	EVENTOUT
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	USART1_TX	SPI2_MISO	DFSDM1_DATIN2	USART3_RTS	UART4_RTS	TIM12_CH1	SDMMC2_D0	-	OTG_HS_DM	-	-	EVENTOUT
	PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	USART1_RX	SPI2_MOSI/I2S2_SD	DFSDM1_CKIN2	-	UART4_CTS	TIM12_CH2	SDMMC2_D1	-	OTG_HS_DP	-	-	EVENTOUT

Table 13. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx register boundary addresses(1) (continued)

Bus	Boundary address	Peripheral
	0x4001 7C00 - 0x4001 FFFF	Reserved
APB2	0x4001 7800 - 0x4001 7BFF	MDIOS
	0x4001 7400 - 0x4001 77FF	DFSDM1
	0x4001 6C00 - 0x4001 73FF	DSI Host
	0x4001 6800 - 0x4001 6BFF	LCD-TFT
	0x4001 6000 - 0x4001 67FF	Reserved
	0x4001 5C00 - 0x4001 5FFF	SAI2
	0x4001 5800 - 0x4001 5BFF	SAI1
	0x4001 5400 - 0x4001 57FF	SPI6
	0x4001 5000 - 0x4001 53FF	SPI5
	0x4001 4C00 - 0x4001 4FFF	Reserved
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4
	0x4001 3000 - 0x4001 33FF	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	SDMMC1
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1 - ADC2 - ADC3
	0x4001 1C00 - 0x4001 1FFF	SDMMC2
	0x4001 1800 - 0x4001 1BFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1

Table 19. VCAP1/VCAP2 operating conditions(1)

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	2.2 µF
ESR	ESR of external capacitor	< 2 Ω

1. When bypassing the voltage regulator, the two 2.2 µF V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

5.3.3 Operating conditions at power-up / power-down (regulator ON)

Subject to general operating conditions for T_A.

Table 20. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	20	∞	µs/V
	V_{DD} fall time rate	20	∞	

5.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A.

Table 21. Operating conditions at power-up / power-down (regulator OFF)(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Power-up	20	∞	µs/V
	V_{DD} fall time rate	Power-down	20	∞	
t_{VCAP}	V_{CAP_1} and V_{CAP_2} rise time rate	Power-up	20	∞	
	V_{CAP_1} and V_{CAP_2} fall time rate	Power-down	20	∞	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when V_{DD} reach below 1.08 V.

5.3.5 Reset and power control block characteristics

The parameters given in *Table 22* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 34. Typical and maximum current consumption in Sleep mode, regulator OFF

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ		Max(1)						Unit
						TA= 25 °C		TA= 85 °C		TA= 105 °C		
				IDD12	IDD	IDD12	IDD	IDD12	IDD	IDD12	IDD	
IDD12/ IDD	Supply current in RUN mode from V12 and V_{DD} supply	All Peripherals Enabled(2)	180	102	1	114	2	148	2	168	2	mA
			168	91	1	101	2	132	2	152	2	
			144	71	1	78	2	105	2	122	2	
			60	32	1	37	2	64	2	81	2	
			25	16	1	20	2	46	2	64	2	
		All Peripherals Disabled	180	13	1	18	2	53	2	73	2	
			168	12	1	16	2	47	2	67	2	
			144	9	1	13	2	39	2	56	2	
			60	5	1	9	2	35	2	52	2	
			25	3	1	7	2	33	2	50	2	

1. Guaranteed by characterization results, unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.

Table 35. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max(1)			Unit
				V_{DD} = 3.6 V			
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
$I_{DD\_STOP\_NM}$ (normal mode)	Supply current in Stop mode, main regulator in Run mode	Flash memory in Stop mode, all oscillators OFF, no IWDG	0.55	3	18	27	mA
		Flash memory in Deep power down mode, all oscillators OFF	0.5	3	18	27	
	Supply current in Stop mode, main regulator in Low-power mode	Flash memory in Stop mode, all oscillators OFF, no IWDG	0.42	2.5	15	24	
		Flash memory in Deep power down mode, all oscillators OFF, no IWDG	0.37	2.5	15	24	
$I_{DD\_STOP\_UDM}$ (under-drive mode)	Supply current in Stop mode, main regulator in Low voltage and under-drive modes	Regulator in Run mode, Flash memory in Deep power down mode, all oscillators OFF, no IWDG	0.18	1.2	6	10	
		Regulator in Low-power mode, Flash memory in Deep power down mode, all oscillators OFF, no IWDG	0.13	1.1	6	10	

1. Data based on characterization, tested in production.

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

5.3.17 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 60*. They are based on the EMS levels and classes defined in application note AN1709.

Table 60. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 216 MHz, conforms to IEC 61000-4-2	2B
V_{FTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A =+25 °C, f_{HCLK} = 168 MHz, conforms to IEC 61000-4-2	5A

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

5.3.25 Temperature sensor characteristics

Table 77. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L (1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	-	2.5	-	mV/°C
V_{25} (1)	Voltage at 25 °C	-	0.76	-	V
t_{START} (2)	Startup time	-	6	10	µs
T_{S_temp} (2)	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	µs

1. Guaranteed by characterization results.
2. Guaranteed by design.

Table 78. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FF0 F44C - 0x1FF0 F44D
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C, V_{DDA}= 3.3 V	0x1FF0 F44E - 0x1FF0 F44F

5.3.26 V_{BAT} monitoring characteristics

Table 79. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	
Er(1)	Error on Q	–1	-	+1	%
T_{S_vbat} (2)(2)	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

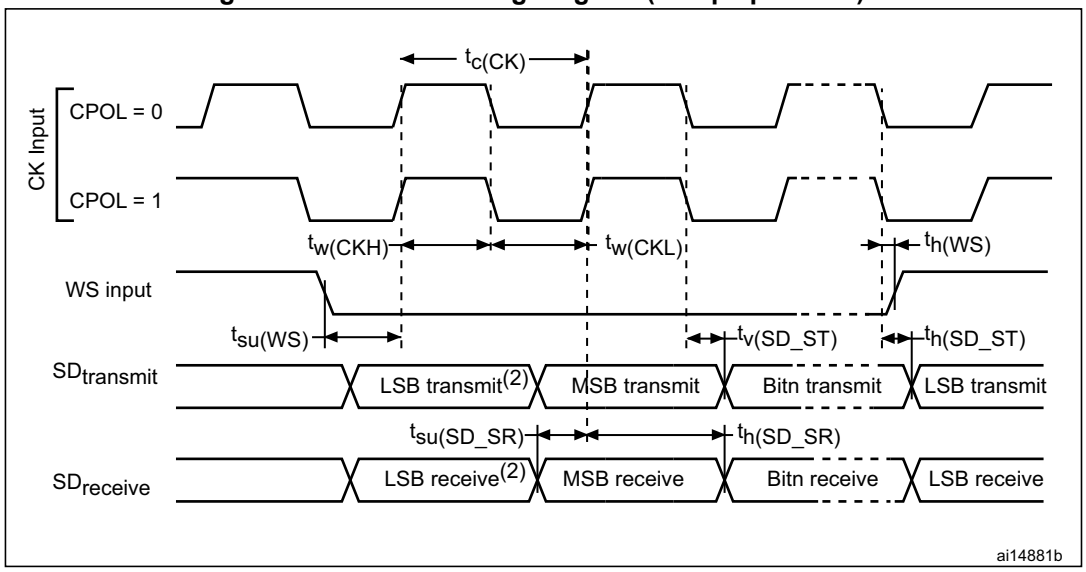
5.3.27 Reference voltage

The parameters given in *Table 80* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 80. internal reference voltage

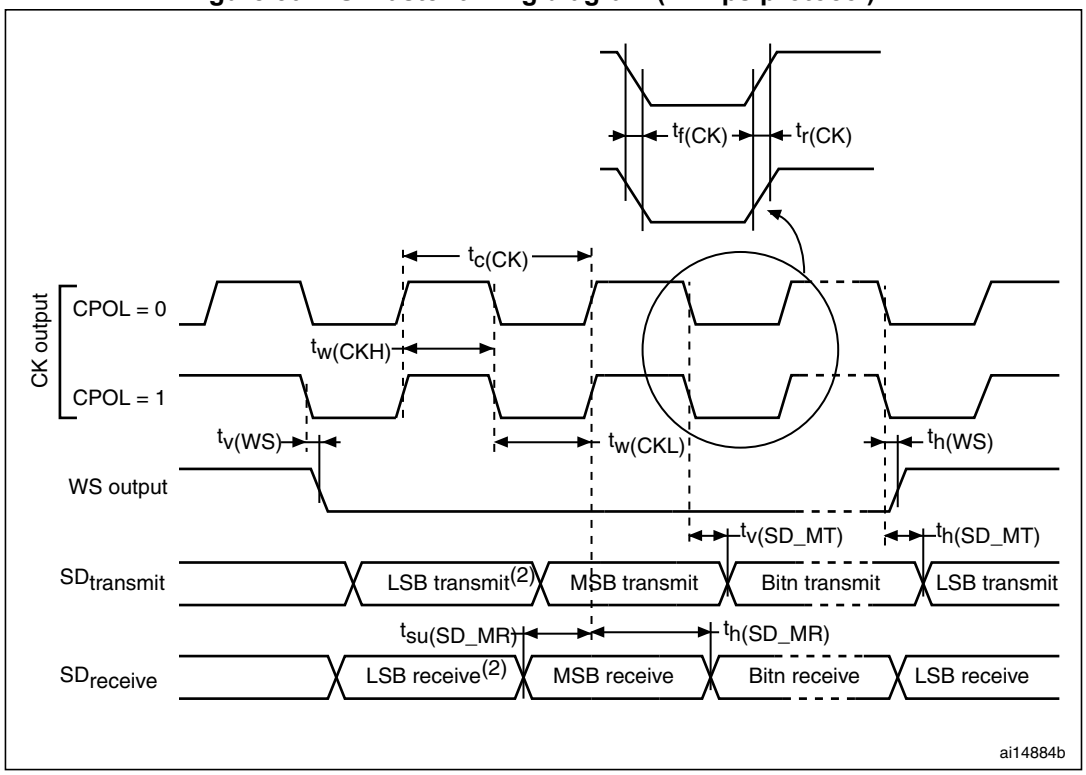
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.18	1.21	1.24	V
$T_{S\_vrefint}$ (1)	ADC sampling time when reading the internal reference voltage	-	10	-	-	µs
V_{RERINT_s} (2)	Internal reference voltage spread over the temperature range	V_{DD} = 3V ± 10mV	-	3	5	mV

Figure 49. I²S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 50. I²S master timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Table 89. SAI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge) 2.7≤VDD≤3.6V	-	12	ns
		Slave transmitter (after enable edge) 1.71≤VDD≤3.6V	-	20	
$t_{h(SD\_B\_MT)}$	Data output hold time	Slave transmitter (after enable edge)	5	-	
$t_{v(SD\_MT)\_A}$	Data output valid time	Master transmitter (after enable edge) 2.7≤VDD≤3.6V	-	15	
		Master transmitter (after enable edge) 1.71≤VDD≤3.6V	-	20	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	5	-	

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.
3. With F_S=192kHz.

Figure 53. SAI master timing waveforms

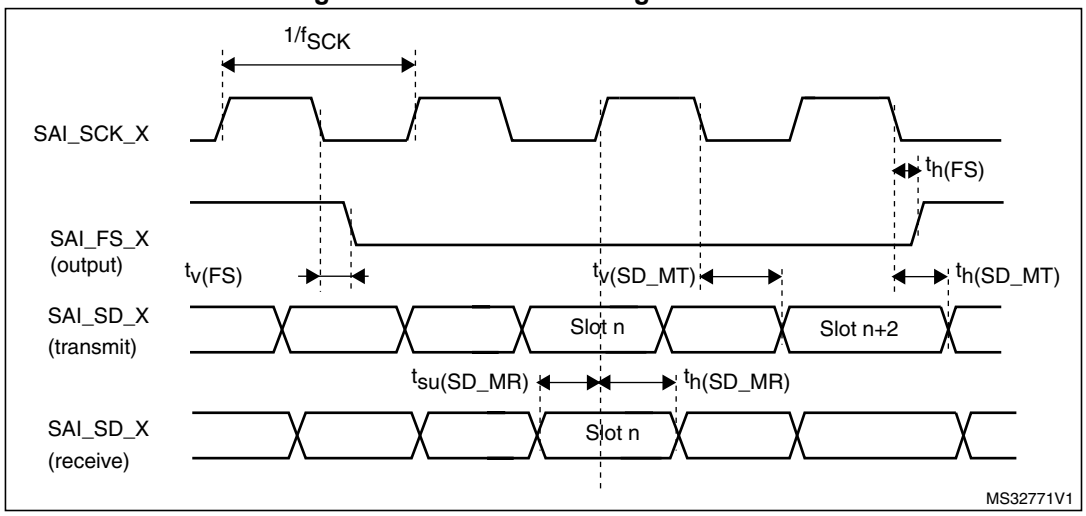


Table 91. USB OTG full speed DC electrical characteristics (continued)

Symbol	Parameter	Conditions	Min. (1)	Typ.	Max. (1)	Unit
R_{PD}	PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM)	$V_{IN} = V_{DD}$	17	21	24	kΩ
	PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)		2.4	5.2	8	
R_{PU}	PA12, PB15 (USB_FS_DP, USB_HS_DP)	$V_{IN} = V_{SS}$	1.5	1.8	2.1	
	PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	$V_{IN} = V_{SS}$	0.55	0.95	1.35	

1. All the voltages are measured from the local ground potential.
2. The USB OTG full speed transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DDUSB} voltage range.
3. Guaranteed by design.
4. R_L is the load connected on the USB OTG full speed drivers.

Note: When VBUS sensing feature is enabled, PA9 and PB13 should be left at their default state (floating input), not as alternate function. A typical 200 µA current consumption of the sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 and PB13 when the feature is enabled.

Figure 55. USB OTG full speed timings: definition of data signal rise and fall time

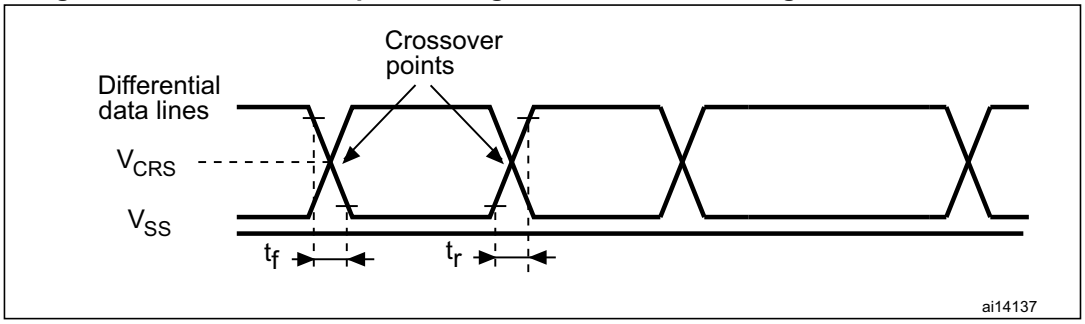


Table 92. USB OTG full speed electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V
Z_{DRV}	Output driver impedance(3)	Driving high or low	28	44	Ω

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output characteristics.

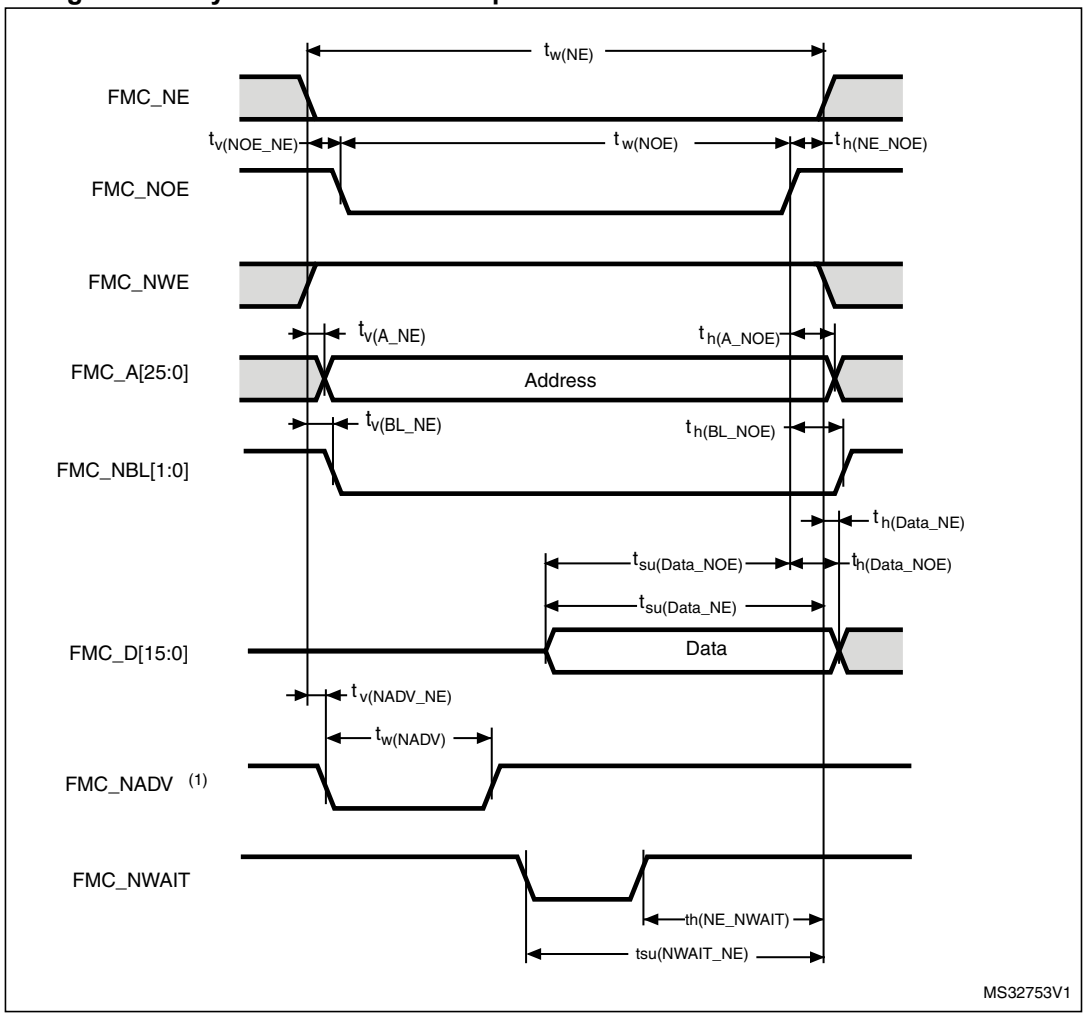
Asynchronous waveforms and timings

Figure 61 through *Figure 64* represent asynchronous waveforms and *Table 100* through *Table 107* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode , DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- Capcitive load CL = 30 pF

In all timing tables, the T_{HCLK} is the HCLK clock period

Figure 61. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms

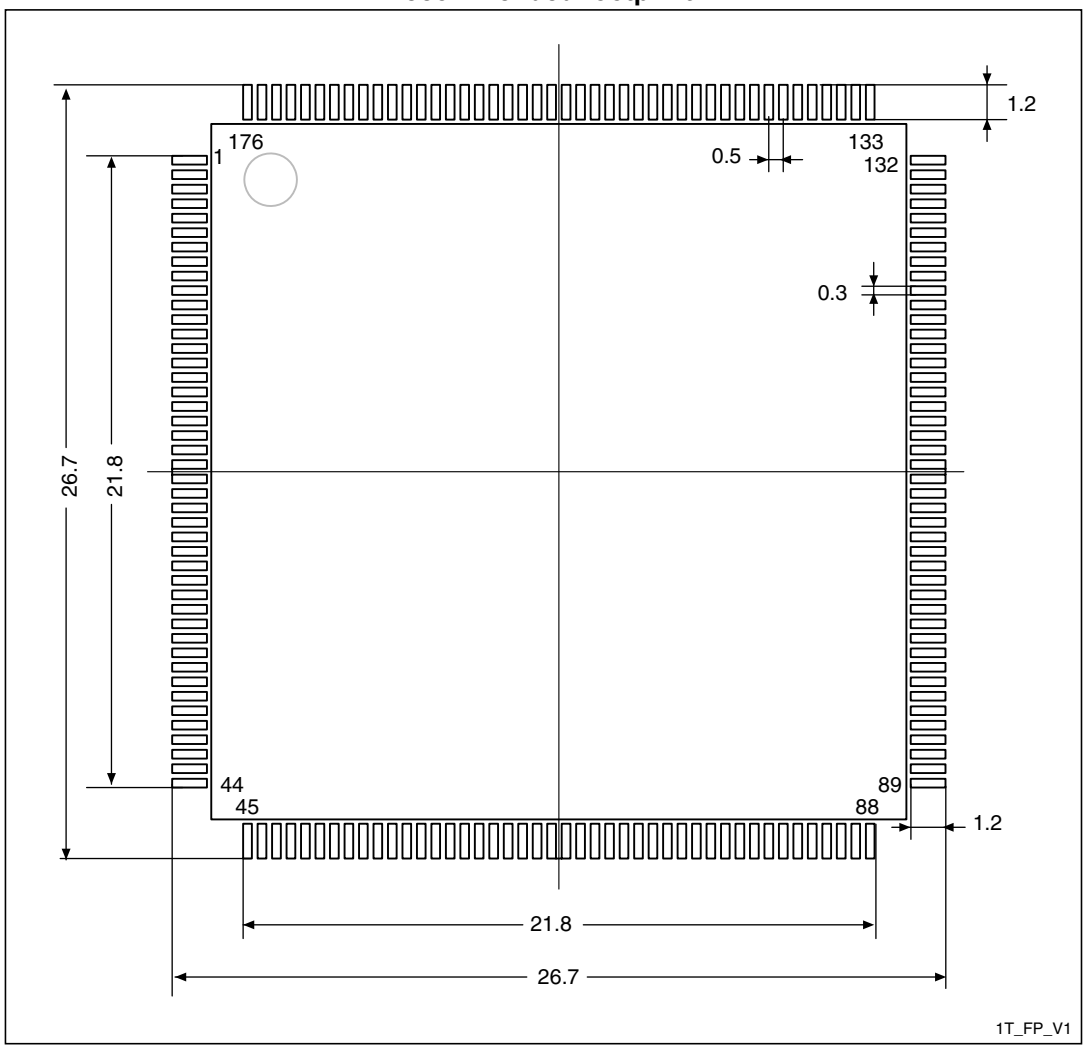


1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 122. DFSDM measured timing 1.71-3.6V (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < V_{DD} < 3.6 V	TCKIN/2 - 0.5	$T_{CKIN}/2$	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < V_{DD} < 3.6 V	2	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < V_{DD} < 3.6 V	3	-	-	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0]=2,3), Internal clock mode (SPICKSEL[1:0]≠0), 1.71 < V_{DD} < 3.6 V	(CKOUTDIV+1) * $T_{DFSDMCLK}$	-	(2*CKOUTDIV) * $T_{DFSDMCLK}$	

Figure 90. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

7 Ordering information

Table 136. Ordering information scheme

Example: STM32 F 76x V G T 6 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

765= STM32F765xx, USB OTG FS/HS, camera interface, Ethernet
767= STM32F767xx, USB OTG FS/HS, camera interface, Ethernet, LCD-TFT
768 = STM32F768Ax, USB OTG FS/HS, camera interface, DSI host, WLCSP with internal regulator OFF
769= STM32F769xx, USB OTG FS/HS, camera interface, Ethernet, DSI host

Pin count

V = 100 pins
Z = 144 pins
I = 176 pins
A = 180 pins
B = 208 pins
N = 216 pins

Flash memory size

G = 1024 Kbytes of Flash memory
I = 2048 Kbytes of Flash memory

Package

T = LQFP
K = UFBGA
H = TFBGA
Y = WLCSP

Temperature range

6 = Industrial temperature range, –40 to 85 °C.
7 = Industrial temperature range, –40 to 105 °C.

Options

xxx = programmed parts
TR = tape and reel

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.