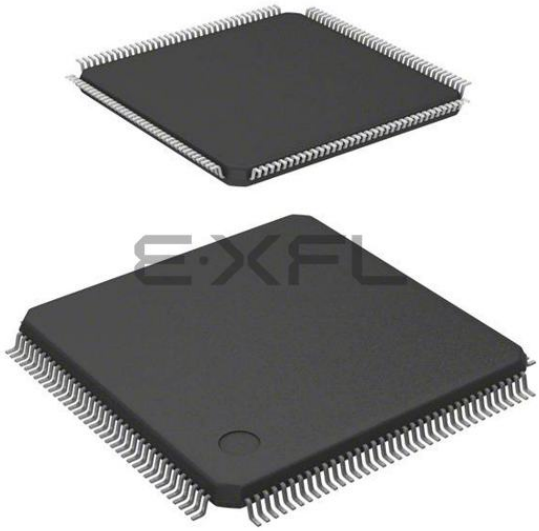

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f765zgt7

1 Description

The STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx devices are based on the high-performance ARM® Cortex®-M7 32-bit RISC core operating at up to 216 MHz frequency. The Cortex®-M7 core features a floating point unit (FPU) which supports ARM® double-precision and single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances the application security.

The STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx devices incorporate high-speed embedded memories with a Flash memory up to 2 Mbytes, 512 Kbytes of SRAM (including 128 Kbytes of Data TCM RAM for critical real-time data), 16 Kbytes of instruction TCM RAM (for critical real-time routines), 4 Kbytes of backup SRAM available in the lowest power modes, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses, a 32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memories access.

All the devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers, a true random number generator (RNG). They also feature standard and advanced communication interfaces.

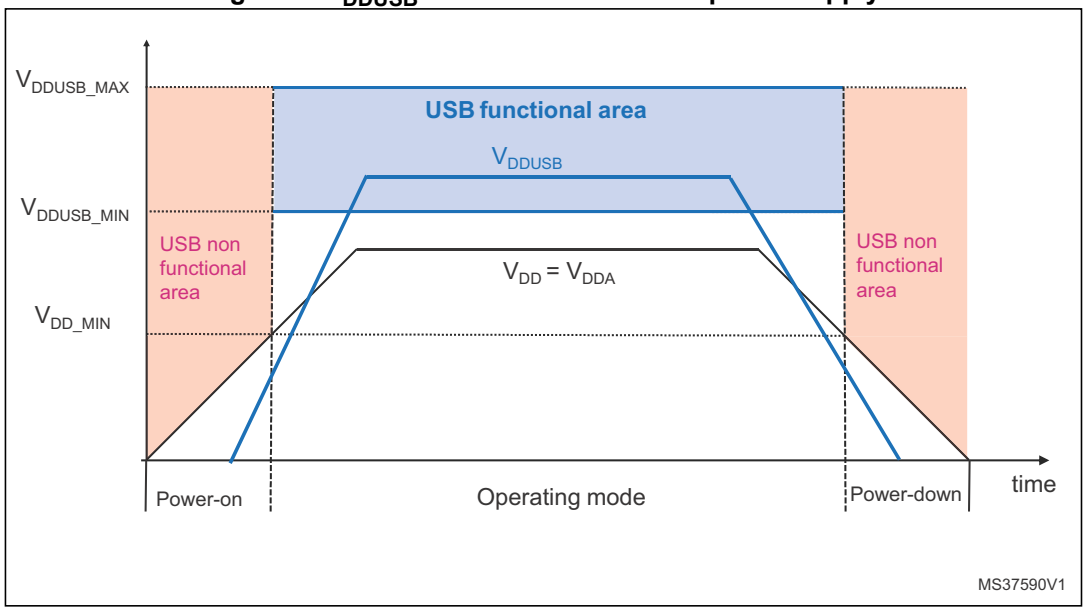
- Up to four I^2Cs
- Six SPIs, three I^2Ss in half-duplex mode. To achieve audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI)
- Three CANs
- Two SAI serial audio interfaces
- Two SDMMC host interfaces
- Ethernet and camera interfaces
- LCD-TFT display controller
- Chrom-ART Accelerator™
- SPDIFRX interface
- HDMI-CEC

Advanced peripherals include two SDMMC interfaces, a flexible memory control (FMC) interface, a Quad-SPI Flash memory interface, a camera interface for CMOS sensors. Refer to *Table 2: STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx features and peripheral counts* for the list of peripherals available on each part number.

The STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx devices operate in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply. Dedicated supply inputs for USB (OTG_FS and OTG_HS) and SDMMC2 (clock, command and 4-bit data) are available on all the packages except LQFP100 for a greater power supply choice.

The supply voltage can drop to 1.7 V with the use of an external power supply supervisor (refer to *Section 2.18.2: Internal reset OFF*). A comprehensive set of power-saving mode allows the design of low-power applications.

Figure 5. V_{DDUSB} connected to external power supply



The DSI (Display Serial Interface) sub-system uses several power supply pins which are independent from the other supply pins:

- V_{DDDSI} is an independent DSI power supply dedicated for DSI Regulator and MIPI D-PHY. This supply must be connected to global V_{DD}.
- The V_{CAPDSI} pin is the output of DSI Regulator (1.2V) which must be connected externally to $V_{DD12DSI}$.
- The $V_{DD12DSI}$ pin is used to supply the MIPI D-PHY, and to supply the clock and data lanes pins. An external capacitor of 2.2 uF must be connected on the $V_{DD12DSI}$ pin.
- The V_{SSDSI} pin is an isolated supply ground used for DSI sub-system.
- If the DSI functionality is not used at all, then:
  - The V_{DDDSI} pin must be connected to global V_{DD}.
  - The V_{CAPDSI} pin must be connected externally to $V_{DD12DSI}$ but the external capacitor is no more needed.
  - The V_{SSDSI} pin must be grounded.

2.18 Power supply supervisor

2.18.1 Internal reset ON

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On the other packages, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR thresholds, or to disable BOR permanently. Three BOR thresholds are available through

- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Battery Charging Specification Revision 1.2 support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected

2.36 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The devices embed a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI-CEC controller to wakeup the MCU from Stop mode on data reception.

2.37 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain a data transfer rate up to 54 Mbytes/s in 8-bit mode at 54 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

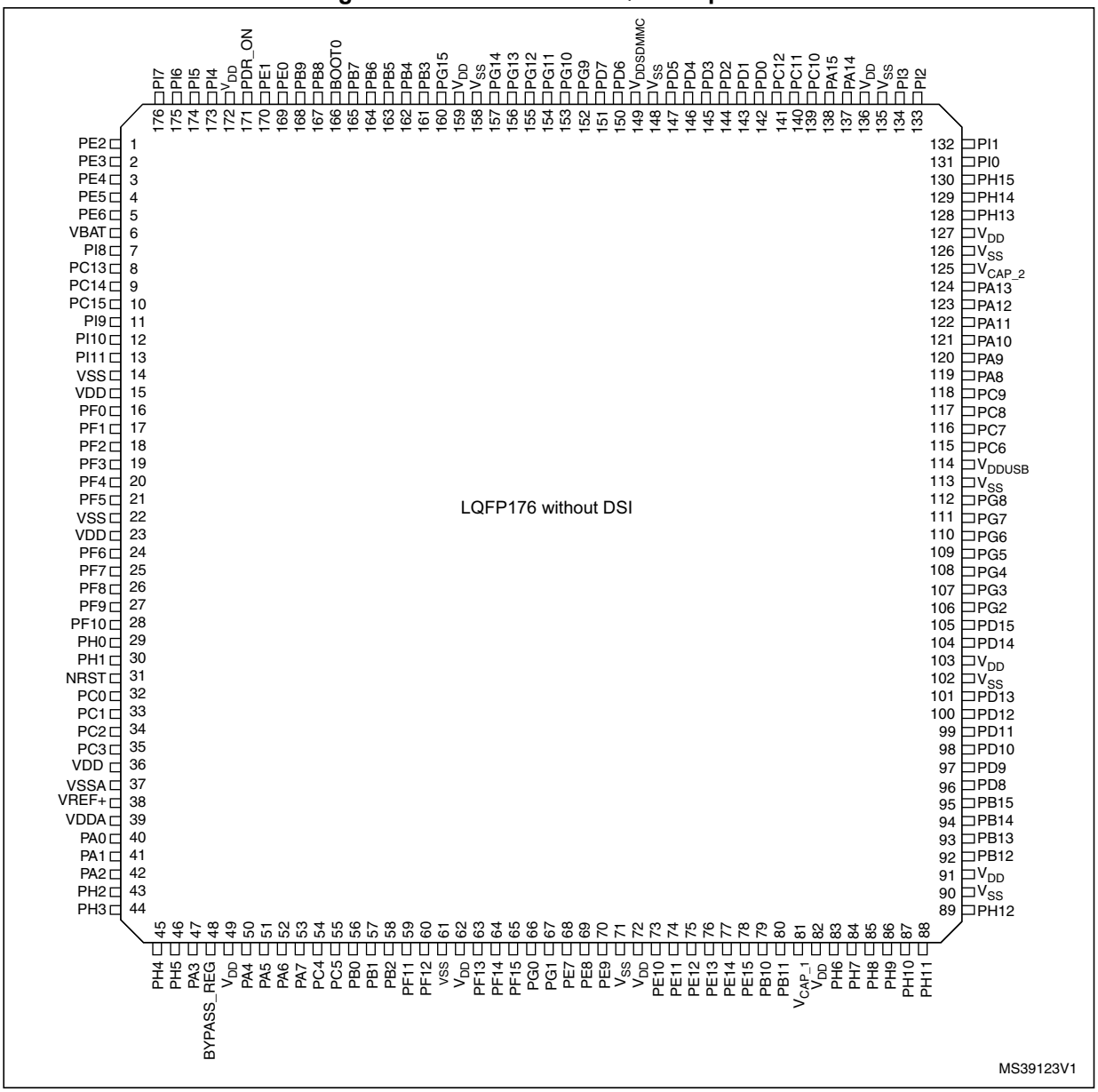
  - Refreshed by software
- DMA capability to read the final conversion data
- Interrupts: end of conversion, overrun, analog watchdog, short circuit, input serial channel clock absence
- “regular” or “injected” conversions:
  - “regular” conversions can be requested at any time or even in continuous mode without having any impact on the timing of “injected” conversions
  - “injected” conversions for precise timing and with high conversion priority

2.43 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with the temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the same input channel as V_{BAT}, ADC1_IN18, which is used to convert the sensor output voltage into a digital value. When the temperature sensor and V_{BAT} conversion are enabled at the same time, only V_{BAT} conversion is performed.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

Figure 13. STM32F76xxx LQFP176 pinout



1. The above figure shows the package top view.

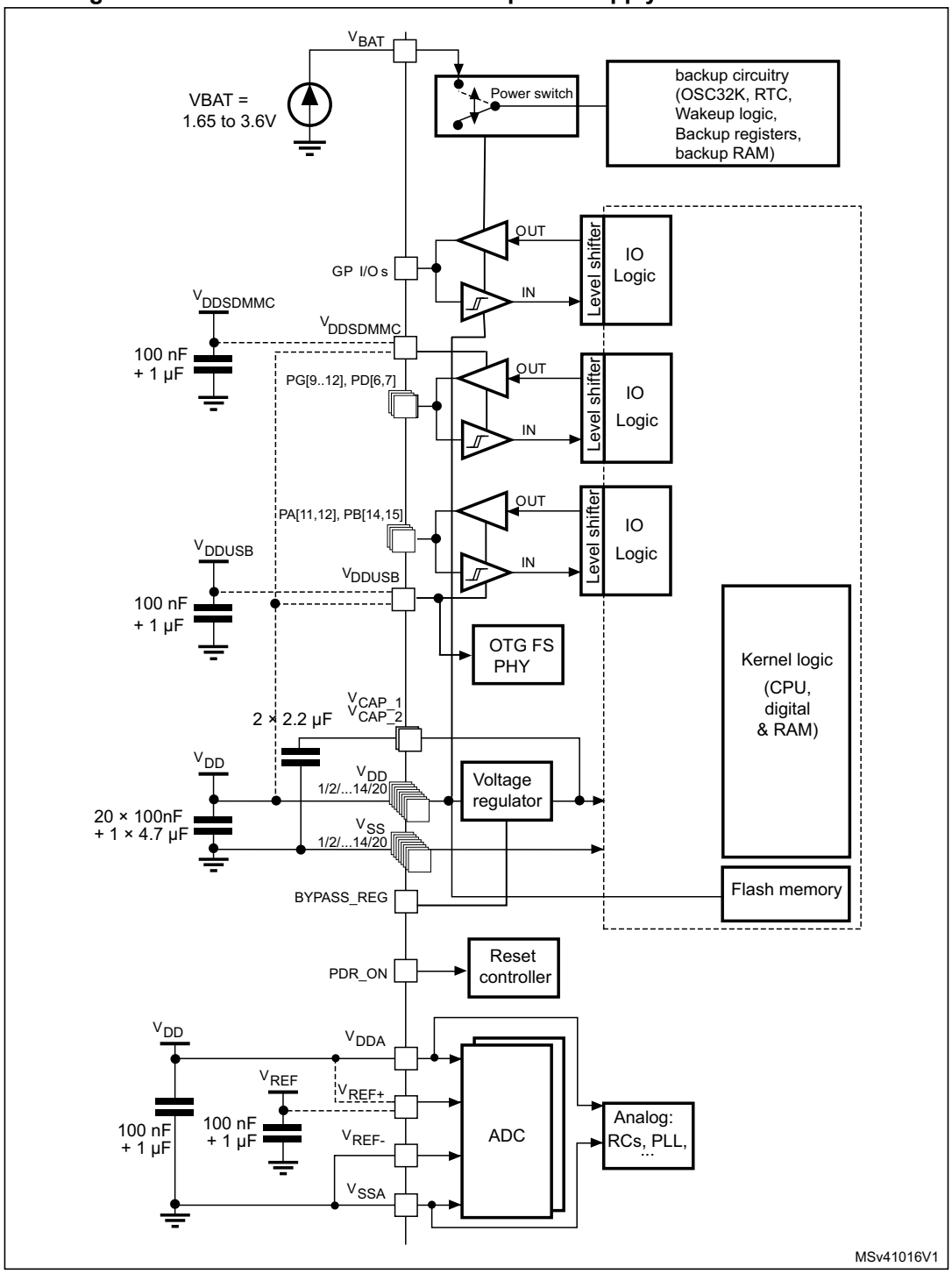
Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	-	F6	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	F7	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	F8	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	F9	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	F10	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	G6	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	G7	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	G8	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	G9	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	G10	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	H6	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	H7	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	H8	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	H9	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	H10	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	J6	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	J7	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	J8	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	J9	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	J10	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	K6	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	K7	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	K8	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	K9	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	K10	-	-	-	-	-	-	-	VSS	S	-	-	-	-

Table 12. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM1/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port A	PA0	-	TIM2_CH1/TIM2_ETR	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS	UART4_TX	-	SAI2_SD_B	ETH_MII_CRS	-	-	-	EVENTOUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS	UART4_RX	QUADSPI_BK1_IO3	SAI2_MCK_B	ETH_MII_RX_CLK/ETH_RMII_REF_CLK	-	-	LCD_R2	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_TX	SAI2_SCK_B	-	-	ETH_MDIO	MDIOS_MDIO	-	LCD_R1	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	-	USART2_RX	-	LCD_B2	OTG_HS_ULPI_D0	ETH_MII_COL	-	-	LCD_B5	EVENTOUT
	PA4	-	-	-	-	-	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART2_CK	SPI6_NSS	-	-	-	OTG_HS_SOF	DCMI_HSYNC	LCD_VSYNC	EVENTOUT
	PA5	-	TIM2_CH1/TIM2_ETR	-	TIM8_CH1N	-	SPI1_SCK/I2S1_CK	-	-	SPI6_SCK	-	OTG_HS_ULPI_CK	-	-	-	LCD_R4	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	-	SPI6_MISO	TIM13_CH1	-	-	MDIOS_MDC	DCMI_PIXCLK	LCD_G2	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI/I2S1_SD	-	-	SPI6_MOSI	TIM14_CH1	-	ETH_MII_RX_DV/ETH_RMII_CRS_DV	FMC_SDNWE	-	-	EVENTOUT
	PA8	MCO1	TIM1_CH1	-	TIM8_BKIN2	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	CAN3_RX	UART7_RX	LCD_B3	LCD_R6	EVENTOUT
	PA9	-	TIM1_CH2	-	-	I2C3_SMBA	SPI2_SCK/I2S2_CK	-	USART1_TX	-	-	-	-	-	DCMI_D0	LCD_R5	EVENTOUT
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_RX	-	LCD_B4	OTG_FS_ID	-	MDIOS_MDIO	DCMI_D1	LCD_B1	EVENTOUT

Figure 25. STM32F767xx/STM32F777xx power supply scheme



1. To connect BYPASS_REG and PDR_ON pins, refer to *Section 2.18: Power supply supervisor* and *Section 2.19: Voltage regulator*.
2. The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors when the voltage regulator is OFF.
3. The 4.7 µF ceramic capacitor must be connected to one of the V_{DD} pin.
4. V_{DDA}=V_{DD} and V_{SSA}=V_{SS}.

Table 30. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (Dual bank mode) on ITCM interface (ART disabled), regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					TA= 25 °C	TA=85 °C	TA=105 °C	
I_{DD}	Supply current in RUN mode	All peripherals enabled(2)(3)	216	191	218	255	-	mA
			200	178	195	241	269	
			180	164	179	214	236	
			168	147	160	192	212	
			144	121	130	157	175	
			60	60	66	93	111	
			25	28	33	59	77	
		All peripherals disabled(3)	216	93	104	150	-	
			200	87	97	144	171	
			180	83	92	126	148	
			168	75	82	114	134	
			144	65	71	97	115	
			60	35	40	66	84	
			25	16	20	47	64	

1. Guaranteed by characterization results, unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 36. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions	Typ(1)			Max(2)			Unit
			T_A = 25 °C			T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
			V_{DD} = 1.7 V	V_{DD}= 2.4 V	V_{DD} = 3.3 V	V_{DD} = 3.3 V			
I_{DD_STBY}	Supply current in Standby mode	Backup SRAM OFF, RTC and LSE OFF	1.1	1.9	2.4	5(3)	18(3)	38(3)	µA
		Backup SRAM ON, RTC and LSE OFF	1.9	2.7	3.2	6(3)	23(3)	48(3)	
		Backup SRAM OFF, RTC ON and LSE in low drive mode	1.7	2.7	3.5	7	26	55	
		Backup SRAM OFF, RTC ON and LSE in medium low drive mode	1.7	2.7	3.5	7	26	56	
		Backup SRAM OFF, RTC ON and LSE in medium high drive mode	1.8	2.8	3.6	8	28	57	
		Backup SRAM OFF, RTC ON and LSE in high drive mode	1.9	2.9	3.7	8	28	59	
		Backup SRAM ON, RTC ON and LSE in low drive mode	2.4	3.4	4.3	8	31	65	
		Backup SRAM ON, RTC ON and LSE in Medium low drive mode	2.4	3.5	4.3	8	31	65	
		Backup SRAM ON, RTC ON and LSE in Medium high drive mode	2.6	3.7	4.5	8	33	68	
		Backup SRAM ON, RTC ON and LSE in High drive mode	2.6	3.7	4.5	9	33	68	

1. The typical current consumption values are given with PDR OFF (internal reset OFF). When the PDR is OFF (internal reset OFF), the typical current consumption is reduced by additional 1.2 µA.
2. Guaranteed by characterization results, unless otherwise specified.
3. Guaranteed by test in production.

5.3.8 Wakeup time from low-power modes

The wakeup times given in *Table 40* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD}=3.3 V.

Table 40. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ(1)	Max(1)	Unit
$t_{WUSLEEP}$(2)	Wakeup from Sleep	-	13	13	CPU clock cycles
t_{WUSTOP}(2)	Wakeup from Stop mode with MR/LP regulator in normal mode	Main regulator is ON	14	14.9	µs
		Main regulator is ON and Flash memory in Deep power down mode	104.1	107.6	
		Low power regulator is ON	21.4	24.2	
		Low power regulator is ON and Flash memory in Deep power down mode	111.5	116.5	
t_{WUSTOP}(2)	Wakeup from Stop mode with MR/LP regulator in Under-drive mode	Main regulator in under-drive mode (Flash memory in Deep power-down mode)	107.4	113.2	
		Low power regulator in under-drive mode (Flash memory in Deep power-down mode)	112.7	120	
tWUSTDBY (2)	Wakeup from Standby mode	Exit Standby mode on rising edge	308	313	
		Exit Standby mode on falling edge	307	313	

1. Guaranteed by characterization results.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first

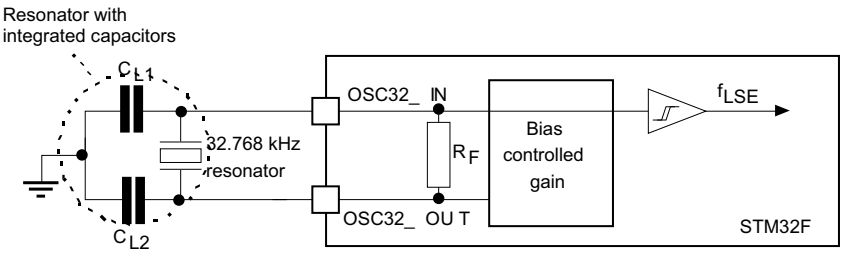
Table 44. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_m_crit_max	Maximum critical crystal g_m	LSEDRV[1:0]=00 Low drive capability	-	-	0.48	µA/V
		LSEDRV[1:0]=10 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0]=01 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0]=11 High drive capability	-	-	2.7	
t_{SU}(2)	start-up time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Guaranteed by characterization results. t_{SU} is the start-up time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 31. Typical application with a 32.768 kHz crystal



1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

5.3.17 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 60*. They are based on the EMS levels and classes defined in application note AN1709.

Table 60. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 216 MHz, conforms to IEC 61000-4-2	2B
V_{FTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A =+25 °C, f_{HCLK} = 168 MHz, conforms to IEC 61000-4-2	5A

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Table 74. ADC static accuracy at f_{ADC} = 36 MHz

Symbol	Parameter	Test conditions	Typ	Max(1)	Unit
ET	Total unadjusted error	f_{ADC} =36 MHz, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V $V_{DDA} - V_{REF} < 1.2$ V	±4	±7	LSB
EO	Offset error		±2	±3	
EG	Gain error		±3	±6	
ED	Differential linearity error		±2	±3	
EL	Integral linearity error		±3	±6	

1. Guaranteed by characterization results.

Table 75. ADC dynamic accuracy at f_{ADC} = 18 MHz - limited test conditions(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} =18 MHz $V_{DDA} = V_{REF+}$= 1.7 V Input Frequency = 20 KHz Temperature = 25 °C	10.3	10.4	-	bits
SINAD	Signal-to-noise and distortion ratio		64	64.2	-	dB
SNR	Signal-to-noise ratio		64	65	-	
THD	Total harmonic distortion		− 67	− 72	-	

1. Guaranteed by characterization results.

Table 76. ADC dynamic accuracy at f_{ADC} = 36 MHz - limited test conditions(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} =36 MHz $V_{DDA} = V_{REF+}$ = 3.3 V Input Frequency = 20 KHz Temperature = 25 °C	10.6	10.8	-	bits
SINAD	Signal-to noise and distortion ratio		66	67	-	dB
SNR	Signal-to noise ratio		64	68	-	
THD	Total harmonic distortion		− 70	− 72	-	

1. Guaranteed by characterization results.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.20* does not affect the ADC accuracy.

Table 97. Dynamics characteristics: Ethernet MAC signals for RMII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	1	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	2	-	-	
$t_{su(CRS)}$	Carrier sense setup time	2	-	-	
$t_{ih(CRS)}$	Carrier sense hold time	2	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	7.5	8	12	
$t_{d(TXD)}$	Transmit data valid delay time	7	7.5	12.5	

1. Guaranteed by characterization results.

Table 98 gives the list of Ethernet MAC signals for MII and *Figure 58* shows the corresponding timing diagram.

Figure 59. Ethernet MII timing diagram

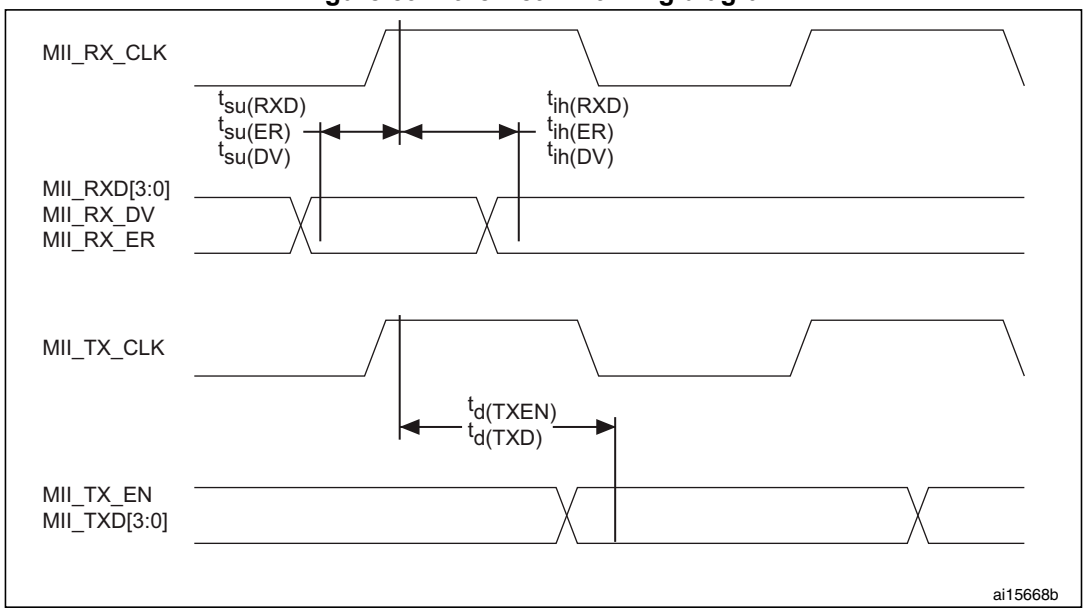


Table 98. Dynamics characteristics: Ethernet MAC signals for MII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	1	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	2.5	-	-	
$t_{su(DV)}$	Data valid setup time	1.5	-	-	
$t_{ih(DV)}$	Data valid hold time	0.5	-	-	
$t_{su(ER)}$	Error setup time	2.5	-	-	
$t_{ih(ER)}$	Error hold time	0.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	10	8	13	
$t_{d(TXD)}$	Transmit data valid delay time	9	7.5	13	

Table 108. Synchronous multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}$ – 0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH\_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	T_{HCLK} + 0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	T_{HCLK} – 0.5	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	1.5	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	3.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. Guaranteed by characterization results.

Table 114. SDRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK} + 0.5$	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	1.5	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	1.5	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	3.5	
$t_{d(SDCLKL-SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	0.5	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0.5	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

Table 115. LPSDR SDRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{W(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK} + 0.5$	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	0	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	4.5	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	2.5	
$t_{d(SDCLKL\_SDNE)}$	Chip select valid time	-	2.5	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL\_SDNRAS}$	SDNRAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

Table 118. Quad-SPI characteristics (continued)in SDR mode(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tw(CKH)	Quad-SPI clock high and low time	-	t(CK)/2 - 1	-	t(CK)/2	ns
tw(CKL)			t(CK)/2	-	t(CK)/2 + 1	
ts(IN)	Data input setup time	-	0.5	-	-	
th(IN)	Data input hold time		3	-	-	
tv(OUT)	Data output valid time	2.7 V<V_{DD}<3.6 V	-	1.5	3.5	
		1.71 V<V_{DD}<3.6 V	-	1.5	2	
th(OUT)	Data output hold time	-	0.5	-	-	

1. Guaranteed by characterization results.

Table 119. Quad SPI characteristics in DDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Fck1/t(CK)	Quad-SPI clock frequency	2.7 V<V_{DD}<3.6 V CL=20 pF	-	-	80	MHz
		1.8 V<V_{DD}<3.6 V CL=15 pF	-	-	80	
		1.71 V<V_{DD}<3.6 V CL=10 pF	-	-	80	
tw(CKH)	Quad-SPI clock high and low time	-	t(CK)/2 - 1	-	t(CK)/2	ns
tw(CKL)			t(CK)/2	-	t(CK)/2 + 1	
ts(IN), tsf(IN)	Data input setup time	2.7 V<V_{DD}<3.6 V	0.75	-	-	
		1.71 V<V_{DD}<2 V	0.5	-	-	
thr(IN), thf(IN)	Data input hold time	2.7 V<V_{DD}<3.6 V	2	-	-	
		1.71 V<V_{DD}<2 V	3	-	-	
tvr(OUT), tvf(OUT)	Data output valid time	2.7 V<V_{DD}<3.6 V	-	8.5	10	
		1.71 V<V_{DD}<3.6 V DHHC=0	-	8	12	
		DHHC=1 Pres=1, 2...	-	T_{HCLK}/2 + 1.5	T_{HCLK}/2 + 2.5	
thr(OUT), thf(OUT)	Data output hold time	DHHC=0	7.5	-	-	
		DHHC=1 Pres=1, 2...	T_{HCLK}/2 + 0.5	-	-	

1. Guaranteed by characterization results.

Table 123. Dynamic characteristics: SD / MMC characteristics, V_{DD}=2.7V to 3.6V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDMMC_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	fpp =50 MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50 MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	fpp =50 MHz	3.5	-	-	ns
t_{IH}	Input hold time HS	fpp =50 MHz	2.5	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	fpp =50 MHz	-	11	12	ns
t_{OH}	Output hold time HS	fpp =50 MHz	9	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
tISUD	Input setup time SD	fpp =25 MHz	3.5	-	-	ns
tIHD	Input hold time SD	fpp =25 MHz	2.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
tOVD	Output valid default time SD	fpp =25 MHz	-	0.5	1.5	ns
tOHD	Output hold default time SD	fpp =25 MHz	0	-	-	

1. Guaranteed by characterization results.

Table 124. Dynamic characteristics: eMMC characteristics, V_{DD}=1.71V to 1.9V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDMMC_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	fpp =50 MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50 MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	fpp =50 MHz	3	-	-	ns
t_{IH}	Input hold time HS	fpp =50 MHz	4	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	fpp =50 MHz	-	11	15.5	ns
t_{OH}	Output hold time HS	fpp =50 MHz	9.5	-	-	

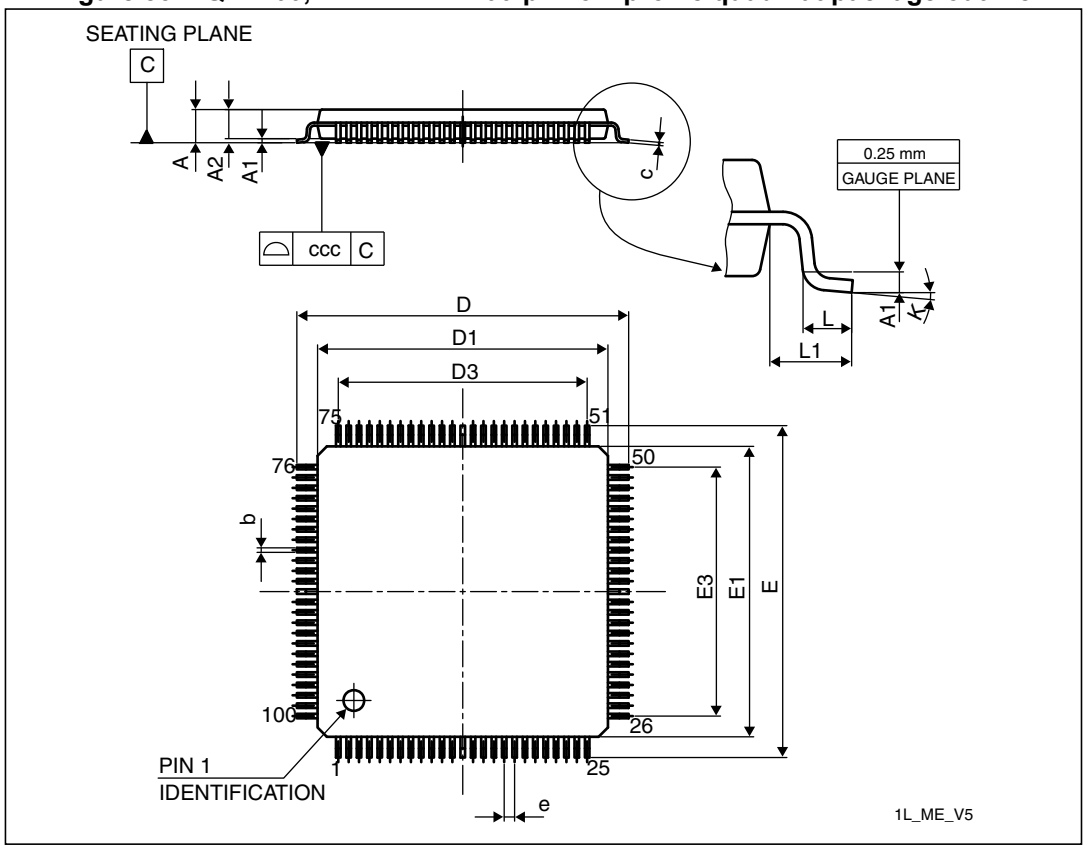
1. Guaranteed by characterization results.
2. Cload = 20 pF.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

6.1 LQFP100 14x 14 mm, low-profile quad flat package information

Figure 83. LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline



1. Drawing is not to scale.