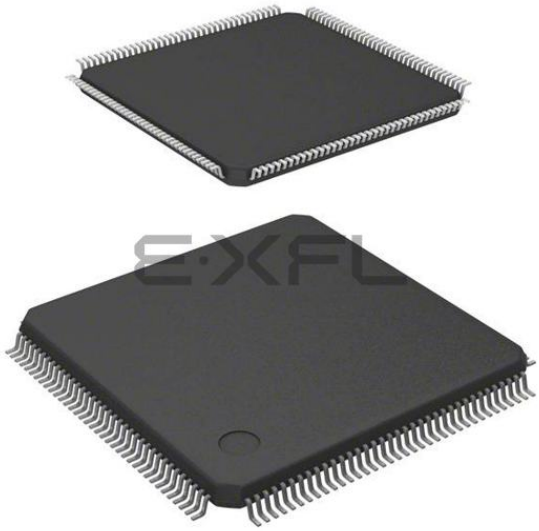

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f765zit6

Table 2. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx features and peripheral counts

Peripherals		STM32F 765Vx		STM32F767 /769Vx		STM32F 765Zx		STM32F767 /769Zx		STM32F 769Ax		STM32F 768Ax	STM32F 765Ix		STM32F767 /769Ix		STM32F 765Bx		STM32F767 /769Bx		STM32F 765Nx		STM32F767 /769Nx	
Flash memory in Kbytes		1024	2048	1024	2048	1024	2048	1024	2048	1024	2048	2048	1024	2048	1024	2048	1024	2048	1024	2048	1024	2048	1024	2048
SRAM in Kbytes	System	512(368+16+128)																						
	Instruction	16																						
	Backup	4																						
FMC memory controller		Yes(1)																						
Quad-SPI		Yes																						
Ethernet		Yes								No		Yes												
Timers	General-purpose	10																						
	Advanced-control	2																						
	Basic	2																						
	Low-power	1																						
Random number generator		Yes																						
Communication interfaces	SPI / I^2S	4/3 (simplex)(2)				6/3 (simplex)(2)																		
	I^2C	4																						
	USART/UART	4/4																						
	USB OTG FS	Yes																						
	USB OTG HS	Yes																						
	CAN	3																						
	SAI	2																						
	SPDIFRX	4 inputs																						
	SDMMC1	Yes																						
	SDMMC2	Yes(3)																						
Camera interface		Yes																						
MIPI-DSI Host(4)		No								Yes			No		Yes		No		Yes		No		Yes	
LCD-TFT		No		Yes		No		Yes					No		Yes		No		Yes		No		Yes	

2.8 Flexible memory controller (FMC)

The Flexible memory controller (FMC) includes three memory controllers:

- The NOR/PSRAM memory controller
- The NAND/memory controller
- The Synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) controller

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM (4 memory banks)
  - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories
- 8-,16-,32-bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is HCLK/2

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

2.9 Quad-SPI memory interface (QUADSPI)

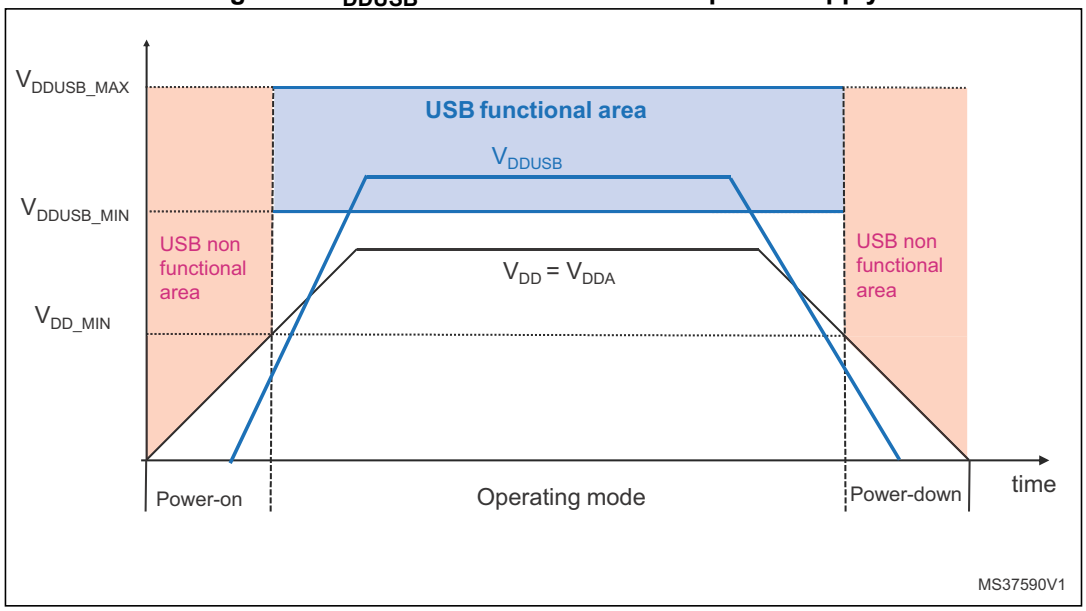
All the devices embed a Quad-SPI memory interface, which is a specialized communication interface targetting Single, Dual or Quad-SPI Flash memories. It can work in:

- Direct mode through registers
- External Flash status register polling mode
- Memory mapped mode.

Up to 256 Mbytes external Flash are memory mapped, supporting 8, 16 and 32-bit access. Code execution is supported.

The opcode and the frame format are fully programmable. The communication can be either in Single Data Rate or Dual Data Rate.

Figure 5. V_{DDUSB} connected to external power supply



The DSI (Display Serial Interface) sub-system uses several power supply pins which are independent from the other supply pins:

- V_{DDDSI} is an independent DSI power supply dedicated for DSI Regulator and MIPI D-PHY. This supply must be connected to global V_{DD}.
- The V_{CAPDSI} pin is the output of DSI Regulator (1.2V) which must be connected externally to $V_{DD12DSI}$.
- The $V_{DD12DSI}$ pin is used to supply the MIPI D-PHY, and to supply the clock and data lanes pins. An external capacitor of 2.2 uF must be connected on the $V_{DD12DSI}$ pin.
- The V_{SSDSI} pin is an isolated supply ground used for DSI sub-system.
- If the DSI functionality is not used at all, then:
  - The V_{DDDSI} pin must be connected to global V_{DD}.
  - The V_{CAPDSI} pin must be connected externally to $V_{DD12DSI}$ but the external capacitor is no more needed.
  - The V_{SSDSI} pin must be grounded.

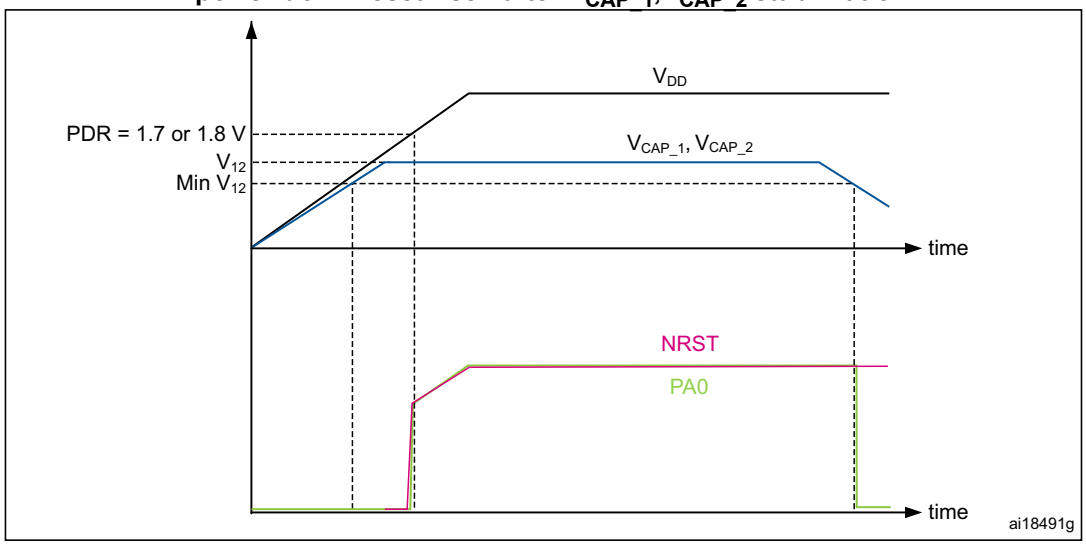
2.18 Power supply supervisor

2.18.1 Internal reset ON

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On the other packages, the power supply supervisor is always enabled.

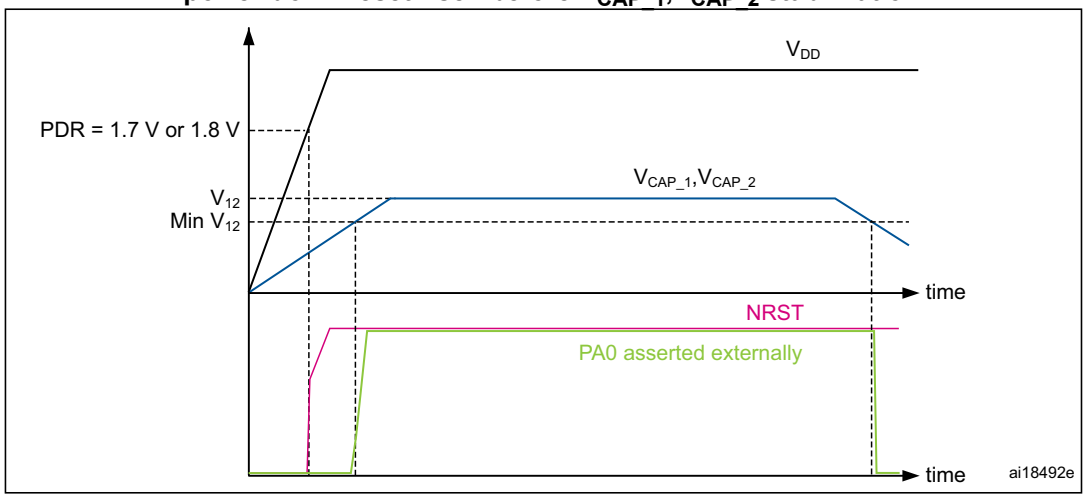
The device has an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR thresholds, or to disable BOR permanently. Three BOR thresholds are available through

Figure 9. Startup in regulator OFF: slow V_{DD} slope - power-down reset risen after V_{CAP_1},V_{CAP_2} stabilization



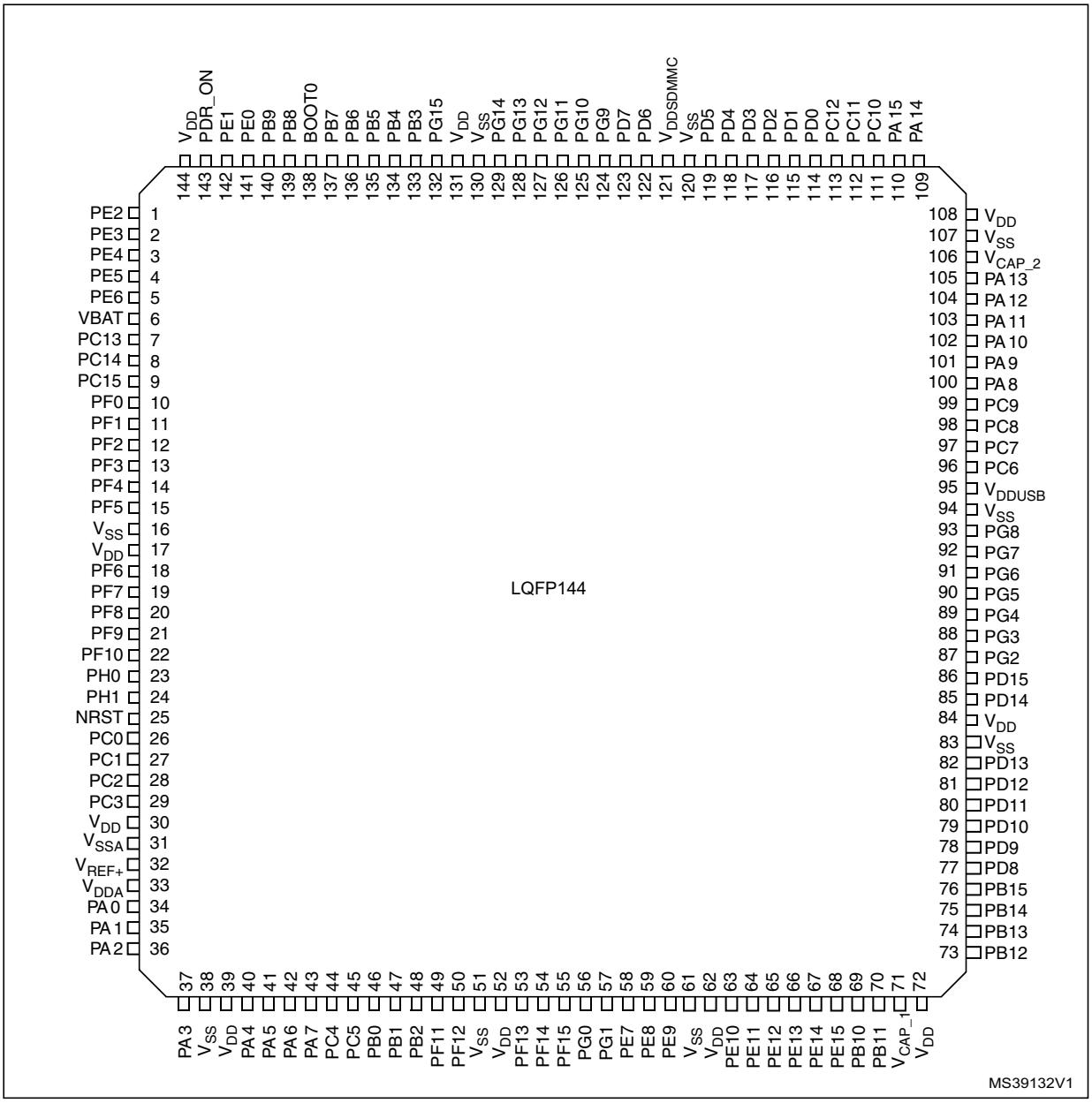
1. This figure is valid whatever the internal reset mode (ON or OFF).

Figure 10. Startup in regulator OFF mode: fast V_{DD} slope - power-down reset risen before V_{CAP_1},V_{CAP_2} stabilization



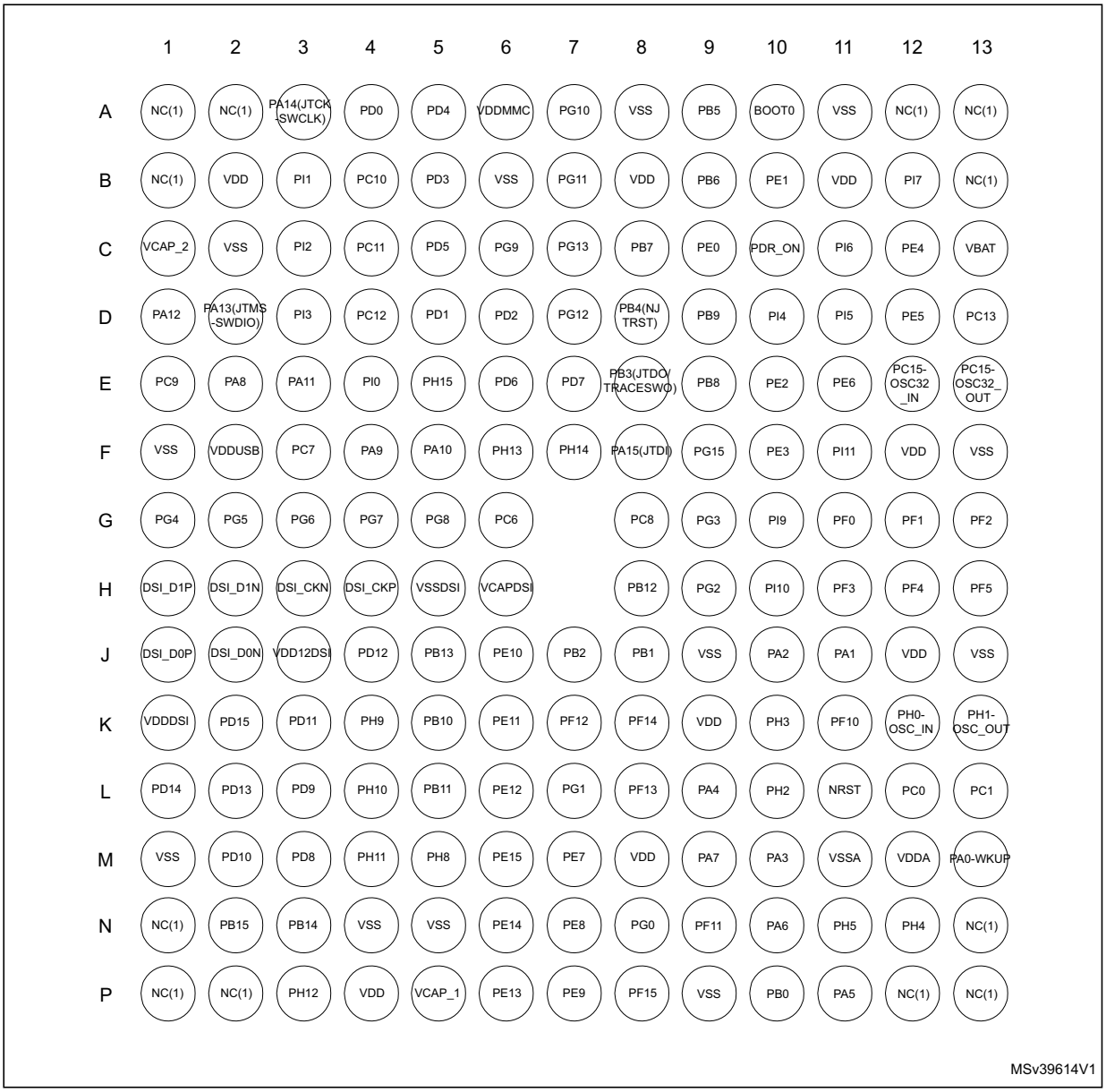
1. This figure is valid whatever the internal reset mode (ON or OFF).

Figure 12. STM32F76xxx LQFP144 pinout



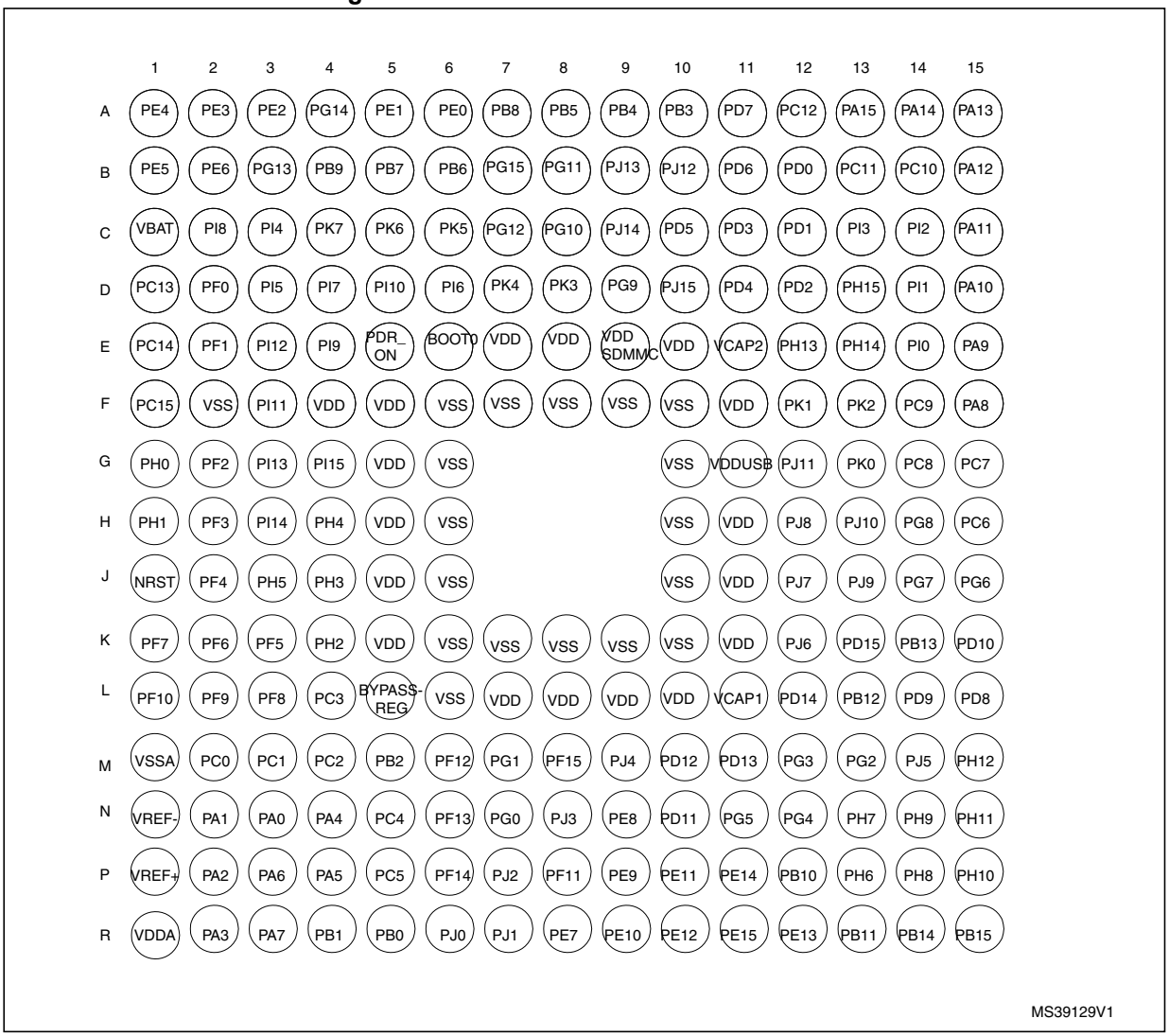
1. The above figure shows the package top view.

Figure 15. STM32F769Ax/STM32F768Ax WLCSP180 ballout



1. NC ball must not be connected to GND nor to VDD.
2. The above figure shows the package top view.

Figure 19. STM32F76xxx TFBGA216 ballout



1. The above figure shows the package top view.

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	-	-	-	60	L6	-	-	60	L6	VSS	S	-	-	-	-
34	46	R5	56	61	R5	P10	56	61	R5	PB0	I/O	FT	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, DFSDM1_CKOUT, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, LCD_G1, EVENTOUT	ADC1_IN8, ADC2_IN8
35	47	R4	57	62	R4	J8	57	62	R4	PB1	I/O	FT	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN1, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, LCD_G0, EVENTOUT	ADC1_IN9, ADC2_IN9
36	48	M6	58	63	M5	J7	58	63	M5	PB2	I/O	FT	-	SAI1_SD_A, SPI3_MOSI/I2S3_SD, QUADSPI_CLK, DFSDM1_CKIN1, EVENTOUT	-
-	-	-	-	64	G4	NC	-	64	G4	PI15	I/O	FT	-	LCD_G2, LCD_R0, EVENTOUT	-
-	-	-	-	65	R6	NC	-	65	R6	PJ0	I/O	FT	-	LCD_R7, LCD_R1, EVENTOUT	-
-	-	-	-	66	R7	NC	-	66	R7	PJ1	I/O	FT	-	LCD_R2, EVENTOUT	-
-	-	-	-	67	P7	NC	-	67	P7	PJ2	I/O	FT	-	DSI_TE, LCD_R3, EVENTOUT	-
-	-	-	-	68	N8	NC	-	68	N8	PJ3	I/O	FT	-	LCD_R4, EVENTOUT	-
-	-	-	-	69	M9	NC	-	69	M9	PJ4	I/O	FT	-	LCD_R5, EVENTOUT	-
-	49	R6	59	70	P8	N9	59	70	P8	PF11	I/O	FT	-	SPI5_MOSI, SAI2_SD_B, FMC_SDNRAS, DCMI_D12, EVENTOUT	-
-	50	P6	60	71	M6	K7	60	71	M6	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	-	K12	89	102	M15	P3	-	102	M15	PH12	I/O	FT	-	TIM5_CH3, I2C4_SDA, FMC_D20, DCMI_D3, LCD_R6, EVENTOUT	-
-	-	H12	90	-	K10	N4	-	-	K10	VSS	S		-	-	-
-	-	J12	91	103	K11	-	-	103	K11	VDD	S		-	-	-
51	73	P12	92	104	L13	H8	85	104	L13	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, DFSDM1_DATIN1, USART3_CK, UART5_RX, CAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_RMII_TXD0, OTG_HS_ID, EVENTOUT	-
52	74	P13	93	105	K14	J5	86	105	K14	PB13	I/O	FT	-	TIM1_CH1N, SPI2_SCK/I2S2_CK, DFSDM1_CKIN1, USART3_CTS, UART5_TX, CAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, EVENTOUT	OTG_HS_VBUS
53	75	R14	94	106	R14	N3	87	106	R14	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, USART1_TX, SPI2_MISO, DFSDM1_DATIN2, USART3_RTS, UART4_RTS, TIM12_CH1, SDMMC2_D0, OTG_HS_DM, EVENTOUT	-
54	76	R15	95	107	R15	N2	88	107	R15	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, USART1_RX, SPI2_MOSI/I2S2_SD, DFSDM1_CKIN2, UART4_CTS, TIM12_CH2, SDMMC2_D1, OTG_HS_DP, EVENTOUT	-

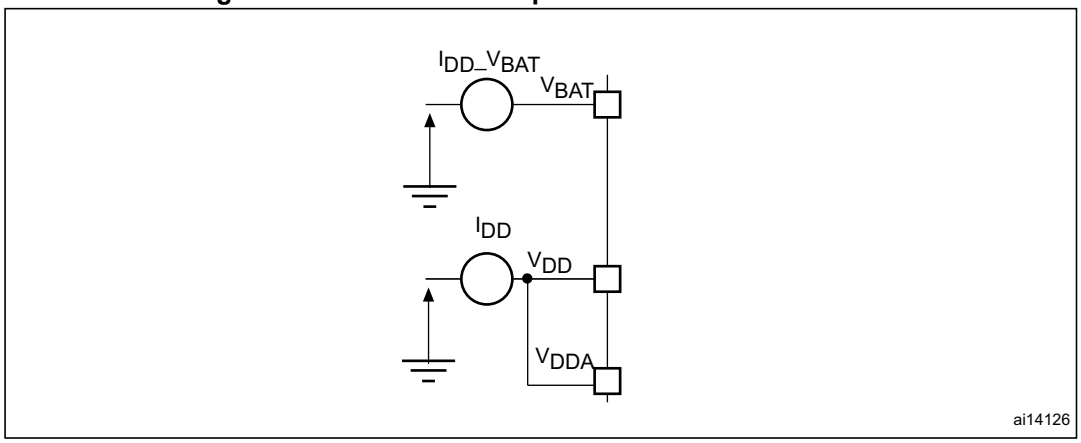
Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
55	77	P15	96	108	L15	M3	89	108	L15	PD8	I/O	FT	-	DFSDM1_CKIN3, USART3_TX, SPDIF_RX1, FMC_D13, EVENTOUT	-
56	78	P14	97	109	L14	L3	90	109	L14	PD9	I/O	FT	-	DFSDM1_DATIN3, USART3_RX, FMC_D14, EVENTOUT	-
57	79	N15	98	110	K15	M2	91	110	K15	PD10	I/O	FT	-	DFSDM1_CKOUT, USART3_CK, FMC_D15, LCD_B3, EVENTOUT	-
58	80	N14	99	111	N10	K3	92	111	N10	PD11	I/O	FT	-	I2C4_SMBA, USART3_CTS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16/FMC_CLE, EVENTOUT	-
59	81	N13	100	112	M10	J4	93	112	M10	PD12	I/O	FT	-	TIM4_CH1, LPTIM1_IN1, I2C4_SCL, USART3_RTS, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17/FMC_ALE, EVENTOUT	-
60	82	M15	101	113	M11	L2	94	113	M11	PD13	I/O	FT	-	TIM4_CH2, LPTIM1_OUT, I2C4_SDA, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18, EVENTOUT	-
-	83	-	102	114	J10	M1	95	114	J10	VSS	S		-	-	-
-	84	J13	103	115	J11	-	96	115	J11	VDD	S		-	-	-
61	85	M14	104	116	L12	L1	97	116	L12	PD14	I/O	FT	-	TIM4_CH3, UART8_CTS, FMC_D0, EVENTOUT	-
62	86	L14	105	117	K13	K2	98	117	K13	PD15	I/O	FT	-	TIM4_CH4, UART8_RTS, FMC_D1, EVENTOUT	-
-	-	-	-	118	K12	-	-	-	-	PJ6	I/O	FT	-	LCD_R7, EVENTOUT	-
-	-	-	-	119	J12	-	-	-	-	PJ7	I/O	FT	-	LCD_G0, EVENTOUT	-

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

5.1.7 Current consumption measurement

Figure 26. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 14: Voltage characteristics*, *Table 15: Current characteristics*, and *Table 16: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. The device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard. Extended mission profiles are available on demand.

Table 14. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{DD}, V_{BAT}, V_{DDUSB}, V_{DDDSI} (1) and $V_{DDSDMMC}$)(2)	− 0.3	4.0	V
V_{IN}	Input voltage on FT pins(3)	V_{SS} − 0.3	V_{DD}+4.0	
	Input voltage on TTa pins	V_{SS} − 0.3	4.0	
	Input voltage on any other pin	V_{SS} − 0.3	4.0	
	Input voltage on BOOT pin	V_{SS}	9.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins(4)	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.18: Absolute maximum ratings (electrical sensitivity)*		-

Table 31. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (Single bank mode, ART ON except prefetch / L1-cache ON) or SRAM on AXI (L1-cache ON), regulator OFF

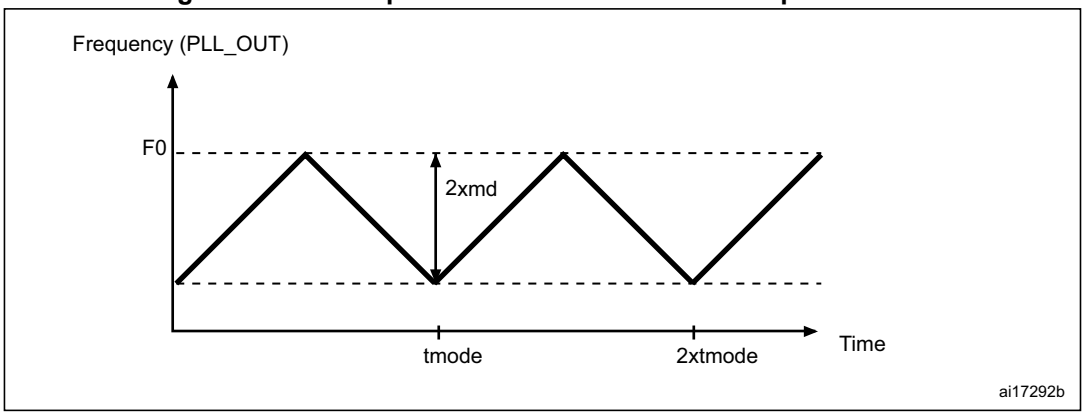
Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ		Max(1)						Unit
						TA= 25 °C		TA= 85 °C		TA= 105 °C		
				IDD12	IDD	IDD12	IDD	IDD12	IDD	IDD12	IDD	
IDD12/ IDD	Supply current in RUN mode from V12 and VDD supply	All Peripherals Enabled(2)(3)	180	152	1	167	2	200	2	220	2	mA
			168	136	1	148	2	179	2	198	2	
			144	105	1	115	2	141	2	158	2	
			60	47	1	53	2	79	2	96	2	
			25	22	1	27	2	53	2	70	2	
		All Peripherals Disabled(3)	180	74	1	83	2	116	2	136	2	
			168	65	1	73	2	104	2	123	2	
			144	50	1	57	2	83	2	100	2	
			60	22	1	27	2	53	2	70	2	
			25	10	1	14	2	41	2	58	2	

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 32. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (Dual bank mode, ART ON except prefetch / L1-cache ON) or SRAM on AXI (L1-cache ON), regulator OFF

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ		Max(1)						Unit
						TA= 25 °C		TA= 85 °C		TA= 105 °C		
				IDD12	IDD	IDD12	IDD	IDD12	IDD	IDD12	IDD	
IDD12/ IDD	Supply current in RUN mode from V12 and VDD supply	All Peripherals Enabled(2)(3)	180	152	1	167	2	200	2	220	2	mA
			168	136	1	148	2	179	2	198	2	
			144	105	1	115	2	141	2	158	2	
			60	47	1	53	2	79	2	96	2	
			25	22	1	27	2	53	2	70	2	
		All Peripherals Disabled(3)	180	74	1	82	2	114	2	137	2	
			168	65	1	73	2	104	2	123	2	
			144	50	1	57	2	83	2	100	2	
			60	22	1	27	2	53	2	70	2	
			25	10	1	14	2	41	2	58	2	

Figure 35. PLL output clock waveforms in down spread mode



5.3.13 MIPI D-PHY characteristics

The parameters given in *Table 51* and *Table 52* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 51. MIPI D-PHY characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Hi-Speed Input/Output Characteristics						
U_{INST}	UI instantaneous	-	2	-	12.5	ns
V_{CMTX}	HS transmit common mode voltage	-	150	200	250	mV
$\|\Delta V_{CMTX}\|$	V_{CMTX} mismatch when output is Differential-1 or Differential-0	-	-	-	5	
$\|V_{OD}\|$	HS transmit differential voltage	-	140	200	270	
$\|\Delta V_{OD}\|$	V_{OD} mismatch when output is Differential-1 or Differential-0	-	-	-	14	
V_{OHHS}	HS output high voltage	-	-	-	360	
Z_{OS}	Single ended output impedance	-	40	50	62.5	Ω
ΔZ_{OS}	Single ended output impedance mismatch	-	-	-	10	%
t_{HSr} & t_{HSf}	20%-80% rise and fall time	-	100	-	0.35*UI	ps
LP Receiver Input Characteristics						
V_{IL}	Logic 0 input voltage (not in ULP State)	-	-	-	550	mV
$V_{IL-ULPS}$	Logic 0 input voltage in ULP State	-	-	-	300	
V_{IH}	Input high level voltage	-	880	-	-	
V_{hys}	Voltage hysteresis	-	25	-	-	
LP Emitter Output Characteristics						

5.3.21 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 65: I/O static characteristics*).

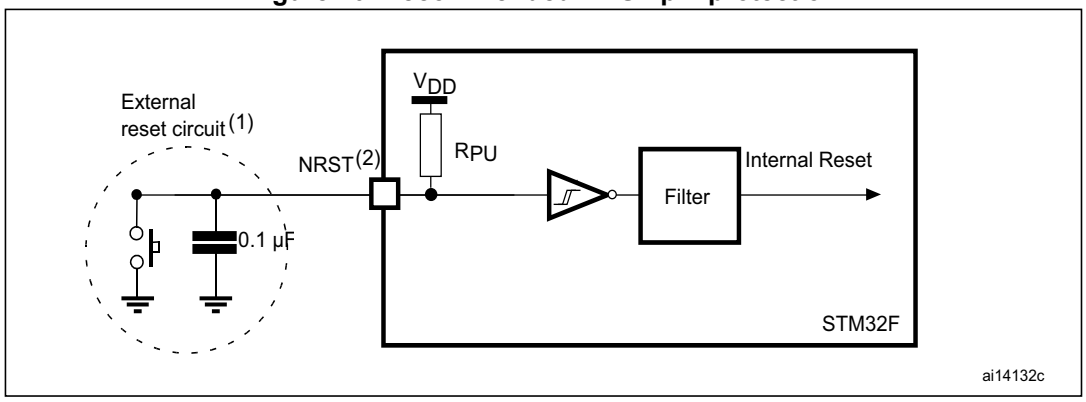
Unless otherwise specified, the parameters given in *Table 68* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 68. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(2)	NRST Input not filtered pulse	$V_{DD} > 2.7$ V	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	µs

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

Figure 40. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 68*. Otherwise the reset is not taken into account by the device.

I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 86* for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

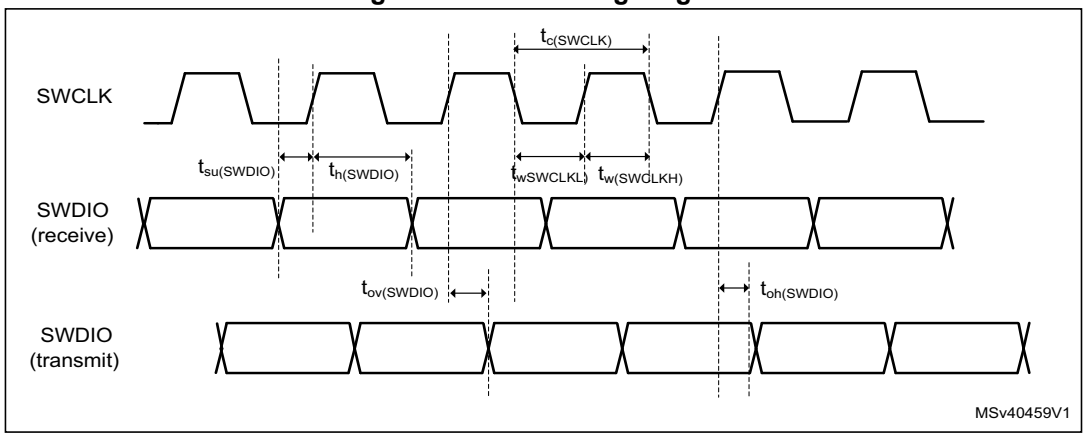
Table 86. I²S dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256x8K	256xFs(2)	MHz
f_{CK}	I2S clock frequency	Master data	-	64xFs	MHz
		Slave data	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	3	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	5	-	
$t_{h(WS)}$	WS hold time	Slave mode	2	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	2.5	-	
$t_{su(SD\_SR)}$		Slave receiver	2.5	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	3.5	-	
$t_{h(SD\_SR)}$		Slave receiver	2	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	12	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	3	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	5	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	0	-	

1. Guaranteed by characterization results.
2. The maximum value of 256xFs is 49.152 MHz (APB1 maximum frequency).

*Note: Refer to RM0410 reference manual I2S section for more details about the sampling frequency (F_S). f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). F_S maximum value is supported for each mode/condition.*

Figure 52. SWD timing diagram



SAI characteristics:

Unless otherwise specified, the parameters given in *Table 89* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: $0.5V_{DD}$

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 89. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	SAI Main clock output	-	256 x 8K	256xFs	MHz
F_{CK}	SAI clock frequency(2)	Master data: 32 bits	-	128xFs(3)	MHz
		Slave data: 32 bits	-	128xFs	
$t_{v(FS)}$	FS valid time	Master mode 2.7≤VDD≤3.6V	-	15	ns
		Master mode 1.71≤VDD≤3.6V	-	20	
$t_{su(FS)}$	FS setup time	Slave mode	7	-	
$t_{h(FS)}$	FS hold time	Master mode	1	-	
		Slave mode	1	-	
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	3	-	
$t_{su(SD\_B\_SR)}$		Slave receiver	3.5	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	5	-	
$t_{h(SD\_B\_SR)}$		Slave receiver	1	-	

1. Guaranteed by characterization results.

Figure 68. Synchronous non-multiplexed PSRAM write timings

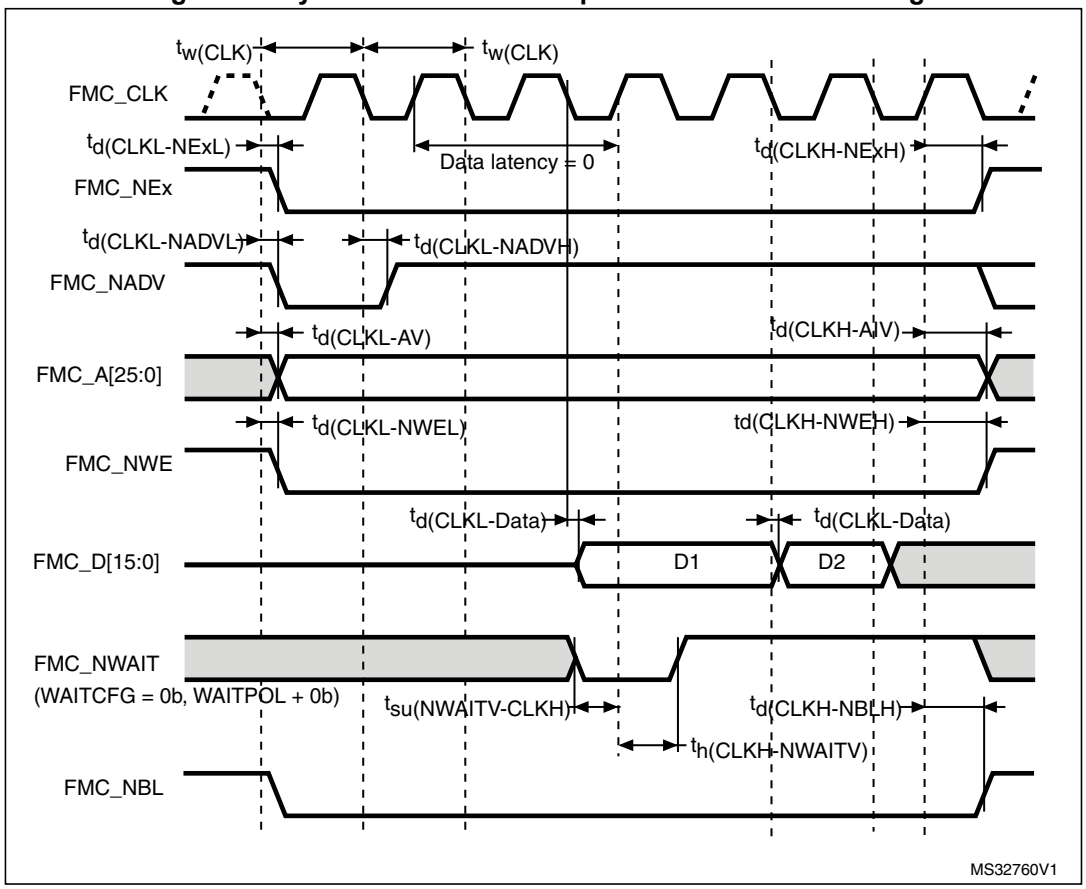
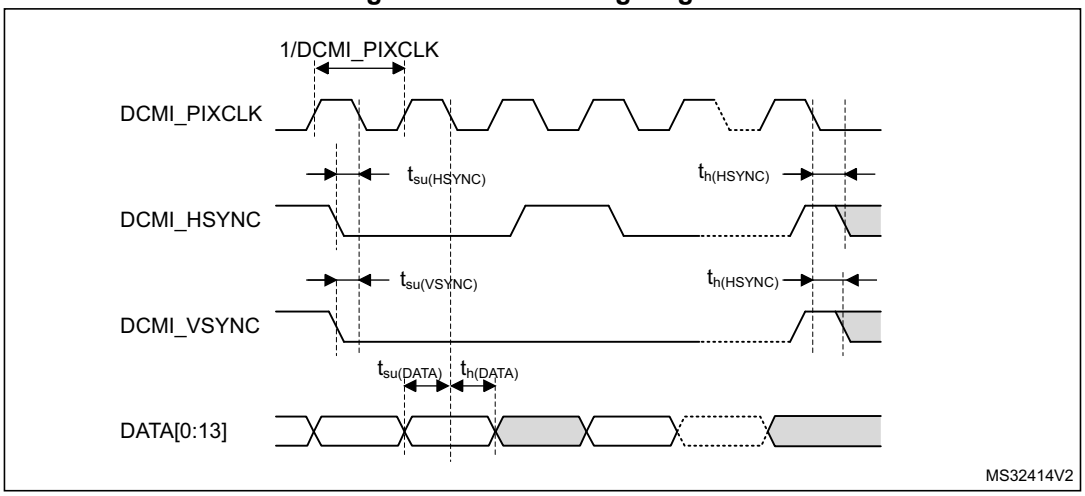


Figure 77. DCMI timing diagram



5.3.33 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in *Table 121* for LCD-TFT are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 17*, with the following configuration:

- LCD_CLK polarity: high
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits

Table 121. LTDC characteristics (1)

Symbol	Parameter	Min	Max	Unit
f_{CLK}	LTDC clock output frequency	-	65	MHz
D_{CLK}	LTDC clock output duty cycle	45	55	%
$t_{w(CLKH)}$, $t_{w(CLKL)}$	Clock High time, low time	tw(CLK)/2−0.5	tw(CLK)/2+0.5	ns
$t_{v(DATA)}$	Data output valid time	-	6	
$t_{h(DATA)}$	Data output hold time	0	-	
$t_{v(HSYNC)}$, $t_{v(VSYNC)}$, $t_{v(DE)}$	HSYNC/VSYNC/DE output valid time	-	3.5	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$, $t_{h(DE)}$	HSYNC/VSYNC/DE output hold time	0.5	-	

1. Guaranteed by characterization results.