Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	159
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f767bgt6

1 Description

The STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx devices are based on the high-performance ARM® Cortex®-M7 32-bit RISC core operating at up to 216 MHz frequency. The Cortex®-M7 core features a floating point unit (FPU) which supports ARM® double-precision and single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances the application security.

The STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx devices incorporate high-speed embedded memories with a Flash memory up to 2 Mbytes, 512 Kbytes of SRAM (including 128 Kbytes of Data TCM RAM for critical real-time data), 16 Kbytes of instruction TCM RAM (for critical real-time routines), 4 Kbytes of backup SRAM available in the lowest power modes, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses, a 32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memories access.

All the devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers, a true random number generator (RNG). They also feature standard and advanced communication interfaces.

- Up to four I^2Cs
- Six SPIs, three I^2Ss in half-duplex mode. To achieve audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI)
- Three CANs
- Two SAI serial audio interfaces
- Two SDMMC host interfaces
- Ethernet and camera interfaces
- LCD-TFT display controller
- Chrom-ART Accelerator™
- SPDIFRX interface
- HDMI-CEC

Advanced peripherals include two SDMMC interfaces, a flexible memory control (FMC) interface, a Quad-SPI Flash memory interface, a camera interface for CMOS sensors. Refer to *Table 2: STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx features and peripheral counts* for the list of peripherals available on each part number.

The STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx devices operate in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply. Dedicated supply inputs for USB (OTG_FS and OTG_HS) and SDMMC2 (clock, command and 4-bit data) are available on all the packages except LQFP100 for a greater power supply choice.

The supply voltage can drop to 1.7 V with the use of an external power supply supervisor (refer to *Section 2.18.2: Internal reset OFF*). A comprehensive set of power-saving mode allows the design of low-power applications.

option bytes. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

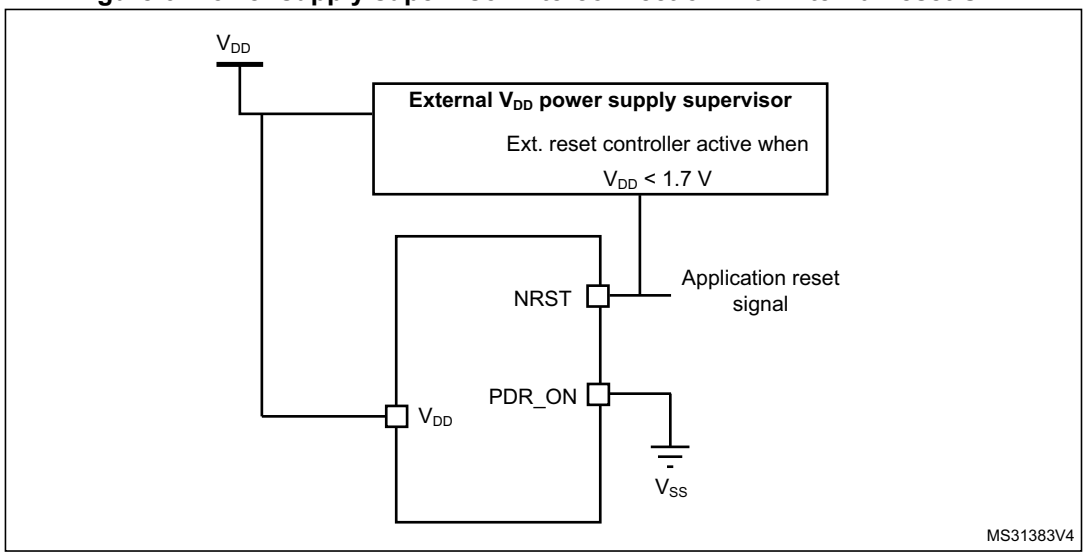
The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.18.2 Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled through the PDR_ON pin.

An external power supply supervisor should monitor V_{DD} and NRST and should maintain the device in reset mode as long as V_{DD} is below a specified threshold. PDR_ON should be connected to V_{SS}. Refer to *Figure 6: Power supply supervisor interconnection with internal reset OFF*.

Figure 6. Power supply supervisor interconnection with internal reset OFF



The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.7 V (see *Figure 7*).

A comprehensive set of power-saving mode allows to design low-power applications.

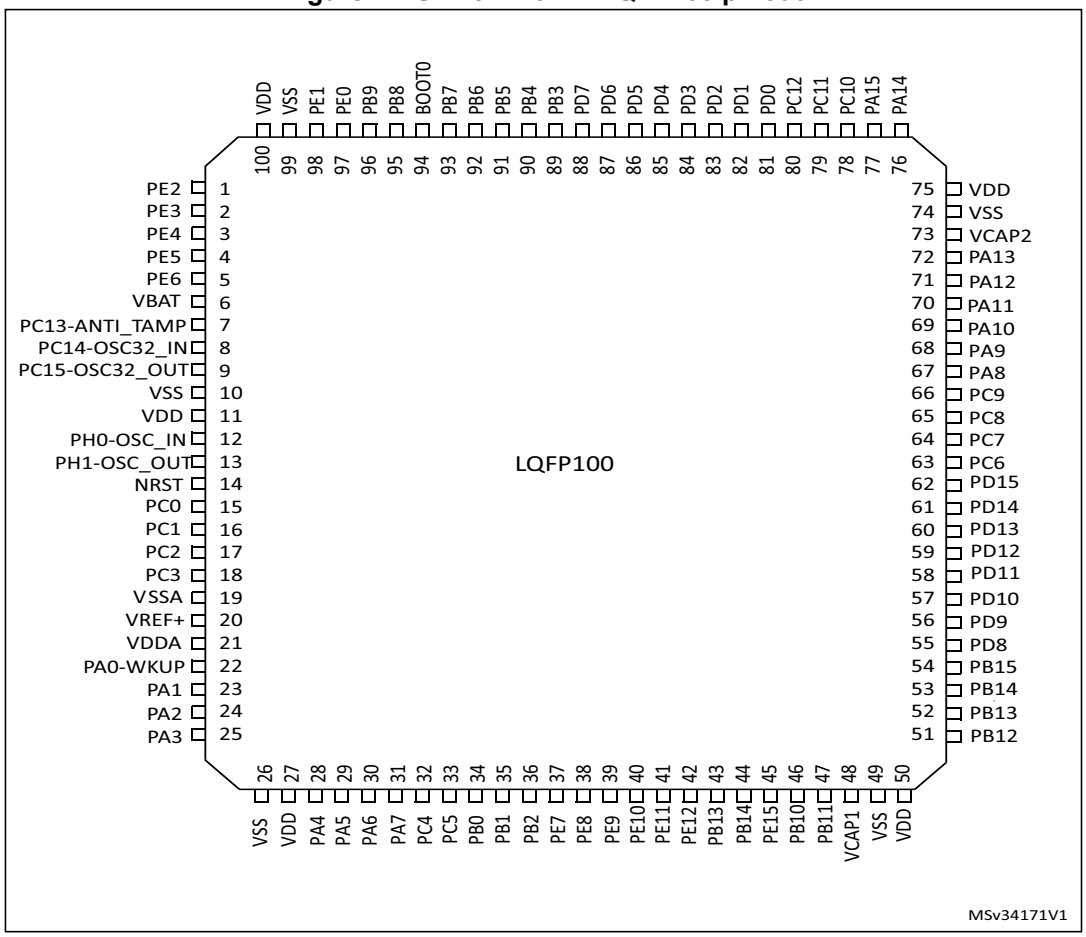
When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry must be disabled
- The embedded programmable voltage detector (PVD) is disabled
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}.

All the packages, except for the LQFP100, allow to disable the internal reset through the PDR_ON signal when connected to V_{SS}.

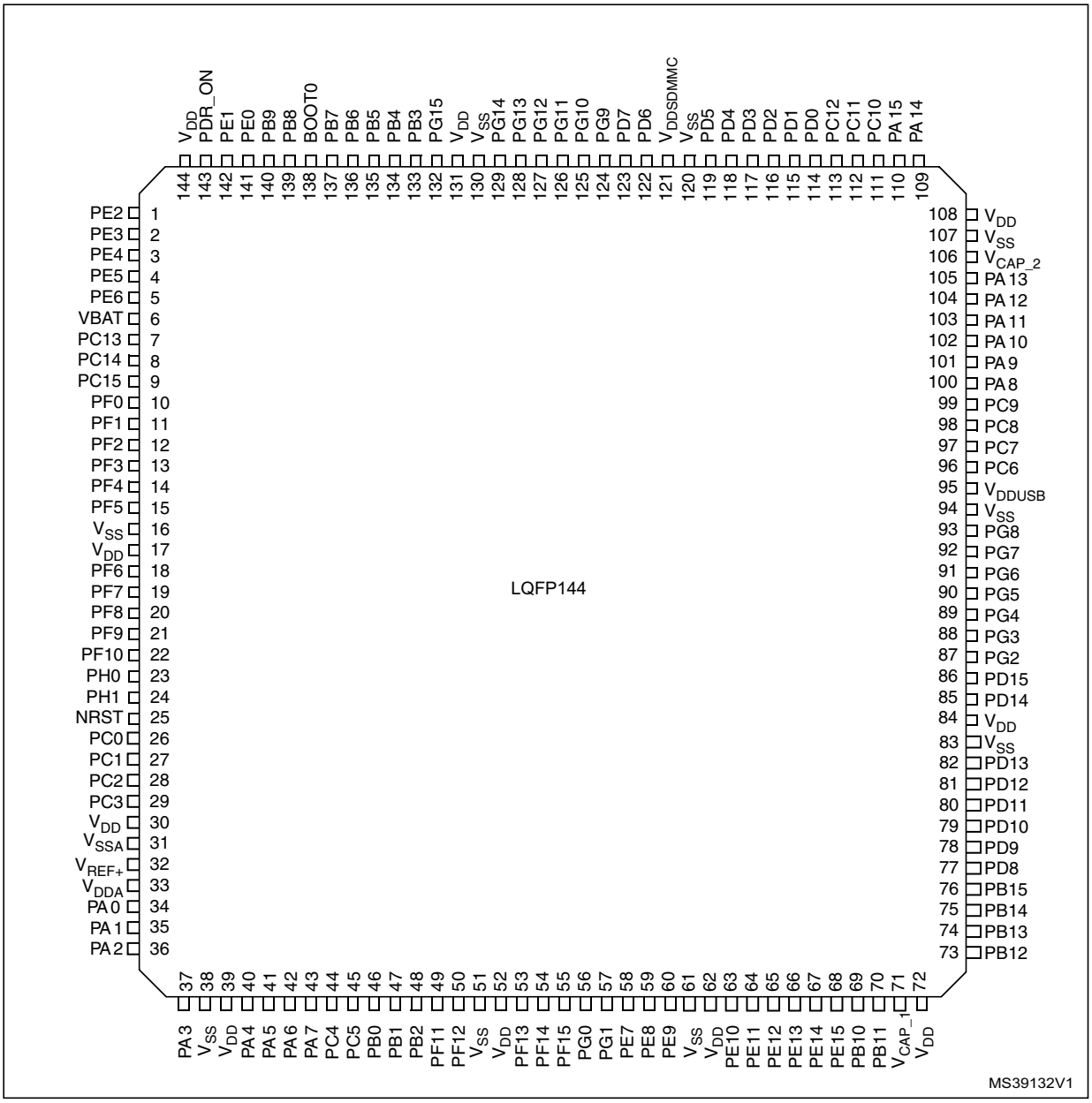
3 Pinouts and pin description

Figure 11. STM32F76xxx LQFP100 pinout



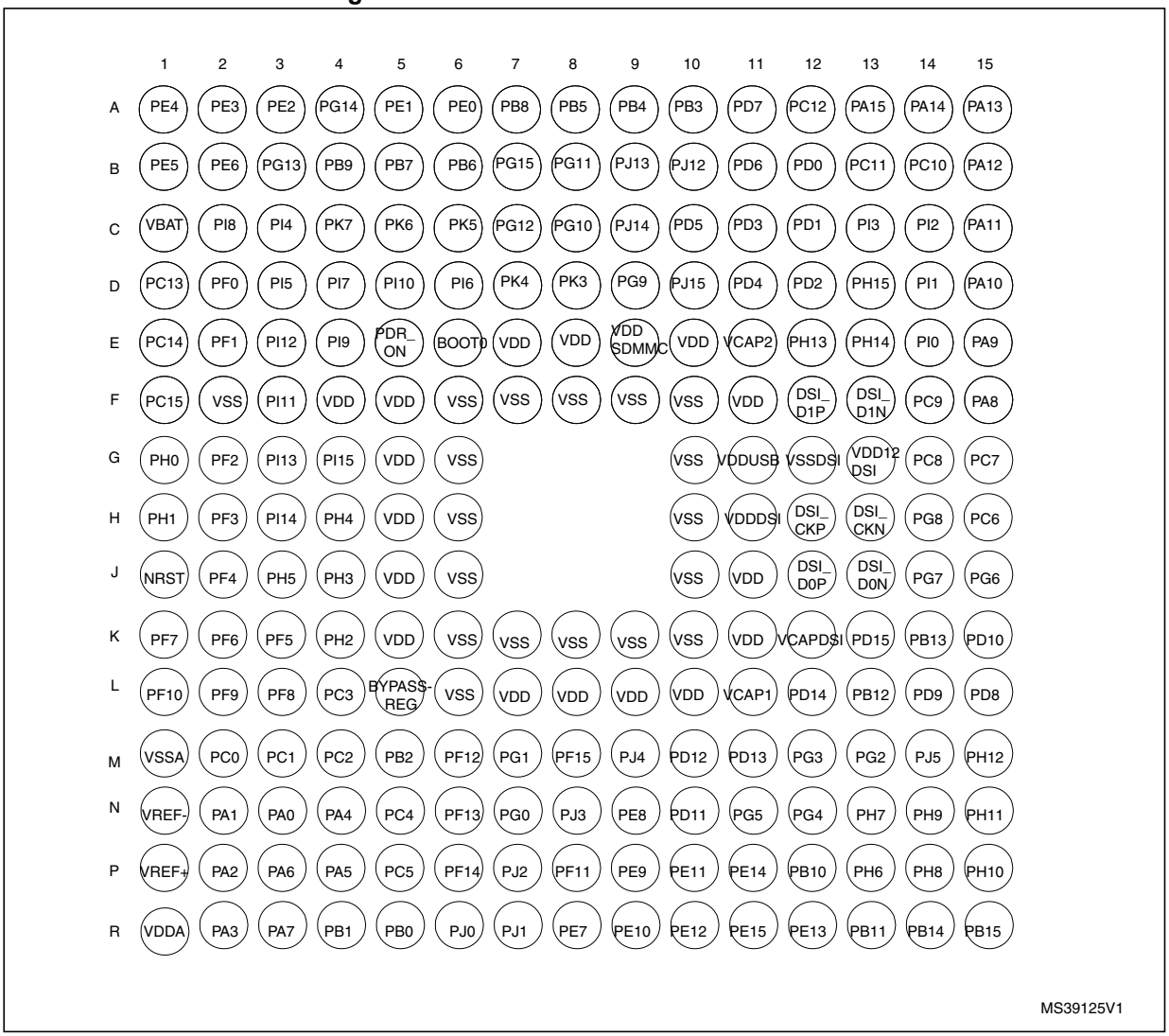
1. The above figure shows the package top view.

Figure 12. STM32F76xxx LQFP144 pinout



1. The above figure shows the package top view.

Figure 20. STM32F769xx TFBGA216 ballout



1. The above figure shows the package top view.

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
24	36	P2	42	45	P2	J10	42	45	P2	PA2	I/O	FT	-	TIM2_CH3, TIM5_CH3, TIM9_CH1, USART2_TX, SAI2_SCK_B, ETH_MDIO, MDIOS_MDIO, LCD_R1, EVENTOUT	ADC1_IN2, ADC2_IN2, ADC3_IN2, WKUP2
-	-	F4	43	46	K4	L10	43	46	K4	PH2	I/O	FT	-	LPTIM1_IN2, QUADSPI_BK2_IO0, SAI2_SCK_B, ETH_MII_CRS, FMC_SDCKE0, LCD_R0, EVENTOUT	-
-	-	G4	44	47	J4	K10	44	47	J4	PH3	I/O	FT	-	QUADSPI_BK2_IO1, SAI2_MCLK_B, ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT	-
-	-	H4	45	48	H4	N12	45	48	H4	PH4	I/O	FT	-	I2C2_SCL, LCD_G5, OTG_HS_ULPI_NXT, LCD_G4, EVENTOUT	-
-	-	J4	46	49	J3	N11	46	49	J3	PH5	I/O	FT	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	-
25	37	R2	47	50	R2	M10	47	50	R2	PA3	I/O	FT	-	TIM2_CH4, TIM5_CH4, TIM9_CH2, USART2_RX, LCD_B2, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	ADC1_IN3, ADC2_IN3, ADC3_IN3
26	38	-	-	51	K6	J9	-	51	K6	VSS	S	-	-	-	-
-	-	L4	48	-	L5	-[5]	48	-	L5	BYPASS_ REG	I	FT	-	-	-
27	39	K4	49	52	K5	K9	49	52	K5	VDD	S	-	-	-	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
47	70	R13	80	91	R13	L5	80	91	R13	PB11	I/O	FT	-	TIM2_CH4, I2C2_SDA, DFSDM1_CKIN7, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_RMII_TX_EN, DSI_TE, LCD_G5, EVENTOUT	-
48	71	M10	81	92	L11	P5	81	92	L11	VCAP_1	S	-	-	-	-
49	-	-	-	93	K9	N5	-	93	K9	VSS	S	-	-	-	-
50	72	N10	82	94	L10	P4	82	94	L10	VDD	S	-	-	-	-
-	-	-	-	95	M14	NC	-	95	M14	PJ5	I/O	FT	-	LCD_R6, EVENTOUT	-
-	-	M11	83	96	P13	NC	83	96	P13	PH6	I/O	FT	-	I2C2_SMBA, SPI5_SCK, TIM12_CH1, ETH_MII_RXD2, FMC_SDNE1, DCMI_D8, EVENTOUT	-
-	-	N12	84	97	N13	NC	84	97	N13	PH7	I/O	FT	-	I2C3_SCL, SPI5_MISO, ETH_MII_RXD3, FMC_SDCKE1, DCMI_D9, EVENTOUT	-
-	-	M12	85	98	P14	M5	-	98	P14	PH8	I/O	FT	-	I2C3_SDA, FMC_D16, DCMI_HSYNC, LCD_R2, EVENTOUT	-
-	-	M13	86	99	N14	K4	-	99	N14	PH9	I/O	FT	-	I2C3_SMBA, TIM12_CH2, FMC_D17, DCMI_D0, LCD_R3, EVENTOUT	-
-	-	L13	87	100	P15	L4	-	100	P15	PH10	I/O	FT	-	TIM5_CH1, I2C4_SMBA, FMC_D18, DCMI_D1, LCD_R4, EVENTOUT	-
-	-	L12	88	101	N15	M4	-	101	N15	PH11	I/O	FT	-	TIM5_CH2, I2C4_SCL, FMC_D19, DCMI_D2, LCD_R5, EVENTOUT	-

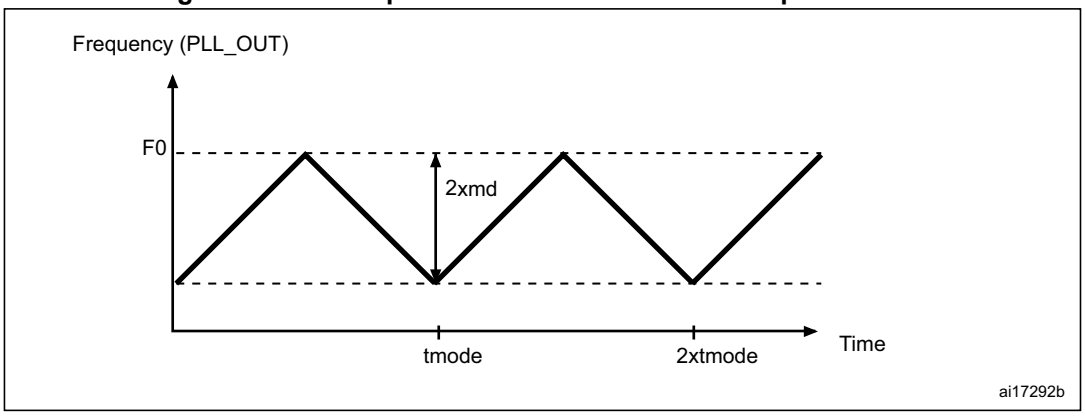
Table 12. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM1/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port B	PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	DFSDM1_CKIN5	USART1_RX	-	-	-	I2S4_SDA	FMC_NL	DCMI_VSYNC	-	EVENTOUT
	PB8	-	I2C4_SCL	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	DFSDM1_CKIN7	UART5_RX	-	CAN1_RX	SDMMC2_D4	ETH_MII_TXD3	SDMMC_D4	DCMI_D6	LCD_B6	EVENTOUT
	PB9	-	I2S4_SDA	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS/I2S2_WS	DFSDM1_DATIN7	UART5_TX	-	CAN1_TX	SDMMC2_D5	I2C4_SMBA	SDMMC_D5	DCMI_D7	LCD_B7	EVENTOUT
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK/I2S2_CK	DFSDM1_DATIN7	USART3_TX	-	- QUADSPI_BK1_NCS	OTG_HS_ULPI_D3	ETH_MII_RX_ER	-	-	LCD_G4	EVENTOUT
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	DFSDM1_CKIN7	USART3_RX	-	-	OTG_HS_ULPI_D4	ETH_MII_TX_EN/ETH_RMII_TX_EN	-	DSI_TE	LCD_G5	EVENTOUT
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS/I2S2_WS	DFSDM1_DATIN1	USART3_CK	UART5_RX	CAN2_RX	OTG_HS_ULPI_D5	ETH_MII_TXD0/ETH_RMII_TXD0	OTG_HS_ID	-	-	EVENTOUT
	PB13	-	TIM1_CH1N	-	-	-	SPI2_SCK/I2S2_CK	DFSDM1_CKIN1	USART3_CTS	UART5_TX	CAN2_TX	OTG_HS_ULPI_D6	ETH_MII_TXD1/ETH_RMII_TXD1	-	-	-	EVENTOUT
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	USART1_TX	SPI2_MISO	DFSDM1_DATIN2	USART3_RTS	UART4_RTS	TIM12_CH1	SDMMC2_D0	-	OTG_HS_DM	-	-	EVENTOUT
	PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	USART1_RX	SPI2_MOSI/I2S2_SD	DFSDM1_CKIN2	-	UART4_CTS	TIM12_CH2	SDMMC2_D1	-	OTG_HS_DP	-	-	EVENTOUT

Table 12. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM1/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	-	-	LPTIM1_IN2	-	-	-	-	-	QUADSPI_BK2_IO0	SAI2_SCK_B	ETH_MII_CRS	FMC_SDCKE0	-	LCD_R0	EVENTOUT
	PH3	-	-	-	-	-	-	-	-	-	QUADSPI_BK2_IO1	SAI2_MCK_B	ETH_MII_COL	FMC_SDNE0	-	LCD_R1	EVENTOUT
	PH4	-	-	-	-	I2C2_SCL	-	-	-	-	LCD_G5	OTG_HS_ULPI_NXT	-	-	-	LCD_G4	EVENTOUT
	PH5	-	-	-	-	I2C2_SDA	SPI5_NSS	-	-	-	-	-	-	FMC_SDNWE	-	-	EVENTOUT
	PH6	-	-	-	-	I2C2_SMBA	SPI5_SCK	-	-	-	TIM12_CH1	-	ETH_MII_RXD2	FMC_SDNE1	DCMI_D8	-	EVENTOUT
	PH7	-	-	-	-	I2C3_SCL	SPI5_MISO	-	-	-	-	-	ETH_MII_RXD3	FMC_SDCKE1	DCMI_D9	-	EVENTOUT
	PH8	-	-	-	-	I2C3_SDA	-	-	-	-	-	-	-	FMC_D16	DCMI_HSYNC	LCD_R2	EVENTOUT
	PH9	-	-	-	-	I2C3_SMBA	-	-	-	-	TIM12_CH2	-	-	FMC_D17	DCMI_D0	LCD_R3	EVENTOUT
	PH10	-	-	TIM5_CH1	-	I2C4_SMBA	-	-	-	-	-	-	-	FMC_D18	DCMI_D1	LCD_R4	EVENTOUT
	PH11	-	-	TIM5_CH2	-	I2C4_SCL	-	-	-	-	-	-	-	FMC_D19	DCMI_D2	LCD_R5	EVENTOUT
	PH12	-	-	TIM5_CH3	-	I2C4_SDA	-	-	-	-	-	-	-	FMC_D20	DCMI_D3	LCD_R6	EVENTOUT
	PH13	-	-	-	TIM8_CH1N	-	-	-	-	UART4_TX	CAN1_TX	-	-	FMC_D21	-	LCD_G2	EVENTOUT

Figure 35. PLL output clock waveforms in down spread mode



5.3.13 MIPI D-PHY characteristics

The parameters given in *Table 51* and *Table 52* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 51. MIPI D-PHY characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Hi-Speed Input/Output Characteristics						
U_{INST}	UI instantaneous	-	2	-	12.5	ns
V_{CMTX}	HS transmit common mode voltage	-	150	200	250	mV
$\|\Delta V_{CMTX}\|$	V_{CMTX} mismatch when output is Differential-1 or Differential-0	-	-	-	5	
$\|V_{OD}\|$	HS transmit differential voltage	-	140	200	270	
$\|\Delta V_{OD}\|$	V_{OD} mismatch when output is Differential-1 or Differential-0	-	-	-	14	
V_{OHHS}	HS output high voltage	-	-	-	360	
Z_{OS}	Single ended output impedance	-	40	50	62.5	Ω
ΔZ_{OS}	Single ended output impedance mismatch	-	-	-	10	%
t_{HSr} & t_{HSf}	20%-80% rise and fall time	-	100	-	0.35*UI	ps
LP Receiver Input Characteristics						
V_{IL}	Logic 0 input voltage (not in ULP State)	-	-	-	550	mV
$V_{IL-ULPS}$	Logic 0 input voltage in ULP State	-	-	-	300	
V_{IH}	Input high level voltage	-	880	-	-	
V_{hys}	Voltage hysteresis	-	25	-	-	
LP Emitter Output Characteristics						

I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 86* for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 86. I²S dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256x8K	256xFs(2)	MHz
f_{CK}	I2S clock frequency	Master data	-	64xFs	MHz
		Slave data	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	3	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	5	-	
$t_{h(WS)}$	WS hold time	Slave mode	2	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	2.5	-	
$t_{su(SD\_SR)}$		Slave receiver	2.5	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	3.5	-	
$t_{h(SD\_SR)}$		Slave receiver	2	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	12	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	3	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	5	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	0	-	

1. Guaranteed by characterization results.
2. The maximum value of 256xFs is 49.152 MHz (APB1 maximum frequency).

*Note: Refer to RM0410 reference manual I2S section for more details about the sampling frequency (F_S). f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). F_S maximum value is supported for each mode/condition.*

Table 89. SAI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge) 2.7≤VDD≤3.6V	-	12	ns
		Slave transmitter (after enable edge) 1.71≤VDD≤3.6V	-	20	
$t_{h(SD\_B\_MT)}$	Data output hold time	Slave transmitter (after enable edge)	5	-	
$t_{v(SD\_MT)\_A}$	Data output valid time	Master transmitter (after enable edge) 2.7≤VDD≤3.6V	-	15	
		Master transmitter (after enable edge) 1.71≤VDD≤3.6V	-	20	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	5	-	

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.
3. With F_S=192kHz.

Figure 53. SAI master timing waveforms

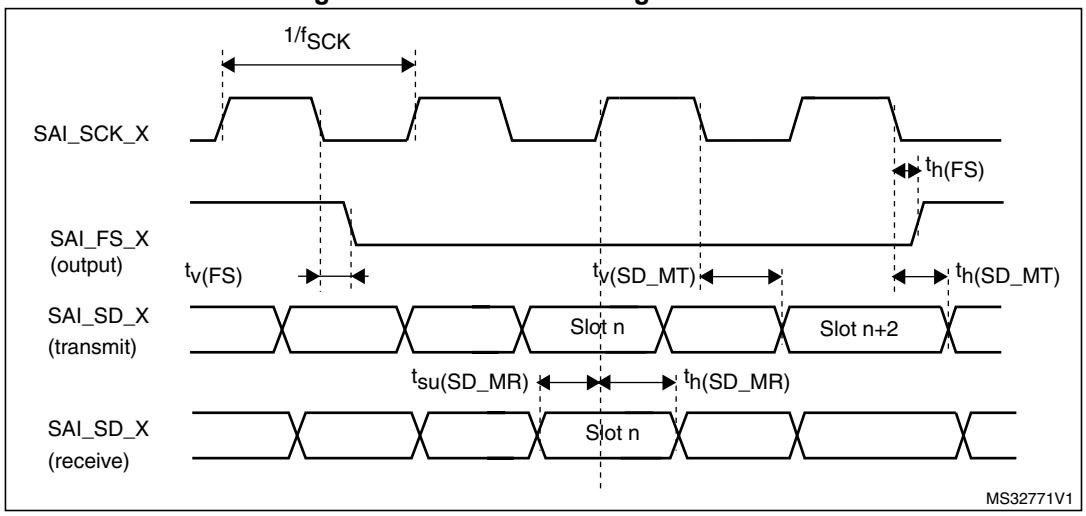


Table 100. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$2T_{HCLK} - 1$	$2 T_{HCLK} +1$	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	0.5	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{HCLK} - 1$	$2T_{HCLK} + 1$	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL\_NOE)}$	FMC_BL hold time after FMC_NOE high	0	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	$T_{HCLK} - 1$	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	$T_{HCLK} - 1$	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{HCLK} + 1$	

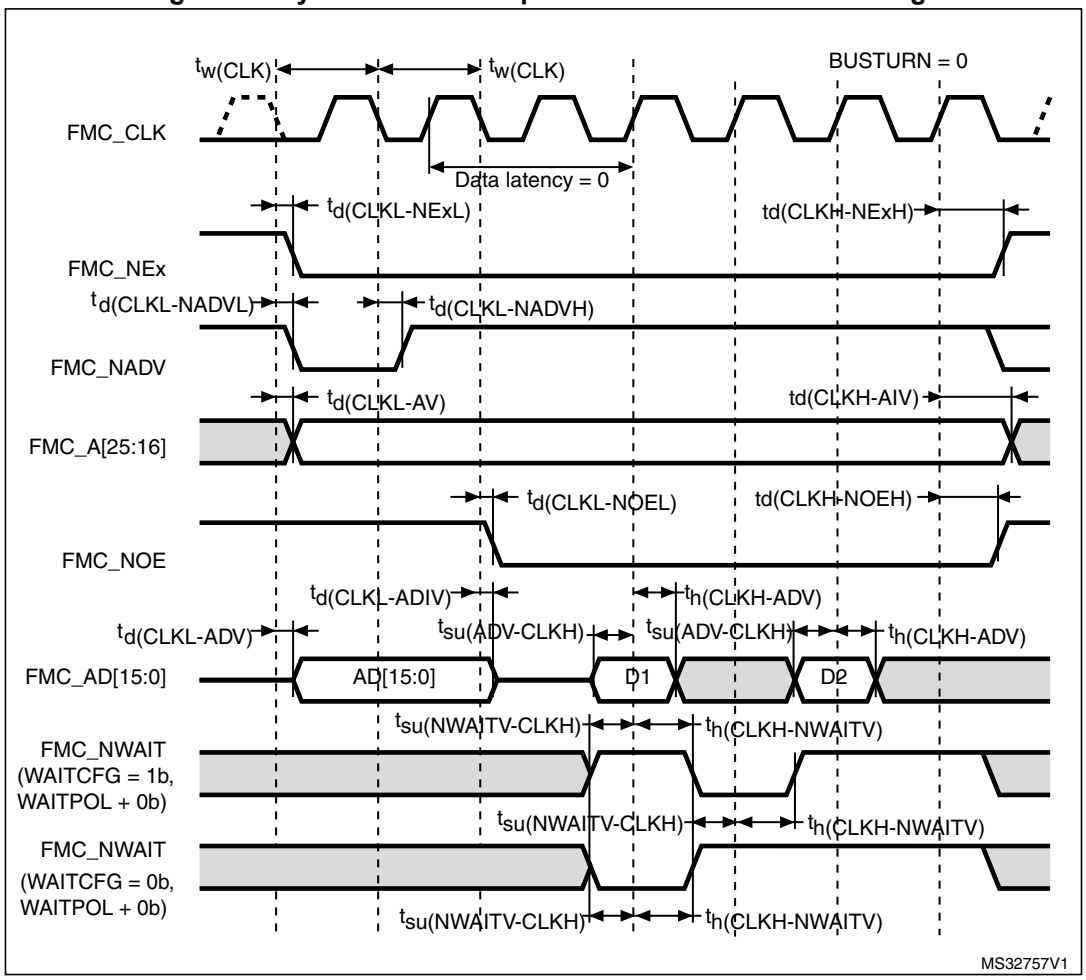
1. C_L = 30 pF.
2. Guaranteed by characterization results.

Table 101. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$7T_{HCLK} +1$	$7T_{HCLK} +1$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK} -1$	$5T_{HCLK} +1$	
$t_{w(NWAIT)}$	FMC_NWAIT low time	$T_{HCLK} -0.5$		
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK} +1.5$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}+1$	-	

1. Guaranteed by characterization results.

Figure 65. Synchronous multiplexed NOR/PSRAM read timings



1. Guaranteed by characterization results.

Figure 68. Synchronous non-multiplexed PSRAM write timings

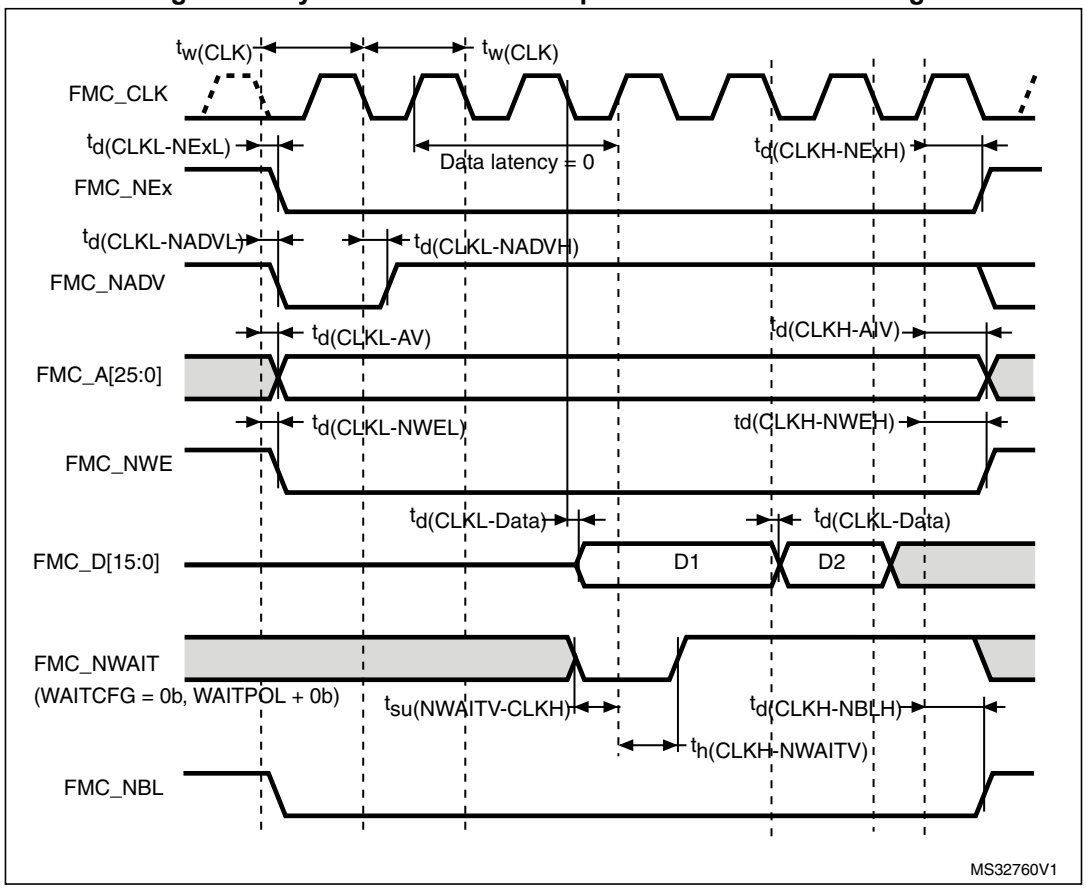


Figure 75. Quad-SPI timing diagram - SDR mode

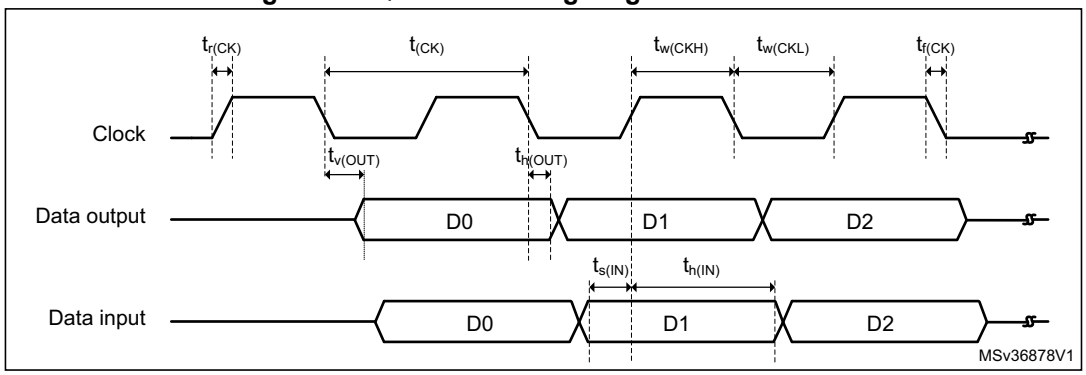
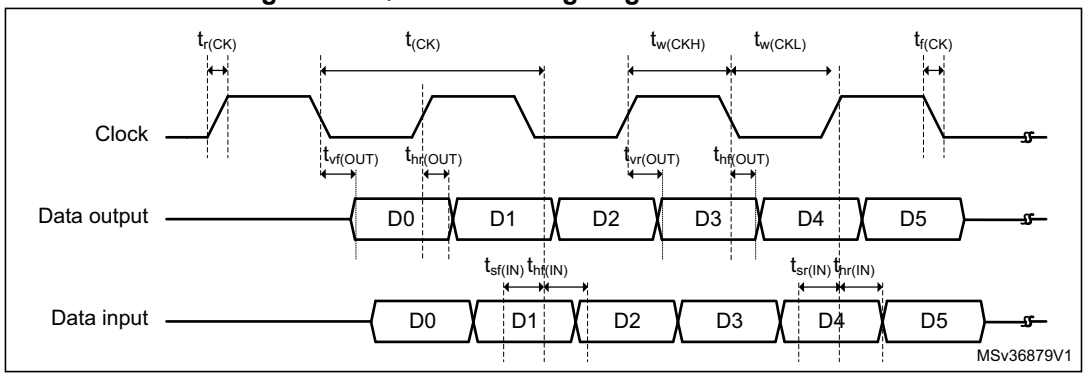


Figure 76. Quad-SPI timing diagram - DDR mode



5.3.32 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 120* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 17*, with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits

Table 120. DCMI characteristics(1)

Symbol	Parameter	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	0.4	
DCMI_PIXCLK	Pixel clock input	-	54	MHz
D_{Pixel}	Pixel clock input duty cycle	30	70	%
$t_{su(DATA)}$	Data input setup time	2	-	ns
$t_{h(DATA)}$	Data input hold time	0.5	-	
$t_{su(HSYNC)}$ $t_{su(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input setup time	2.5	-	
$t_{h(HSYNC)}$ $t_{h(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input hold time	3	-	

1. Guaranteed by characterization results.

5.3.34 Digital filter for Sigma-Delta Modulators (DFSDM) characteristics

Unless otherwise specified, the parameters given in *Table 122* for DFSDM are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DD} supply voltage summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30pF
- Measurement points are done at CMOS levels: 0.5 x VDD

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (DFSDM1_CKINx, DFSDM1_DATINx, DFSDM1_CKOUT for DFSDM1).

Table 122. DFSDM measured timing 1.71-3.6V

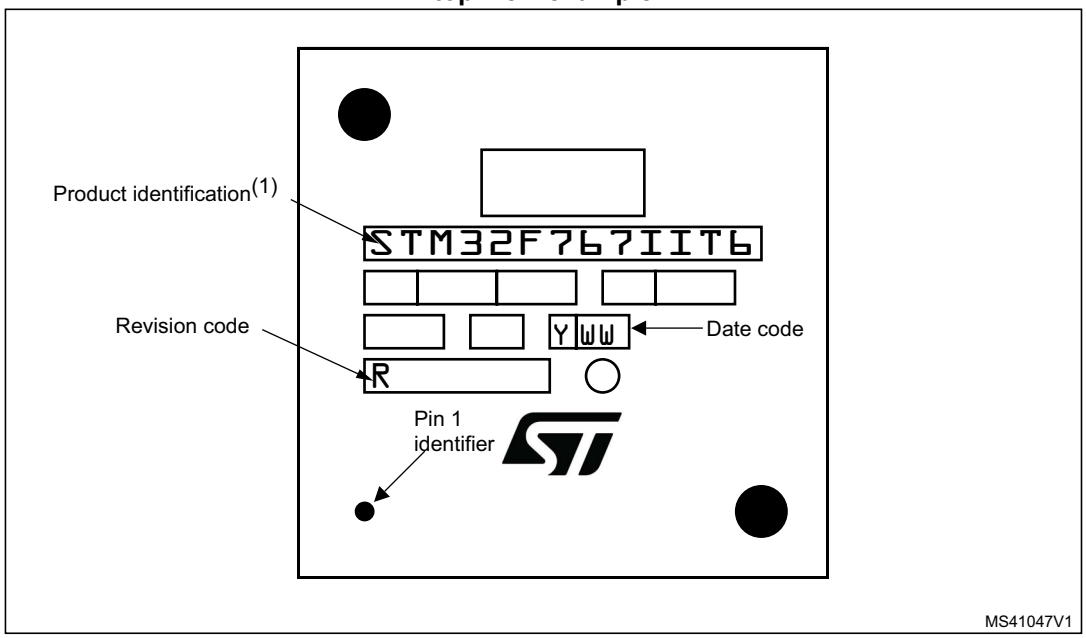
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	1.71 < V_{DD} < 3.6 V	-	-	f_{SYSCLK}	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < V_{DD} < 3.6 V	-	-	20 ($f_{DFSDMCLK}$/4)	
		SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 2.7 < V_{DD} < 3.6 V	-	-	20 ($f_{DFSDMCLK}$/4)	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), 1.71 < V_{DD} < 3.6 V	-	-	20 ($f_{DFSDMCLK}$/4)	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), 2.7 < V_{DD} < 3.6 V	-	-	20 ($f_{DFSDMCLK}$/4)	
f_{CKOUT}	Output clock frequency	1.71 < V_{DD} < 3.6 V	-	-	20	
$DuCy_{CKOUT}$	Output clock frequency duty cycle	1.71 < V_{DD} < 3.6 V	45	50	55	%

LQFP176 device marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 91. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6.8 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max x Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 135. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP100 - 14 × 14 mm / 0.5 mm pitch	43	°C/W
	Thermal resistance junction-ambient WLCSP180 - 0.4 mm pitch	30	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	40	
	Thermal resistance junction-ambient LQFP176 - 24 × 24 mm / 0.5 mm pitch	38	
	Thermal resistance junction-ambient LQFP208 - 28 × 28 mm / 0.5 mm pitch	19	
	Thermal resistance junction-ambient UFBGA176 - 10× 10 mm / 0.5 mm pitch	39	
	Thermal resistance junction-ambient TFBGA216 - 13 × 13 mm / 0.8 mm pitch	29	

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

7 Ordering information

Table 136. Ordering information scheme

Example: STM32 F 76x V G T 6 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

765= STM32F765xx, USB OTG FS/HS, camera interface, Ethernet
767= STM32F767xx, USB OTG FS/HS, camera interface, Ethernet, LCD-TFT
768 = STM32F768Ax, USB OTG FS/HS, camera interface, DSI host, WLCSP with internal regulator OFF
769= STM32F769xx, USB OTG FS/HS, camera interface, Ethernet, DSI host

Pin count

V = 100 pins
Z = 144 pins
I = 176 pins
A = 180 pins
B = 208 pins
N = 216 pins

Flash memory size

G = 1024 Kbytes of Flash memory
I = 2048 Kbytes of Flash memory

Package

T = LQFP
K = UFBGA
H = TFBGA
Y = WLCSP

Temperature range

6 = Industrial temperature range, –40 to 85 °C.
7 = Industrial temperature range, –40 to 105 °C.

Options

xxx = programmed parts
TR = tape and reel

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.