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### What is "[Embedded - Microcontrollers](#)"?

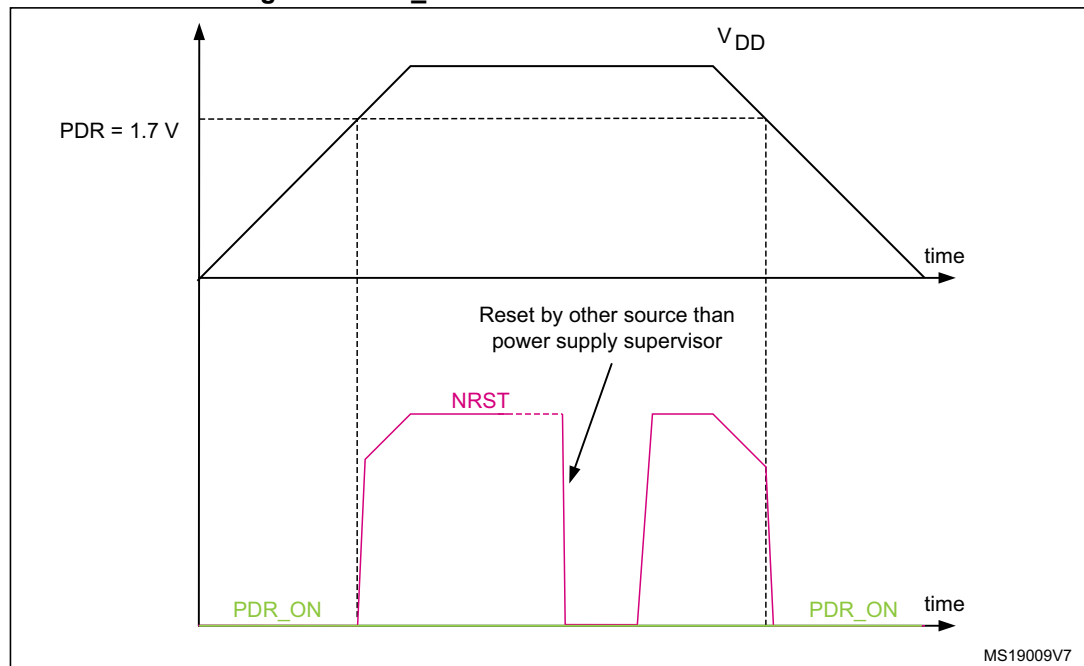
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex® -M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I <sup>2</sup> C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, LCD, POR, PWM, WDT
Number of I/O	140
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f767iit6">https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f767iit6</a>

Figure 7. PDR\_ON control with internal reset OFF



## 2.19 Voltage regulator

The regulator has four operating modes:

- Regulator ON
  - Main regulator mode (MR)
  - Low power regulator (LPR)
  - Power-down
- Regulator OFF

### 2.19.1 Regulator ON

On packages embedding the BYPASS\_REG pin, the regulator is enabled by holding BYPASS\_REG low. On all other packages, the regulator is always enabled.

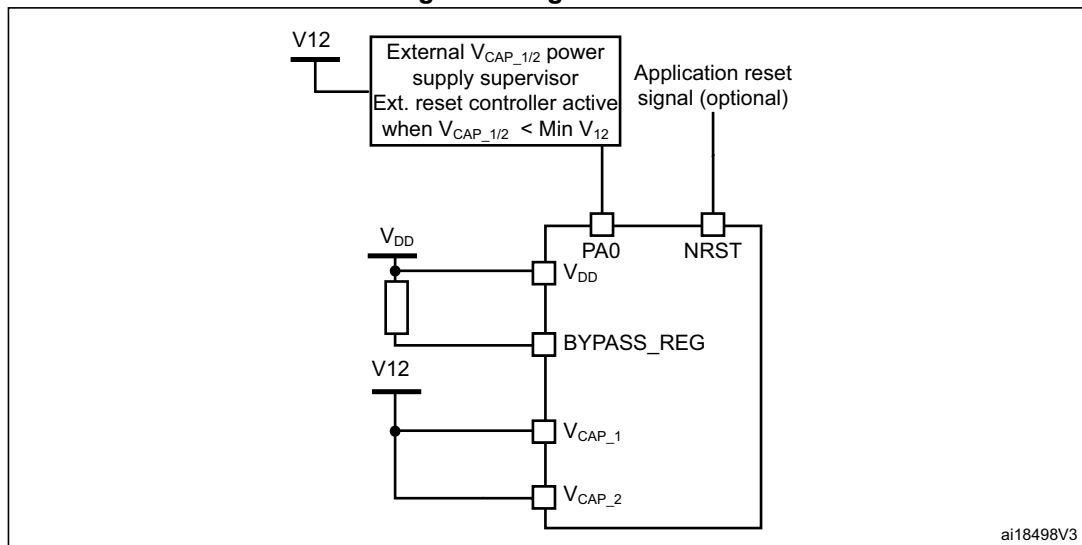
There are three power modes configured by software when the regulator is ON:

- MR mode used in Run/sleep modes or in Stop modes
  - In Run/Sleep modes
 

The MR mode is used either in the normal mode (default mode) or the over-drive mode (enabled by software). Different voltages scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption. The over-drive mode allows operating at a higher frequency than the normal mode for a given voltage scaling.
  - In Stop modes
 

The MR can be configured in two ways during stop mode:  
 MR operates in normal mode (default mode of MR in stop mode)  
 MR operates in under-drive mode (reduced leakage mode).

Figure 8. Regulator OFF



The following conditions must be respected:

- $V_{DD}$  should always be higher than  $V_{CAP\_1}$  and  $V_{CAP\_2}$  to avoid current injection between power domains.
- If the time for  $V_{CAP\_1}$  and  $V_{CAP\_2}$  to reach  $V_{12}$  minimum value is faster than the time for  $V_{DD}$  to reach 1.7 V, then PA0 should be kept low to cover both conditions: until  $V_{CAP\_1}$  and  $V_{CAP\_2}$  reach  $V_{12}$  minimum value and until  $V_{DD}$  reaches 1.7 V (see [Figure 9](#)).
- Otherwise, if the time for  $V_{CAP\_1}$  and  $V_{CAP\_2}$  to reach  $V_{12}$  minimum value is slower than the time for  $V_{DD}$  to reach 1.7 V, then PA0 could be asserted low externally (see [Figure 10](#)).
- If  $V_{CAP\_1}$  and  $V_{CAP\_2}$  go below  $V_{12}$  minimum value and  $V_{DD}$  is higher than 1.7 V, then a reset must be asserted on PA0 pin.

**Note:** The minimum value of  $V_{12}$  depends on the maximum frequency targeted in the application.

### 2.19.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal reset ON/OFF availability

Package	Regulator ON	Regulator OFF	Internal reset ON	Internal reset OFF
LQFP100	Yes	No	Yes	No
LQFP144, LQFP208			Yes PDR_ON set to V <sub>DD</sub>	Yes PDR_ON set to V <sub>SS</sub>
LQFP176, UFBGA176, TFBGA216	Yes BYPASS_REG set to V <sub>SS</sub>	Yes BYPASS_REG set to V <sub>DD</sub>		
WLCSP180	Yes <sup>(1)</sup>			

1. Available only on dedicated part number. Refer to [Section 7: Ordering information](#).

## 2.20 Real-time clock (RTC), backup SRAM and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to V<sub>BAT</sub> mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V<sub>DD</sub> supply when present or from the V<sub>BAT</sub> pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when V<sub>DD</sub> power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

## 2.38 Management Data Input/Output (MDIO) slaves

The devices embed a MDIO slave interface it includes the following features:

- 32 MDIO Registers addresses, each of which is managed using separate input and output data registers:
  - 32 x 16-bit firmware read/write, MDIO read-only output data registers
  - 32 x 16-bit firmware read-only, MDIO write-only input data registers
- Configurable slave (port) address
- Independently maskable interrupts/events:
  - MDIO Register write
  - MDIO Register read
  - MDIO protocol error
- Able to operate in and wake up from STOP mode

## 2.39 Random number generator (RNG)

All the devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

## 2.40 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

A fast I/O handling allows a maximum I/O toggling up to 108 MHz.

## 2.41 Analog-to-digital converters (ADCs)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM5, or TIM8 timer.

- 16-bit RGB, configurations 1, 2, and 3
  - 18-bit RGB, configurations 1 and 2
  - 24-bit RGB
- Programmable polarity of all LTDC interface signals
- Extended resolutions beyond the DPI standard
- Maximum resolution of 800x480 pixels:
- Maximum resolution is limited by available DSI physical link bandwidth:
  - Number of lanes: 2
  - Maximum speed per lane: 500 Mbps1Gbps

### Adapted interface features

Support for sending large amounts of data through the memory\_write\_start(WMS) and memory\_write\_continue(WMC) DCS commands

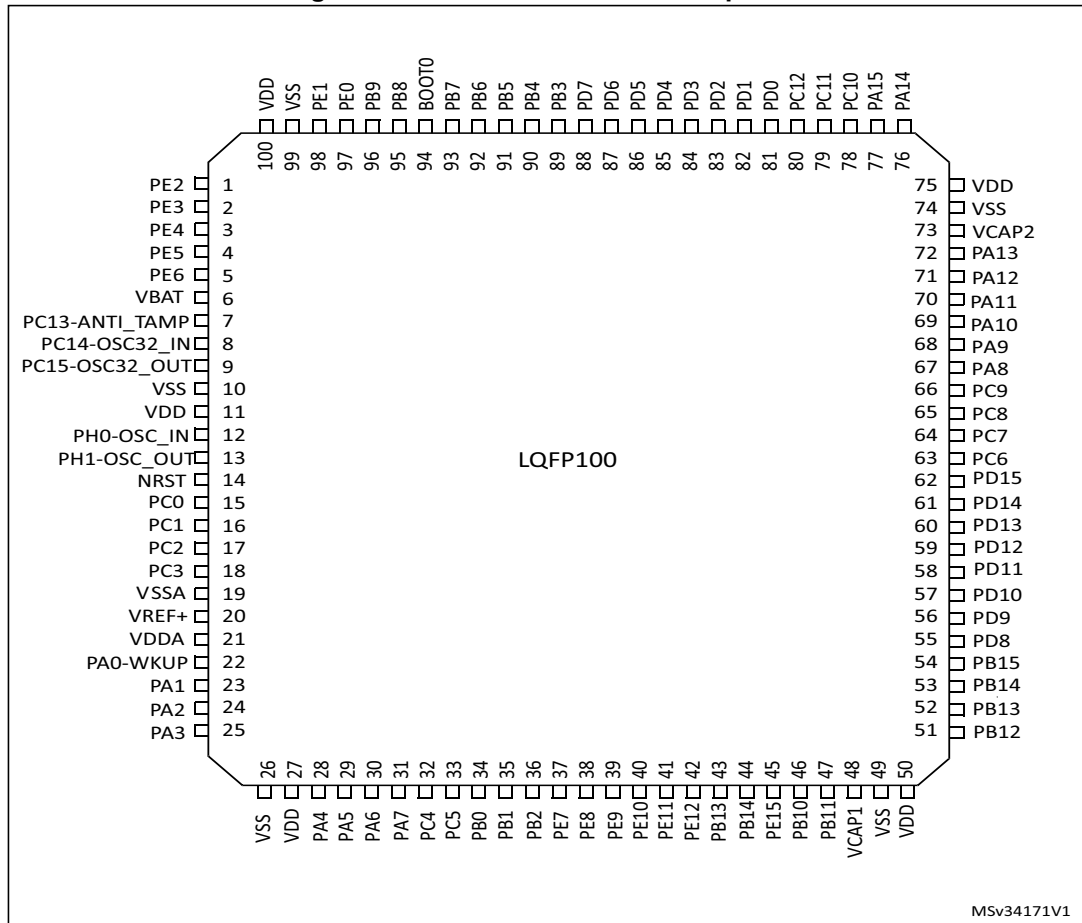
- LTDC interface color coding mappings into 24-bit interface:
  - 16-bit RGB, configurations 1, 2, and 3
  - 18-bit RGB, configurations 1 and 2
  - 24-bit RGB

### Video mode pattern generator:

- Vertical and horizontal color bar generation without LTDC stimuli
- BER pattern without LTDC stimuli

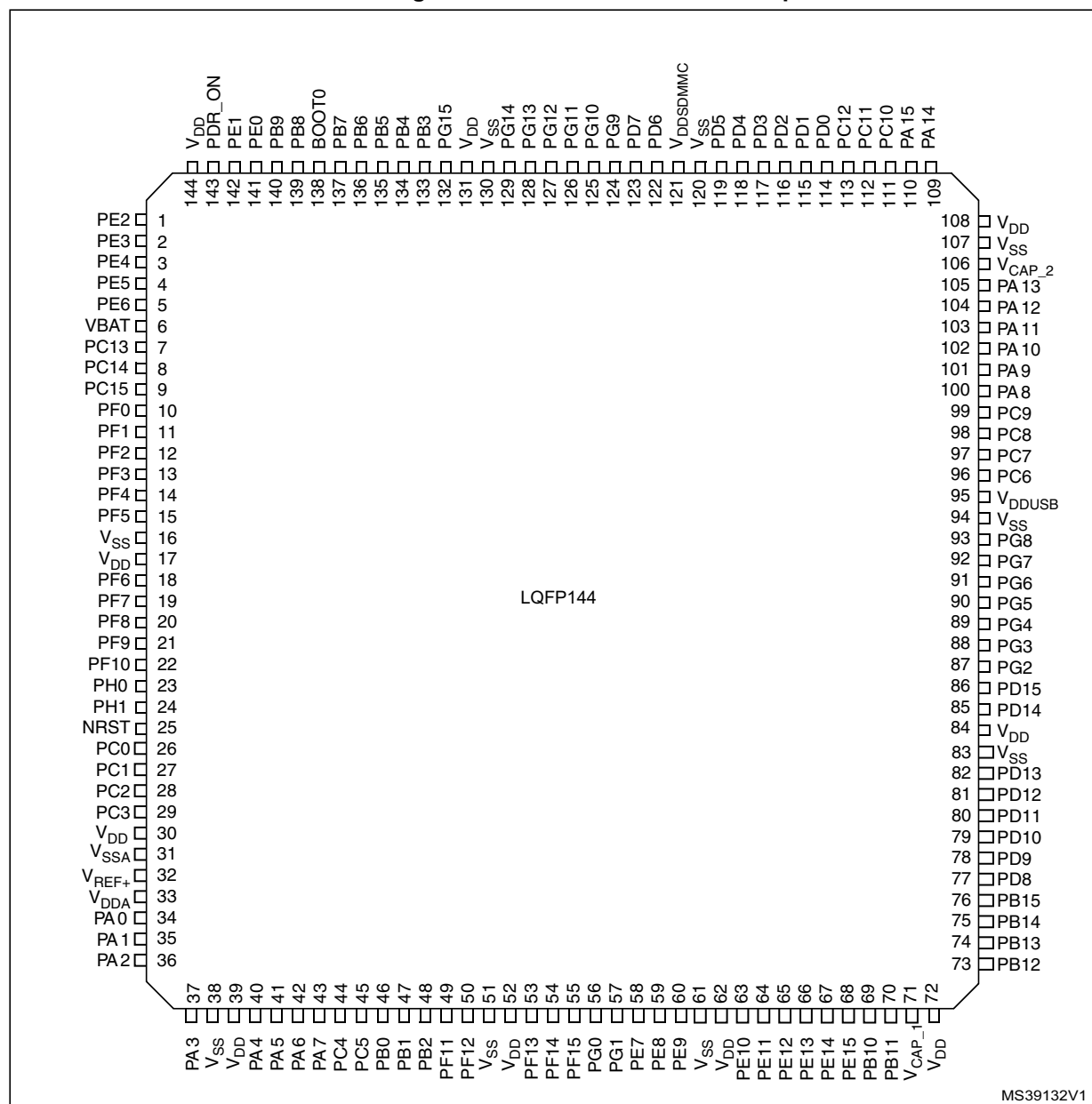
### 3 Pinouts and pin description

Figure 11. STM32F76xxx LQFP100 pinout



1. The above figure shows the package top view.

Figure 12. STM32F76xxx LQFP144 pinout



1. The above figure shows the package top view.



Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180 <sup>(1)</sup>	LQFP176	LQFP208	TFBGA216						
24	36	P2	42	45	P2	J10	42	45	P2	PA2	I/O	FT	-	TIM2_CH3, TIM5_CH3, TIM9_CH1, USART2_TX, SAI2_SCK_B, ETH_MDIO, MDIOS_MDIO, LCD_R1, EVENTOUT	ADC1_IN2, ADC2_IN2, ADC3_IN2, WKUP2
-	-	F4	43	46	K4	L10	43	46	K4	PH2	I/O	FT	-	LPTIM1_IN2, QUADSPI_BK2_IO0, SAI2_SCK_B, ETH_MII_CRS, FMC_SDCKE0, LCD_R0, EVENTOUT	-
-	-	G4	44	47	J4	K10	44	47	J4	PH3	I/O	FT	-	QUADSPI_BK2_IO1, SAI2_MCLK_B, ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT	-
-	-	H4	45	48	H4	N12	45	48	H4	PH4	I/O	FT	-	I2C2_SCL, LCD_G5, OTG_HS_ULPI_NXT, LCD_G4, EVENTOUT	-
-	-	J4	46	49	J3	N11	46	49	J3	PH5	I/O	FT	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	-
25	37	R2	47	50	R2	M10	47	50	R2	PA3	I/O	FT	-	TIM2_CH4, TIM5_CH4, TIM9_CH2, USART2_RX, LCD_B2, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	ADC1_IN3, ADC2_IN3, ADC3_IN3
26	38	-	-	51	K6	J9	-	51	K6	VSS	S	-	-	-	-
-	-	L4	48	-	L5	-( <sup>5</sup> )	48	-	L5	BYPASS_REG	I	FT	-	-	-
27	39	K4	49	52	K5	K9	49	52	K5	VDD	S	-	-	-	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180 <sup>(1)</sup>	LQFP176	LQFP208	TFBGA216						
91	135	A6	163	194	A8	A9	163	194	A8	PB5	I/O	FT	-	UART5_RX, TIM3_CH2, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, SPI6_MOSI, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, FMC_SDCKE1, DCMI_D10, LCD_G7, EVENTOUT	-
92	136	B6	164	195	B6	B9	164	195	B6	PB6	I/O	FT	-	UART5_TX, TIM4_CH1, HDMI_CEC, I2C1_SCL, DFSDM1_DATIN5, USART1_TX, CAN2_TX, QUADSPI_BK1_NCS, I2C4_SCL, FMC_SDNE1, DCMI_D5, EVENTOUT	-
93	137	B5	165	196	B5	C8	165	196	B5	PB7	I/O	FT	-	TIM4_CH2, I2C1_SDA, DFSDM1_CKIN5, USART1_RX, I2C4_SDA, FMC_NL, DCMI_VSYNC, EVENTOUT	-
94	138	D6	166	197	E6	A10	166	197	E6	BOOT0	I	B	-	-	VPP
95	139	A5	167	198	A7	E9	167	198	A7	PB8	I/O	FT	-	I2C4_SCL, TIM4_CH3, TIM10_CH1, I2C1_SCL, DFSDM1_CKIN7, UART5_RX, CAN1_RX, SDMMC2_D4, ETH_MII_TXD3, SDMMC1_D4, DCMI_D6, LCD_B6, EVENTOUT	-

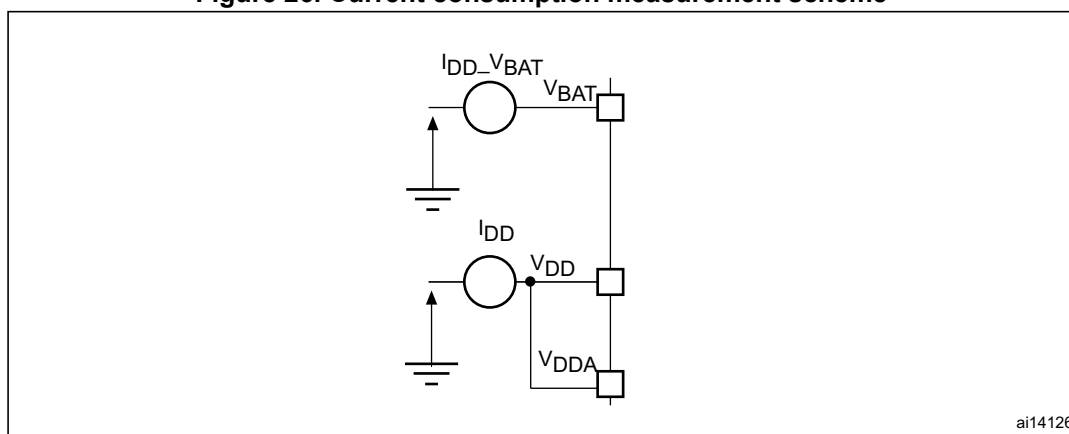
Table 11. FMC pin definition

Pin name	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PF0	A0	-	-	A0
PF1	A1	-	-	A1
PF2	A2	-	-	A2
PF3	A3	-	-	A3
PF4	A4	-	-	A4
PF5	A5	-	-	A5
PF12	A6	-	-	A6
PF13	A7	-	-	A7
PF14	A8	-	-	A8
PF15	A9	-	-	A9
PG0	A10	-	-	A10
PG1	A11	-	-	A11
PG2	A12	-	-	A12
PG3	A13	-	-	-
PG4	A14	-	-	BA0
PG5	A15	-	-	BA1
PD11	A16	A16	CLE	-
PD12	A17	A17	ALE	-
PD13	A18	A18	-	-
PE3	A19	A19	-	-
PE4	A20	A20	-	-
PE5	A21	A21	-	-
PE6	A22	A22	-	-
PE2	A23	A23	-	-
PG13	A24	A24	-	-
PG14	A25	A25	-	-
PD14	D0	DA0	D0	D0
PD15	D1	DA1	D1	D1
PD0	D2	DA2	D2	D2
PD1	D3	DA3	D3	D3
PE7	D4	DA4	D4	D4
PE8	D5	DA5	D5	D5
PE9	D6	DA6	D6	D6
PE10	D7	DA7	D7	D7

**Caution:** Each power supply pair ( $V_{DD}/V_{SS}$ ,  $V_{DDA}/V_{SSA}$  ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

### 5.1.7 Current consumption measurement

Figure 26. Current consumption measurement scheme



## 5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 14: Voltage characteristics](#), [Table 15: Current characteristics](#), and [Table 16: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. The device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard. Extended mission profiles are available on demand.

Table 14. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD}-V_{SS}$	External main supply voltage (including $V_{DDA}$ , $V_{DD}$ , $V_{BAT}$ , $V_{DDUSB}$ , $V_{DDDSI}$ <sup>(1)</sup> and $V_{DDSDMMC}$ <sup>(2)</sup> )	- 0.3	4.0	V
$V_{IN}$	Input voltage on FT pins <sup>(3)</sup>	$V_{SS} - 0.3$	$V_{DD} + 4.0$	
	Input voltage on TTa pins	$V_{SS} - 0.3$	4.0	
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	
	Input voltage on BOOT pin	$V_{SS}$	9.0	mV
$ \Delta V_{DDx} $	Variations between different $V_{DD}$ power pins	-	50	
$ V_{SSx} - V_{SS} $	Variations between all the different ground pins <sup>(4)</sup>	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see <a href="#">Section 5.3.18: Absolute maximum ratings (electrical sensitivity)</a>		-

## 5.3 Operating conditions

### 5.3.1 General operating conditions

Table 17. General operating conditions

Symbol	Parameter	Conditions <sup>(1)</sup>	Min	Typ	Max	Unit
$f_{HCLK}$	Internal AHB clock frequency	Power Scale 3 (VOS[1:0] bits in PWR_CR register = 0x01), Regulator ON, over-drive OFF	0	-	144	MHz
		Power Scale 2 (VOS[1:0] bits in PWR_CR register = 0x10), Regulator ON	0	-	168	
				-	180	
		Power Scale 1 (VOS[1:0] bits in PWR_CR register = 0x11), Regulator ON	0	-	180	
				-	216 <sup>(2)</sup>	
$f_{PCLK1}$	Internal APB1 clock frequency	Over-drive OFF	0	-	45	V
		Over-drive ON	0	-	54	
$f_{PCLK2}$	Internal APB2 clock frequency	Over-drive OFF	0	-	90	
		Over-drive ON	0	-	108	
$V_{DD}$	Standard operating voltage	-	1.7 <sup>(3)</sup>	-	3.6	
$V_{DDA}^{(4)(5)}$	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as $V_{DD}^{(6)}$	1.7 <sup>(3)</sup>	-	2.4	
	Analog operating voltage (ADC limited to 2.4 M samples)		2.4	-	3.6	
$V_{DDUSB}$	USB supply voltage (supply voltage for PA11, PA12, PB14 and PB15 pins)	USB not used	1.7	3.3	3.6	
		USB used	3.0	-	3.6	
$V_{BAT}$	Backup operating voltage	-	1.65	-	3.6	
$V_{DDSDMMC}$	SDMMC2 supply voltage (supply voltage for PG[12:9] and PD6 pins)	It can be different from $V_{DD}$	1.7	-	3.6	
$V_{DDDSI}$	DSI system operating	-	1.7	-	3.6	

**Table 28. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (Dual bank mode), regulator ON**

Symbol	Parameter	Conditions	f <sub>HCLK</sub> (MHz)	Typ	Max <sup>(1)</sup>			Unit
					TA= 25 °C	TA=85 °C	TA=105 °C	
I <sub>DD</sub>	Supply current in RUN mode	All peripherals enabled <sup>(2)(3)</sup>	216	176	194	240	-	mA
			200	164	181	227	255	
			180	149	163	198	220	
			168	133	145	178	198	
			144	106	116	143	161	
			60	54	60	87	105	
			25	27	31	58	76	
		All peripherals disabled <sup>(3)</sup>	216	77	88	135	-	
			200	72	82	129	157	
			180	67	75	110	131	
			168	60	67	99	120	
			144	50	56	83	101	
			60	29	34	60	78	
			25	15	19	45	63	

1. Guaranteed by characterization results, unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC\_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

**Caution:** Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see [Table 39: Peripheral current consumption](#)), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

$I_{SW}$  is the current sunk by a switching I/O to charge/discharge the capacitive load

$V_{DD}$  is the MCU supply voltage

$f_{SW}$  is the I/O switching frequency

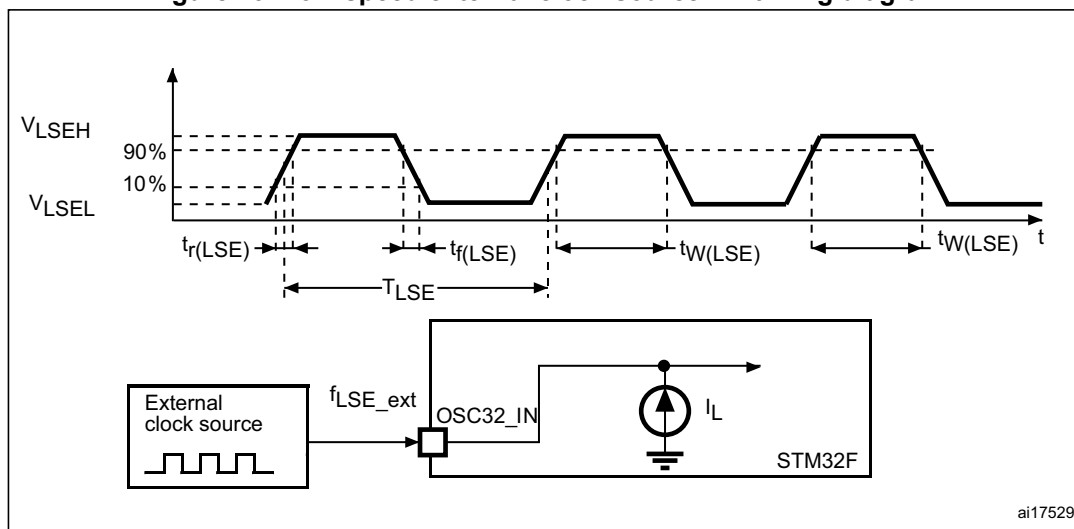
$C$  is the total capacitance seen by the I/O pin:  $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

**Table 38. Switching output I/O current consumption<sup>(1)</sup>**

Symbol	Parameter	Conditions	I/O toggling frequency (f <sub>sw</sub> ) MHz	Typ V <sub>DD</sub> = 3.3 V	Typ V <sub>DD</sub> = 1.8 V	Unit
I <sub>DDIO</sub>	I/O switching Current	C <sub>EXT</sub> = 0 pF C = C <sub>INT</sub> + C <sub>S</sub> + C <sub>EXT</sub>	2	0.1	0.1	mA
			8	0.4	0.2	
			25	1.1	0.7	
			50	2.4	1.3	
			60	3.1	1.6	
			84	4.3	2.4	
			90	4.9	2.6	
			100	5.4	2.8	
		C <sub>EXT</sub> = 10 pF C = C <sub>INT</sub> + C <sub>S</sub> + C <sub>EXT</sub>	2	0.2	0.1	
			8	0.6	0.3	
			25	1.8	1.1	
			50	3.1	2.3	
			60	4.6	3.4	
			84	9.7	3.6	
			90	10.12	5.2	
			100	14.92	5.4	

Figure 29. Low-speed external clock source AC timing diagram



ai17529

### High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 43](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 43. HSE 4-26 MHz oscillator characteristics<sup>(1)</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{OSC\_IN}$	Oscillator frequency		4	-	26	MHz
$R_F$	Feedback resistor		-	200	-	k $\Omega$
$I_{DD}$	HSE current consumption	$V_{DD}=3.3\text{ V}$ , ESR= 30 $\Omega$ , $C_L=5\text{ pF}@25\text{ MHz}$	-	450	-	$\mu\text{A}$
		$V_{DD}=3.3\text{ V}$ , ESR= 30 $\Omega$ , $C_L=10\text{ pF}@25\text{ MHz}$	-	530	-	
$ACC_{HSE}^{(2)}$	HSE accuracy		- 500	-	500	ppm
$G_{m\_crit\_max}$	Maximum critical crystal $g_m$	Startup	-	-	1	mA/V
$t_{SU(HSE)}^{(3)}$	Startup time	$V_{DD}$ is stabilized	-	2	-	ms

1. Guaranteed by design.

2. This parameter depends on the crystal used in the application. The minimum and maximum values must be respected to comply with USB standard specifications.

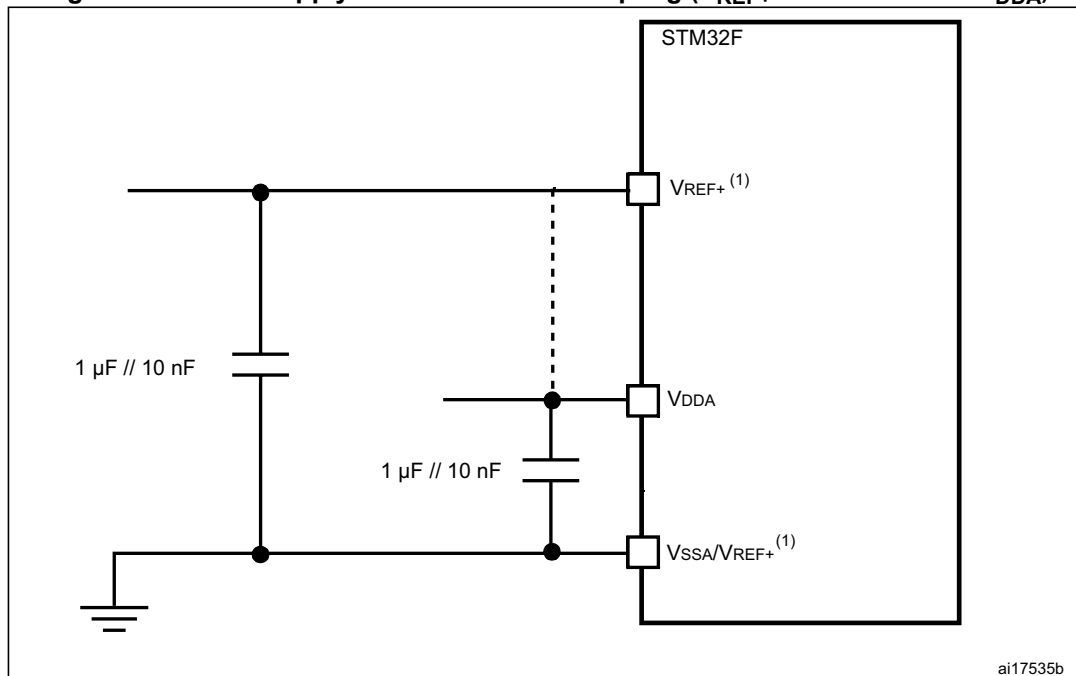
3.  $t_{SU(HSE)}$  is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is guaranteed by characterization results. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.



### General PCB design guidelines

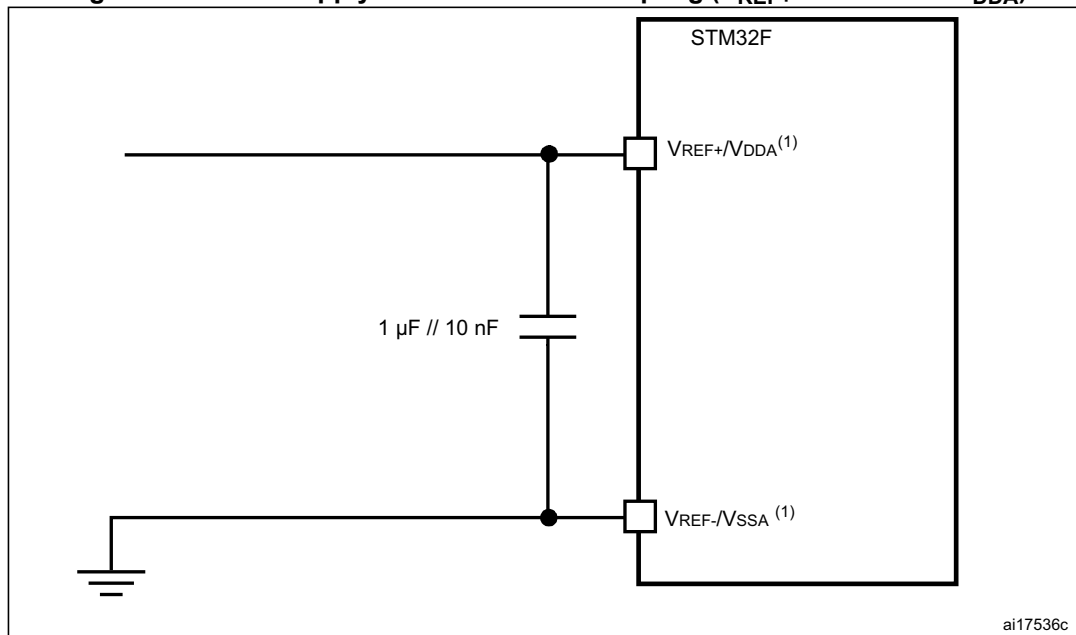
Power supply decoupling should be performed as shown in [Figure 43](#) or [Figure 44](#), depending on whether  $V_{REF+}$  is connected to  $V_{DDA}$  or not. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

**Figure 43. Power supply and reference decoupling ( $V_{REF+}$  not connected to  $V_{DDA}$ )**

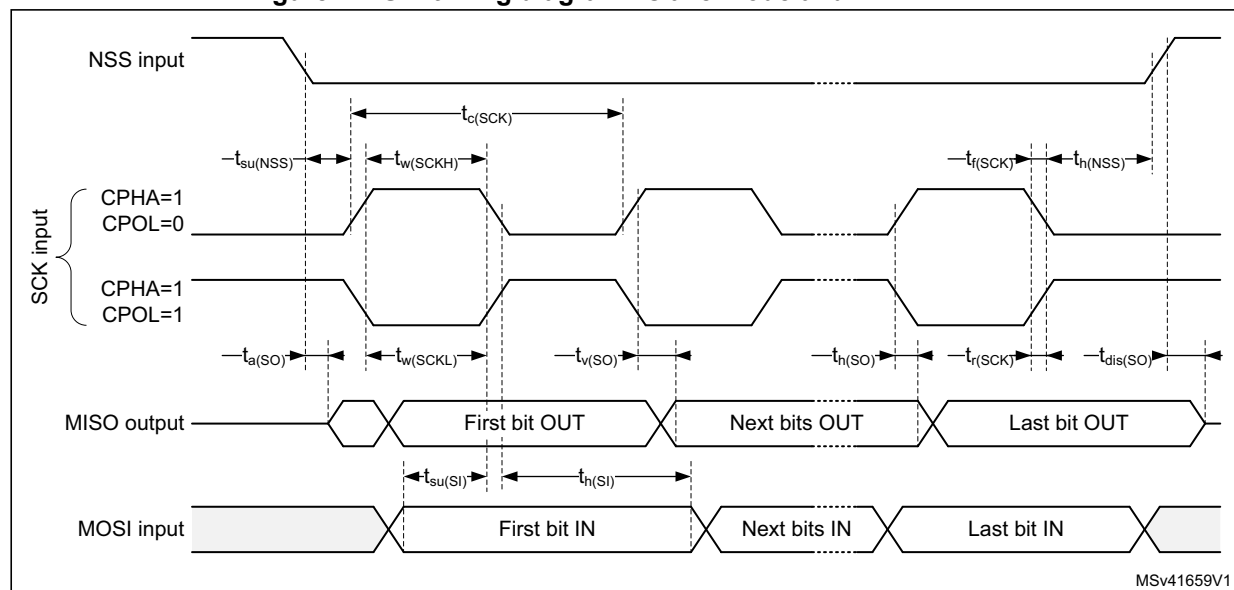


1.  $V_{REF+}$  input is available on all package whereas the  $V_{REF-}$  is available only on UFBGA176 and TFBGA216. When  $V_{REF-}$  is not available, it is internally connected to  $V_{DDA}$  and  $V_{SSA}$ .

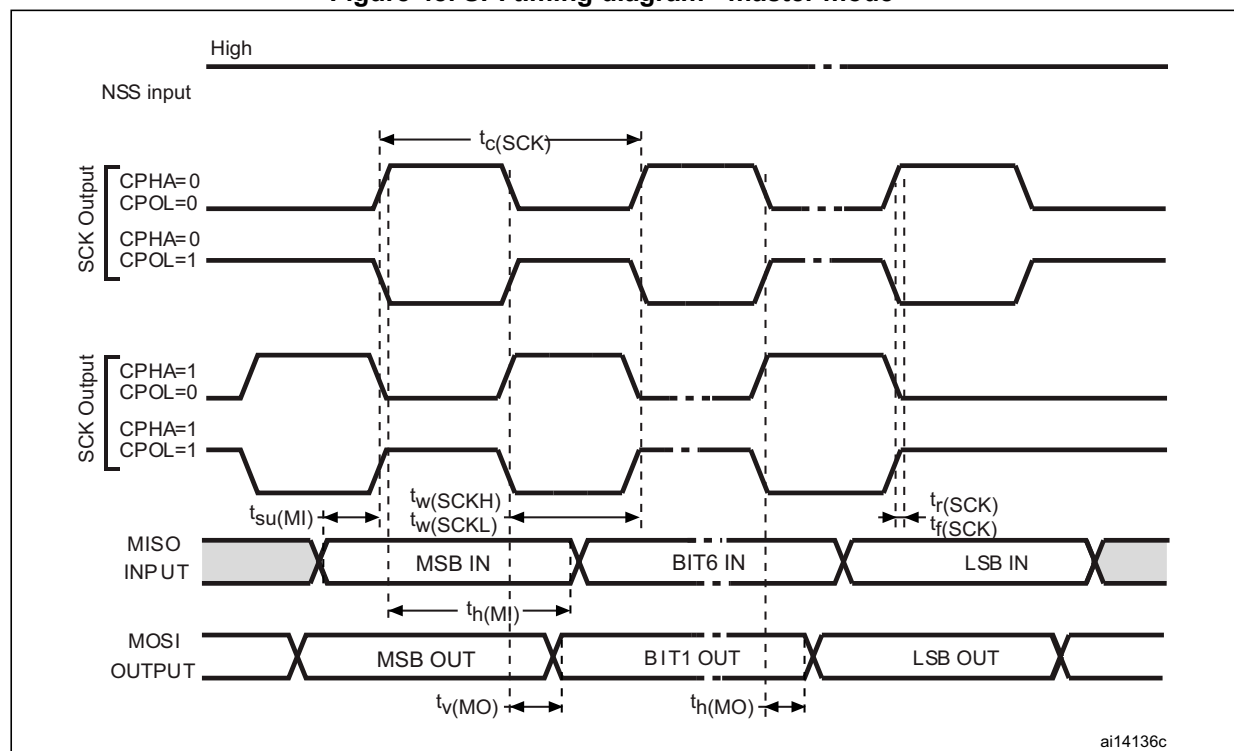
**Figure 44. Power supply and reference decoupling ( $V_{REF+}$  connected to  $V_{DDA}$ )**



1.  $V_{REF+}$  input is available on all package whereas the  $V_{REF-}$  is available only on UFBGA176 and TFBGA216. When  $V_{REF-}$  is not available, it is internally connected to  $V_{DDA}$  and  $V_{SSA}$ .

Figure 47. SPI timing diagram - slave mode and CPHA = 1<sup>(1)</sup>

1. Measurement points are done at  $0.5V_{DD}$  and with external  $C_L = 30$  pF.

Figure 48. SPI timing diagram - master mode<sup>(1)</sup>

1. Measurement points are done at  $0.5V_{DD}$  and with external  $C_L = 30$  pF.

Figure 78. LCD-TFT horizontal timing diagram

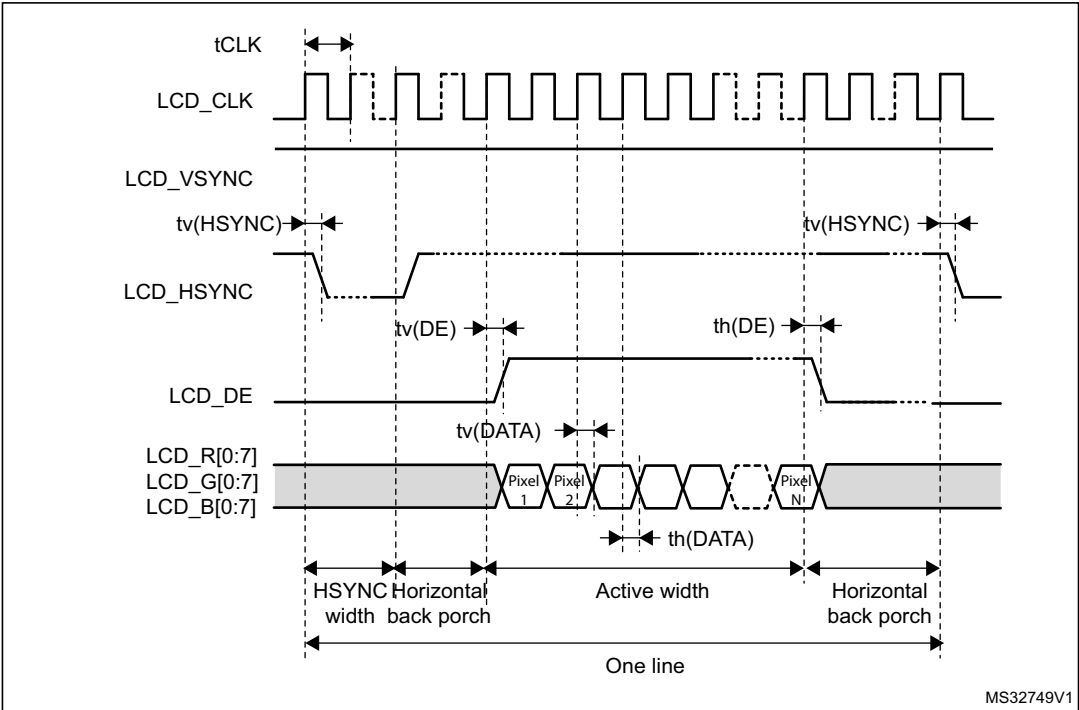
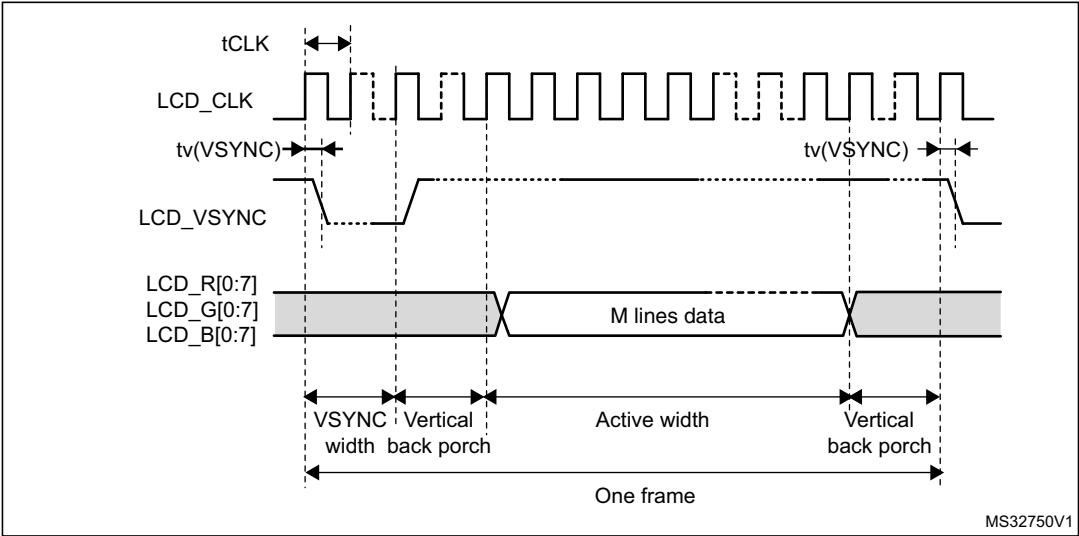


Figure 79. LCD-TFT vertical timing diagram

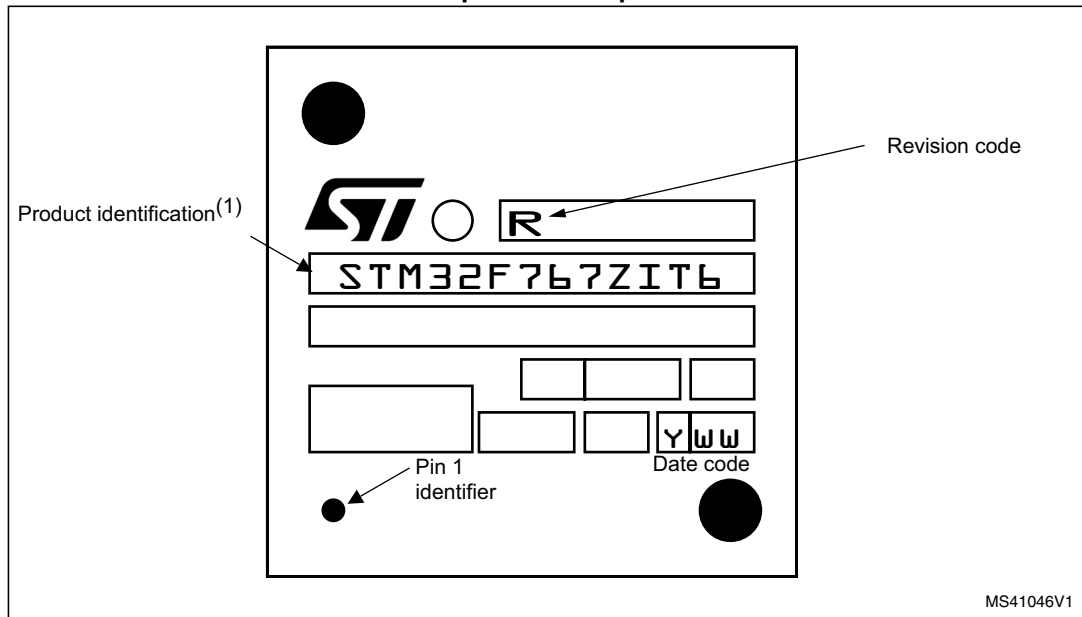


**LQFP144 device marking**

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 88. LQFP144, 20 x 20mm, 144-pin low-profile quad flat package  
top view example**



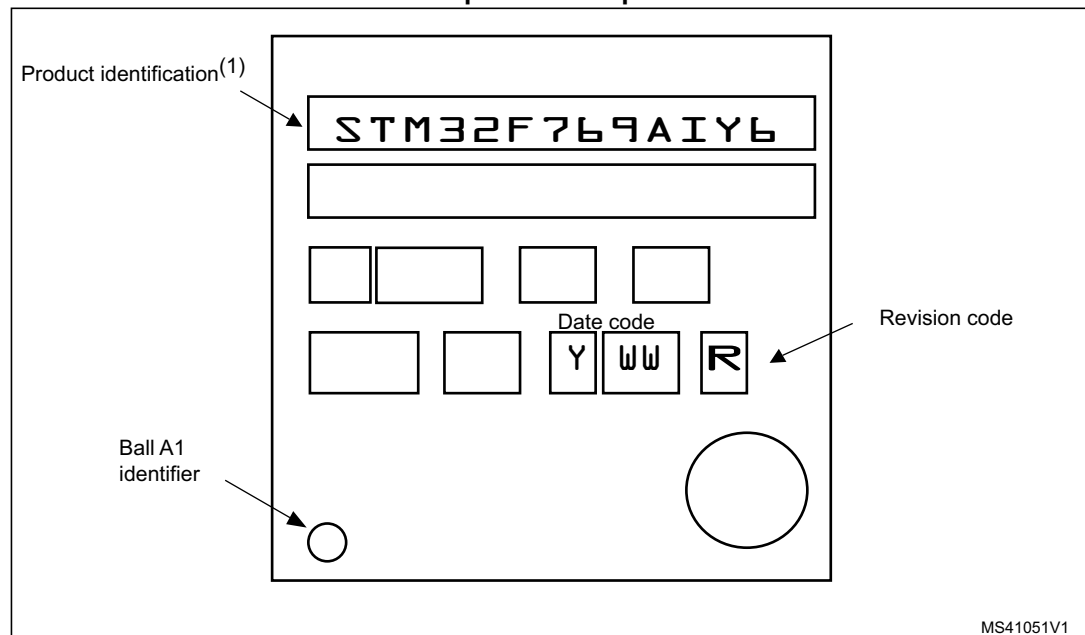
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

**WLCSP180 device marking**

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 97. WLCSP180-bump, 5.5 x 6 mm, 0.4 mm pitch wafer level chip scale package top view example**



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.