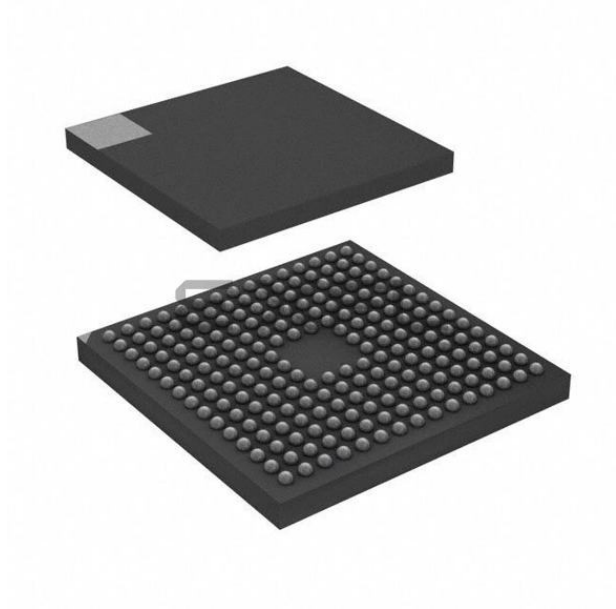

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	168
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	216-TFBGA
Supplier Device Package	216-TFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f767ngh6

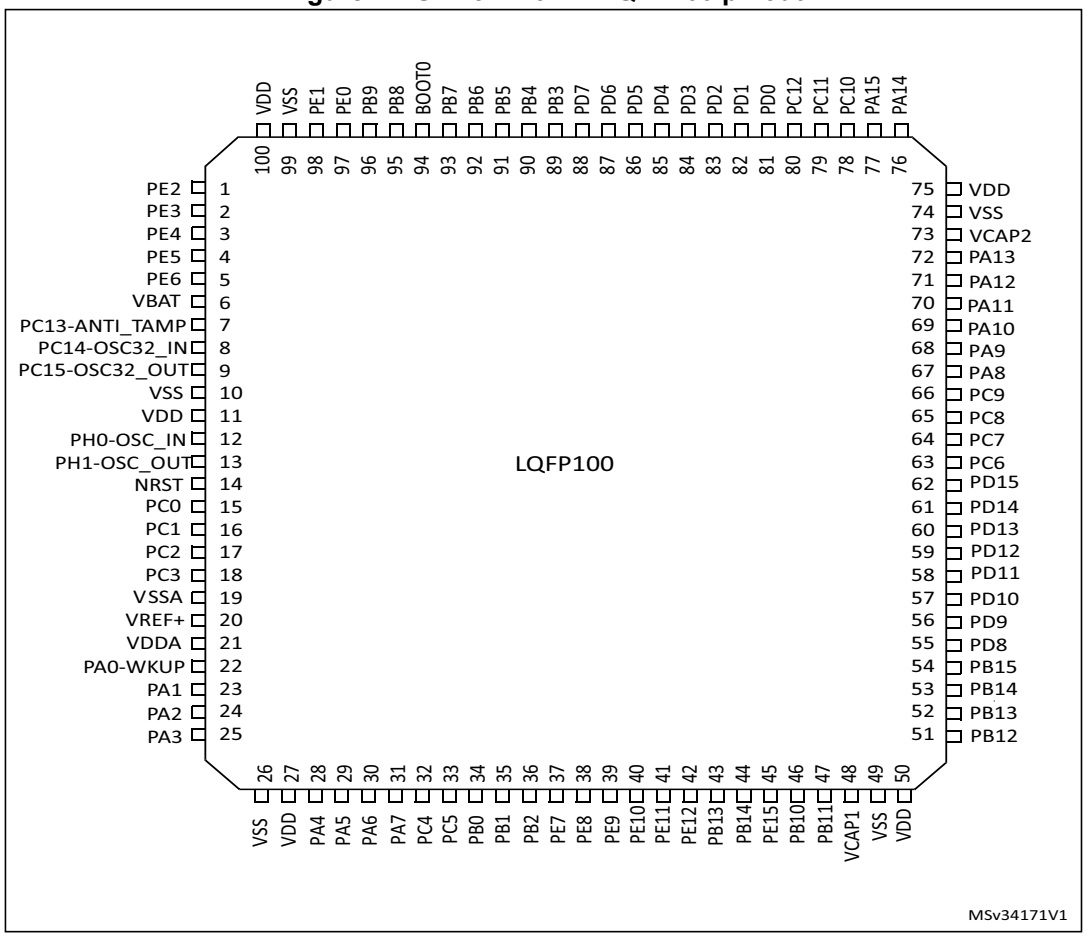
Table 6. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max interface clock (MHz)	Max timer clock (MHz)(1)
Advanced -control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	108	216
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	54	108/216
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	54	108/216
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	108	216
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	108	216
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	54	108/216
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	54	108/216
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	54	108/216

1. The maximum timer clock is either 108 or 216 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

3 Pinouts and pin description

Figure 11. STM32F76xxx LQFP100 pinout



1. The above figure shows the package top view.

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	-	D3	11	11	E4	G10	11	11	E4	PI9	I/O	FT	-	UART4_RX, CAN1_RX, FMC_D30, LCD_VSYNC, EVENTOUT	-
-	-	E3	12	12	D5	H10	12	12	D5	PI10	I/O	FT	-	ETH_MII_RX_ER, FMC_D31, LCD_HSYNC, EVENTOUT	-
-	-	E4	13	13	F3	F11	13	13	F3	PI11	I/O	FT	-	LCD_G6, OTG_HS_ULPI_DIR, EVENTOUT	WKUP6
-	-	F2	14	14	F2	F13	14	14	F2	VSS	S	-	-	-	-
-	-	F3	15	15	F4	F12	15	15	F4	VDD	S	-	-	-	-
-	10	E2	16	16	D2	G11	16	16	D2	PF0	I/O	FT	-	I2C2_SDA, FMC_A0, EVENTOUT	-
-	11	H3	17	17	E2	G12	17	17	E2	PF1	I/O	FT	-	I2C2_SCL, FMC_A1, EVENTOUT	-
-	12	H2	18	18	G2	G13	18	18	G2	PF2	I/O	FT	-	I2C2_SMBA, FMC_A2, EVENTOUT	-
-	-	-	-	19	E3	NC	-	19	E3	PI12	I/O	FT	-	LCD_HSYNC, EVENTOUT	-
-	-	-	-	20	G3	NC	-	20	G3	PI13	I/O	FT	-	LCD_VSYNC, EVENTOUT	-
-	-	-	-	21	H3	NC	-	21	H3	PI14	I/O	FT	-	LCD_CLK, EVENTOUT	-
-	13	J2	19	22	H2	H11	19	22	H2	PF3	I/O	FT	-	FMC_A3, EVENTOUT	ADC3_IN9
-	14	J3	20	23	J2	H12	20	23	J2	PF4	I/O	FT	-	FMC_A4, EVENTOUT	ADC3_IN14
-	15	K3	21	24	K3	H13	21	24	K3	PF5	I/O	FT	-	FMC_A5, EVENTOUT	ADC3_IN15
10	16	G2	22	25	H6	J13	22	25	H6	VSS	S	-	-	-	-
11	17	G3	23	26	H5	J12	23	26	H5	VDD	S	-	-	-	-
-	18	K2	24	27	K2	NC	24	27	K2	PF6	I/O	FT	-	TIM10_CH1, SPI5_NSS, SAI1_SD_B, UART7_RX, QUADSPI_BK1_IO3, EVENTOUT	ADC3_IN4

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
17	28	M4	34	37	M4	NC	34	37	M4	PC2	I/O	FT	-	DFSDM1_CKIN1, SPI2_MISO, DFSDM1_CKOUT, OTG_HS_ULPI_DIR, ETH_MII_TXD2, FMC_SDNE0, EVENTOUT	ADC1_IN12, ADC2_IN12, ADC3_IN12
18	29	M5	35	38	L4	NC	35	38	L4	PC3	I/O	FT	-	DFSDM1_DATIN1, SPI2_MOSI/I2S2_SD, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, FMC_SDCKE0, EVENTOUT	ADC1_IN13, ADC2_IN13, ADC3_IN13
-	30	-	36	39	J5	-	36	39	J5	VDD	S	-	-	-	-
-	-	-	-	-	J6	-	-	-	J6	VSS	S	-	-	-	-
19	31	M1	37	40	M1	M11	37	40	M1	VSSA	S	-	-	-	-
-	-	N1	-	-	N1	-	-	-	N1	VREF-	S	-	-	-	-
20	32	P1	38	41	P1	-	38	41	P1	VREF+	S	-	-	-	-
21	33	R1	39	42	R1	M12	39	42	R1	VDDA	S	-	-	-	-
22	34	N3	40	43	N3	M13	40	43	N3	PA0-WKUP	I/O	FT	(4)	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, SAI2_SD_B, ETH_MII_CRS, EVENTOUT	ADC1_IN0, ADC2_IN0, ADC3_IN0, WKUP1
23	35	N2	41	44	N2	J11	41	44	N2	PA1	I/O	FT	-	TIM2_CH2, TIM5_CH2, USART2_RTS, UART4_RX, QUADSPI_BK1_IO3, SAI2_MCLK_B, ETH_MII_RX_CLK/ETH_RMII_REF_CLK, LCD_R2, EVENTOUT	ADC1_IN1, ADC2_IN1, ADC3_IN1

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
24	36	P2	42	45	P2	J10	42	45	P2	PA2	I/O	FT	-	TIM2_CH3, TIM5_CH3, TIM9_CH1, USART2_TX, SAI2_SCK_B, ETH_MDIO, MDIOS_MDIO, LCD_R1, EVENTOUT	ADC1_IN2, ADC2_IN2, ADC3_IN2, WKUP2
-	-	F4	43	46	K4	L10	43	46	K4	PH2	I/O	FT	-	LPTIM1_IN2, QUADSPI_BK2_IO0, SAI2_SCK_B, ETH_MII_CRS, FMC_SDCKE0, LCD_R0, EVENTOUT	-
-	-	G4	44	47	J4	K10	44	47	J4	PH3	I/O	FT	-	QUADSPI_BK2_IO1, SAI2_MCLK_B, ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT	-
-	-	H4	45	48	H4	N12	45	48	H4	PH4	I/O	FT	-	I2C2_SCL, LCD_G5, OTG_HS_ULPI_NXT, LCD_G4, EVENTOUT	-
-	-	J4	46	49	J3	N11	46	49	J3	PH5	I/O	FT	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	-
25	37	R2	47	50	R2	M10	47	50	R2	PA3	I/O	FT	-	TIM2_CH4, TIM5_CH4, TIM9_CH2, USART2_RX, LCD_B2, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	ADC1_IN3, ADC2_IN3, ADC3_IN3
26	38	-	-	51	K6	J9	-	51	K6	VSS	S	-	-	-	-
-	-	L4	48	-	L5	-[5]	48	-	L5	BYPASS_ REG	I	FT	-	-	-
27	39	K4	49	52	K5	K9	49	52	K5	VDD	S	-	-	-	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
40	63	R9	73	84	R9	J6	73	84	R9	PE10	I/O	FT	-	TIM1_CH2N, DFSDM1_DATIN4, UART7_CTS, QUADSPI_BK2_IO3, FMC_D7, EVENTOUT	-
41	64	P10	74	85	P10	K6	74	85	P10	PE11	I/O	FT	-	TIM1_CH2, SPI4_NSS, DFSDM1_CKIN4, SAI2_SD_B, FMC_D8, LCD_G3, EVENTOUT	-
42	65	R10	75	86	R10	L6	75	86	R10	PE12	I/O	FT	-	TIM1_CH3N, SPI4_SCK, DFSDM1_DATIN5, SAI2_SCK_B, FMC_D9, LCD_B4, EVENTOUT	-
43	66	N11	76	87	R12	P6	76	87	R12	PE13	I/O	FT	-	TIM1_CH3, SPI4_MISO, DFSDM1_CKIN5, SAI2_FS_B, FMC_D10, LCD_DE, EVENTOUT	-
44	67	P11	77	88	P11	N6	77	88	P11	PE14	I/O	FT	-	TIM1_CH4, SPI4_MOSI, SAI2_MCLK_B, FMC_D11, LCD_CLK, EVENTOUT	-
45	68	R11	78	89	R11	M6	78	89	R11	PE15	I/O	FT	-	TIM1_BKIN, FMC_D12, LCD_R7, EVENTOUT	-
46	69	R12	79	90	P12	K5	79	90	P12	PB10	I/O	FT	-	TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, DFSDM1_DATIN7, USART3_TX, QUADSPI_BK1_NCS, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
96	140	B4	168	199	B4	D9	168	199	B4	PB9	I/O	FT	-	I2C4_SDA, TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, DFSDM1_DATIN7, UART5_TX, CAN1_TX, SDMMC2_D5, I2C4_SMBA, SDMMC1_D5, DCMI_D7, LCD_B7, EVENTOUT	-
97	141	A4	169	200	A6	C9	169	200	A6	PE0	I/O	FT	-	TIM4_ETR, LPTIM1_ETR, UART8_RX, SAI2_MCLK_A, FMC_NBL0, DCMI_D2, EVENTOUT	-
98	142	A3	170	201	A5	B10	170	201	A5	PE1	I/O	FT	-	LPTIM1_IN2, UART8_TX, FMC_NBL1, DCMI_D3, EVENTOUT	-
99	-	D5	-	202	F6	A11	-	202	F6	VSS	S	-	-	-	-
-	143	C6	171	203	E5	C10	171	203	E5	PDR_ON	S	-	-	-	-
100	144	C5	172	204	E7	B11	172	204	E7	VDD	S	-	-	-	-
-	-	D4	173	205	C3	D10	173	205	C3	PI4	I/O	FT	-	TIM8_BKIN, SAI2_MCLK_A, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	C4	174	206	D3	D11	174	206	D3	PI5	I/O	FT	-	TIM8_CH1, SAI2_SCK_A, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-
-	-	C3	175	207	D6	C11	175	207	D6	PI6	I/O	FT	-	TIM8_CH2, SAI2_SD_A, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	C2	176	208	D4	B12	176	208	D4	PI7	I/O	FT	-	TIM8_CH3, SAI2_FS_A, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-

Table 12. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM1/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port H	PH14	-	-	-	TIM8_CH2N	-	-	-	-	UART4_RX	CAN1_RX	-	-	FMC_D22	DCMI_D4	LCD_G3	EVENTOUT
	PH15	-	-	-	TIM8_CH3N	-	-	-	-	-	-	-	-	FMC_D23	DCMI_D11	LCD_G4	EVENTOUT
Port I	PI0	-	-	TIM5_CH4	-	-	SPI2_NSS/I2S2_WS	-	-	-	-	-	-	FMC_D24	DCMI_D13	LCD_G5	EVENTOUT
	PI1	-	-	-	TIM8_BKIN2	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	-	FMC_D25	DCMI_D8	LCD_G6	EVENTOUT
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO	-	-	-	-	-	-	FMC_D26	DCMI_D9	LCD_G7	EVENTOUT
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	FMC_D27	DCMI_D10	-	EVENTOUT
	PI4	-	-	-	TIM8_BKIN	-	-	-	-	-	-	SAI2_MCK_A	-	FMC_NBL2	DCMI_D5	LCD_B4	EVENTOUT
	PI5	-	-	-	TIM8_CH1	-	-	-	-	-	-	SAI2_SCK_A	-	FMC_NBL3	DCMI_VSYNC	LCD_B5	EVENTOUT
	PI6	-	-	-	TIM8_CH2	-	-	-	-	-	-	SAI2_SD_A	-	FMC_D28	DCMI_D6	LCD_B6	EVENTOUT
	PI7	-	-	-	TIM8_CH3	-	-	-	-	-	-	SAI2_FS_A	-	FMC_D29	DCMI_D7	LCD_B7	EVENTOUT
	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PI9	-	-	-	-	-	-	-	-	UART4_RX	CAN1_RX	-	-	FMC_D30	-	LCD_VSYNC	EVENTOUT
	PI10	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_RX_ER	FMC_D31	-	LCD_HSYNC	EVENTOUT
	PI11	-	-	-	-	-	-	-	-	-	LCD_G6	OTG_HS_ULPI_DIR	-	-	-	-	EVENTOUT

Table 12. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM1/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port I	PI12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_HSYNC	EVENTOUT
	PI13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_VSYNC	EVENTOUT
	PI14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_CLK	EVENTOUT
	PI15	-	-	-	-	-	-	-	-	-	LCD_G2	-	-	-	-	LCD_R0	EVENTOUT
Port J	PJ0	-	-	-	-	-	-	-	-	-	LCD_R7	-	-	-	-	LCD_R1	EVENTOUT
	PJ1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R2	EVENTOUT
	PJ2	-	-	-	-	-	-	-	-	-	-	-	-	-	DSI_TE	LCD_R3	EVENTOUT
	PJ3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R4	EVENTOUT
	PJ4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R5	EVENTOUT
	PJ5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R6	EVENTOUT
	PJ6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R7	EVENTOUT
	PJ7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G0	EVENTOUT
	PJ8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G1	EVENTOUT
	PJ9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G2	EVENTOUT
	PJ10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G3	EVENTOUT

Table 12. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM1/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port J	PJ11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G4	EVENTOUT
	PJ12	-	-	-	-	-	-	-	-	-	LCD_G3	-	-	-	-	LCD_B0	EVENTOUT
	PJ13	-	-	-	-	-	-	-	-	-	LCD_G4	-	-	-	-	LCD_B1	EVENTOUT
	PJ14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B2	EVENTOUT
	PJ15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B3	EVENTOUT
Port K	PK0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G5	EVENTOUT
	PK1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G6	EVENTOUT
	PK2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G7	EVENTOUT
	PK3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B4	EVENTOUT
	PK4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B5	EVENTOUT
	PK5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B6	EVENTOUT
	PK6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B7	EVENTOUT
	PK7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DE	EVENTOUT

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 1.7 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 22*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 23*.

Figure 22. Pin loading conditions

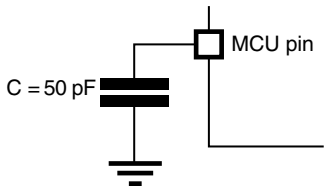


Figure 23. Pin input voltage

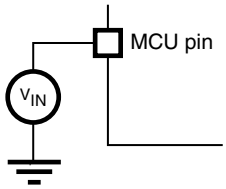


Table 30. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (Dual bank mode) on ITCM interface (ART disabled), regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					TA= 25 °C	TA=85 °C	TA=105 °C	
I_{DD}	Supply current in RUN mode	All peripherals enabled(2)(3)	216	191	218	255	-	mA
			200	178	195	241	269	
			180	164	179	214	236	
			168	147	160	192	212	
			144	121	130	157	175	
			60	60	66	93	111	
			25	28	33	59	77	
		All peripherals disabled(3)	216	93	104	150	-	
			200	87	97	144	171	
			180	83	92	126	148	
			168	75	82	114	134	
			144	65	71	97	115	
			60	35	40	66	84	
			25	16	20	47	64	

1. Guaranteed by characterization results, unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 80. internal reference voltage (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{Coeff}(2)	Temperature coefficient	-	-	30	50	ppm/°C
t_{START}(2)	Startup time	-	-	6	10	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

Table 81. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C V_{DDA} = 3.3 V	0x1FF0 F44A - 0x1FF0 F44B

5.3.28 DAC electrical characteristics

Table 82. DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	1.7(1)	-	3.6	V	-
V_{REF+}	Reference supply voltage	1.7(1)	-	3.6	V	$V_{REF+} \leq V_{DDA}$
V_{SSA}	Ground	0	-	0	V	-
R_{LOAD}(2)	Resistive load with buffer ON	5	-	-	kΩ	-
R_O(2)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(2)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x1C7) to (0xE38) at V_{REF+} = 1.7 V
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer OFF	-	-	V_{REF+} – 1LSB	V	
I_{VREF+}(4)	DAC DC V_{REF} current consumption in quiescent mode (Standby mode)	-	170	240	µA	With no load, worst code (0x800) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
		-	50	75		With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs

Figure 57. Ethernet SMI timing diagram

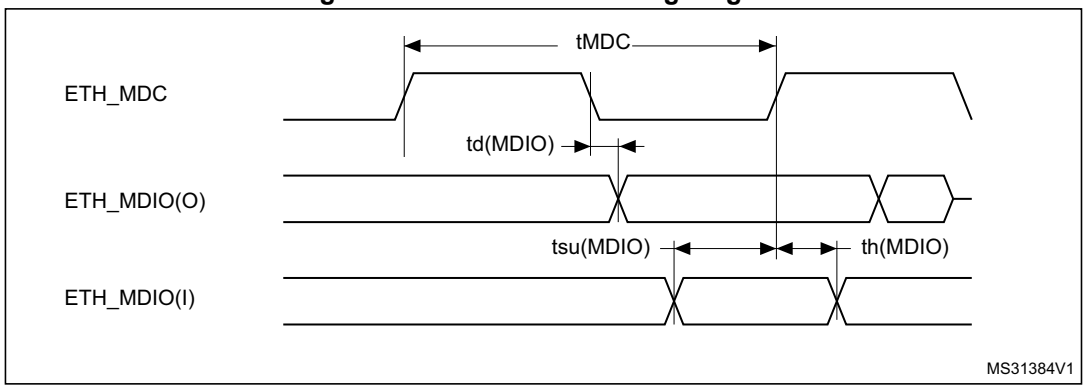


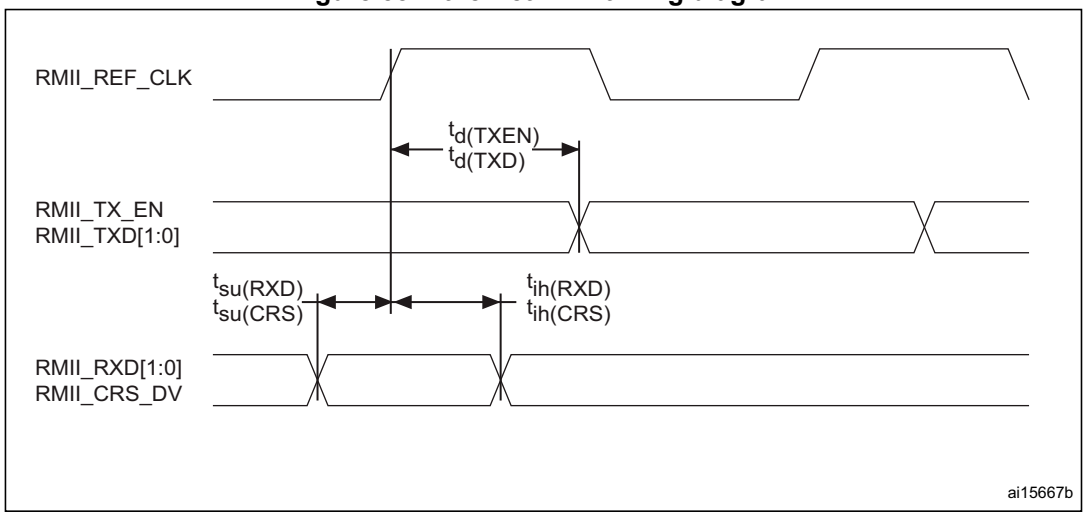
Table 96. Dynamics characteristics: Ethernet MAC signals for SMI(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time(2.38 MHz)	400	400	403	ns
$T_{d(MDIO)}$	Write data valid time	T_{HCLK} + 1	T_{HCLK} + 1.5	T_{HCLK} + 3	
$t_{su(MDIO)}$	Read data setup time	12.5	-	-	
$t_{h(MDIO)}$	Read data hold time	0	-	-	

1. Guaranteed by characterization results.

Table 97 gives the list of Ethernet MAC signals for the RMII and *Figure 58* shows the corresponding timing diagram.

Figure 58. Ethernet RMII timing diagram



Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output characteristics.

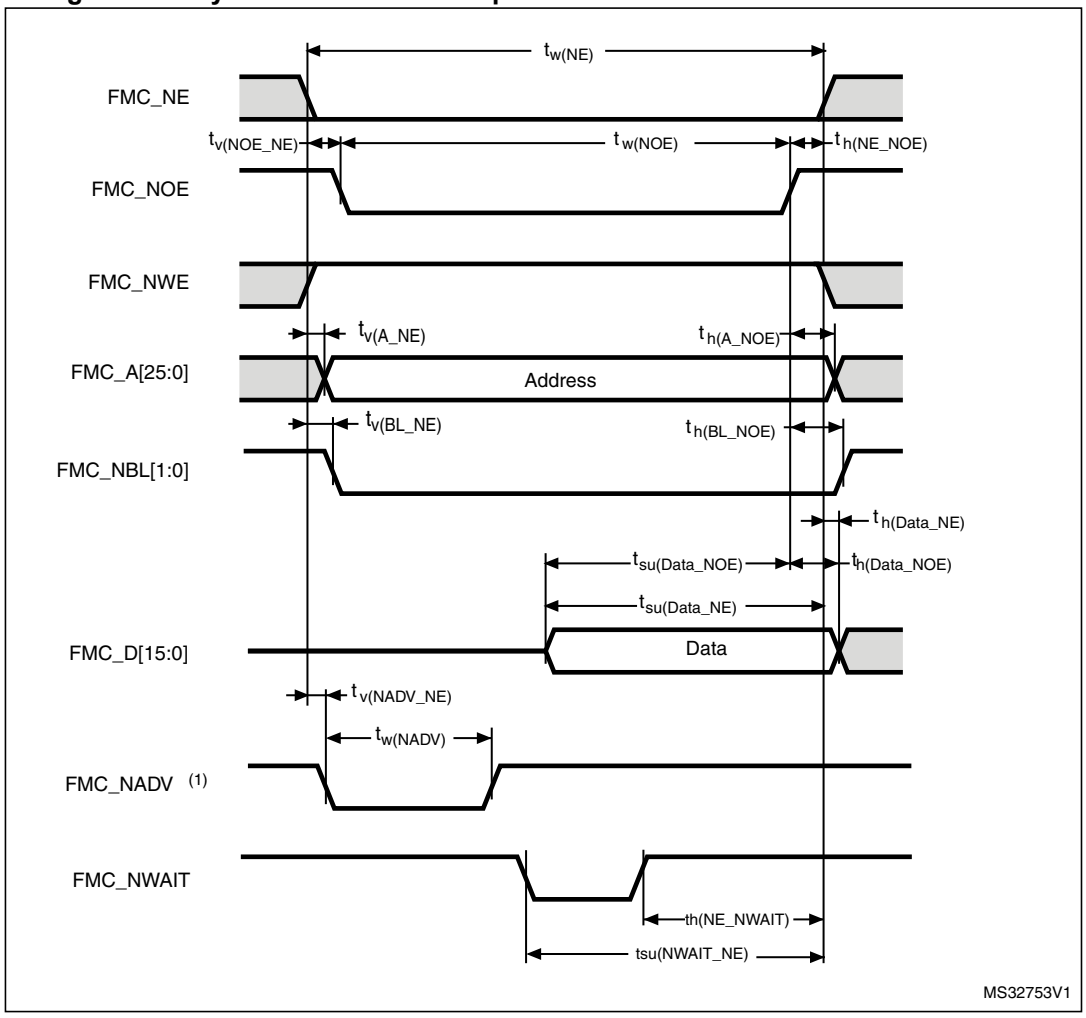
Asynchronous waveforms and timings

Figure 61 through *Figure 64* represent asynchronous waveforms and *Table 100* through *Table 107* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode , DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- Capcitive load CL = 30 pF

In all timing tables, the T_{HCLK} is the HCLK clock period

Figure 61. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

1. Guaranteed by characterization results.

Table 107. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK} - 1$	$9T_{HCLK} + 1$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{HCLK} - 0.5$	$7T_{HCLK} + 0.5$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK} + 2$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK} - 1$	-	

1. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 65 through *Figure 68* represent synchronous waveforms and *Table 108* through *Table 111* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1;
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM
- CL = 30 pF on data and address lines. CL = 10 pF on FMC_CLK unless otherwise specified.

In all the timing tables, the T_{HCLK} is the HCLK clock period.

  - For 2.7 V≤ V_{DD}≤ 3.6 V, maximum FMC_CLK = 100 MHz at CL=20 pF or 90 MHz at CL=30 pF (on FMC_CLK).
  - For 1.71 V≤ V_{DD}<2.7 V, maximum FMC_CLK = 70 MHz at CL=10 pF (on FMC_CLK).

Figure 71. NAND controller waveforms for common memory read access

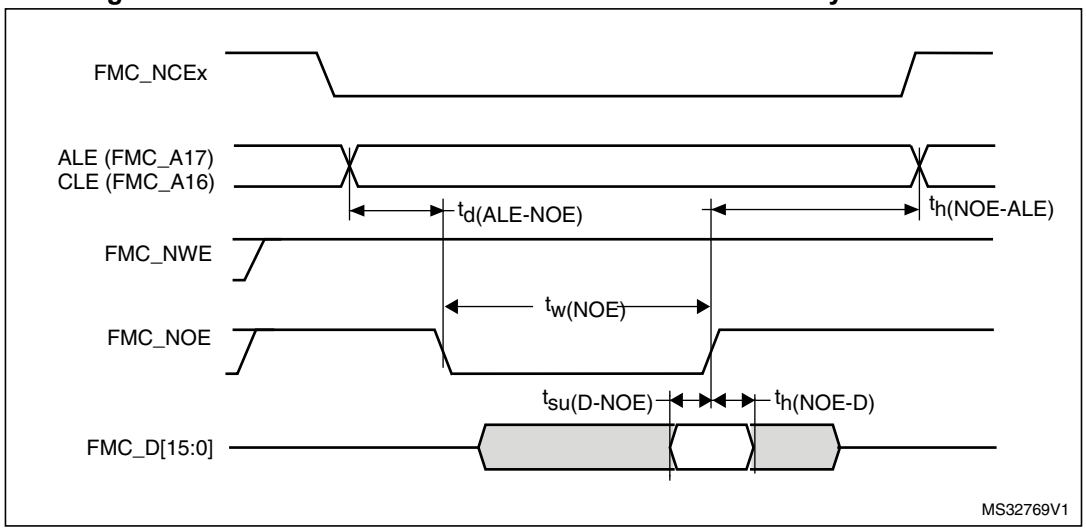


Figure 72. NAND controller waveforms for common memory write access

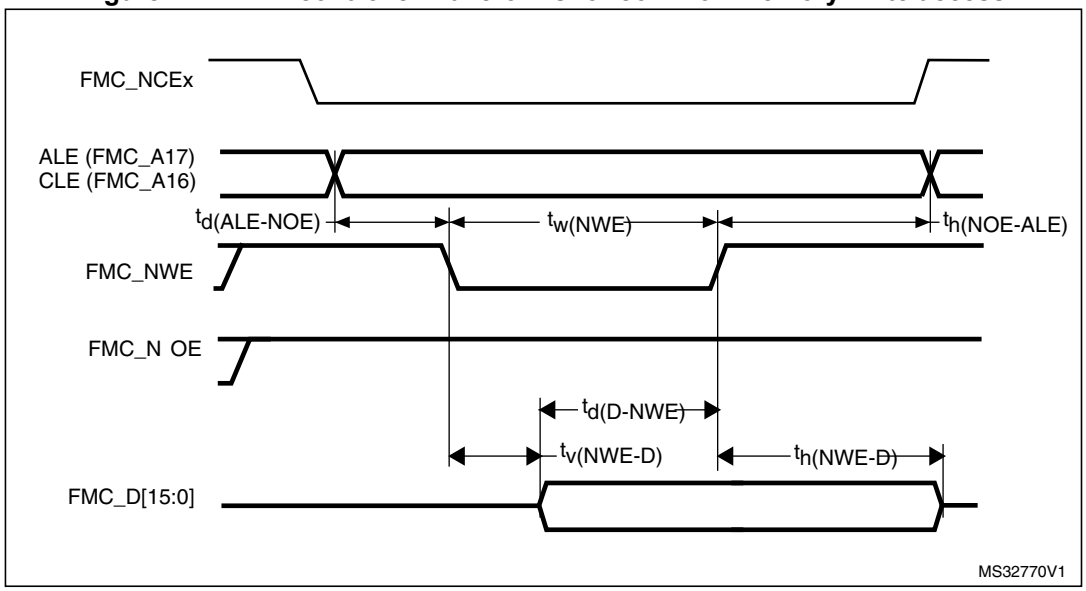


Table 112. Switching characteristics for NAND Flash read cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FMC_NOE low width	$4T_{HCLK} - 0.5$	$4T_{HCLK} + 0.5$	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	11	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	$3T_{HCLK} + 1$	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$4T_{HCLK} - 2$	-	

1. Guaranteed by characterization results.

Table 123. Dynamic characteristics: SD / MMC characteristics, V_{DD}=2.7V to 3.6V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDMMC_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	fpp =50 MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50 MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	fpp =50 MHz	3.5	-	-	ns
t_{IH}	Input hold time HS	fpp =50 MHz	2.5	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	fpp =50 MHz	-	11	12	ns
t_{OH}	Output hold time HS	fpp =50 MHz	9	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
tISUD	Input setup time SD	fpp =25 MHz	3.5	-	-	ns
tIHD	Input hold time SD	fpp =25 MHz	2.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
tOVD	Output valid default time SD	fpp =25 MHz	-	0.5	1.5	ns
tOHD	Output hold default time SD	fpp =25 MHz	0	-	-	

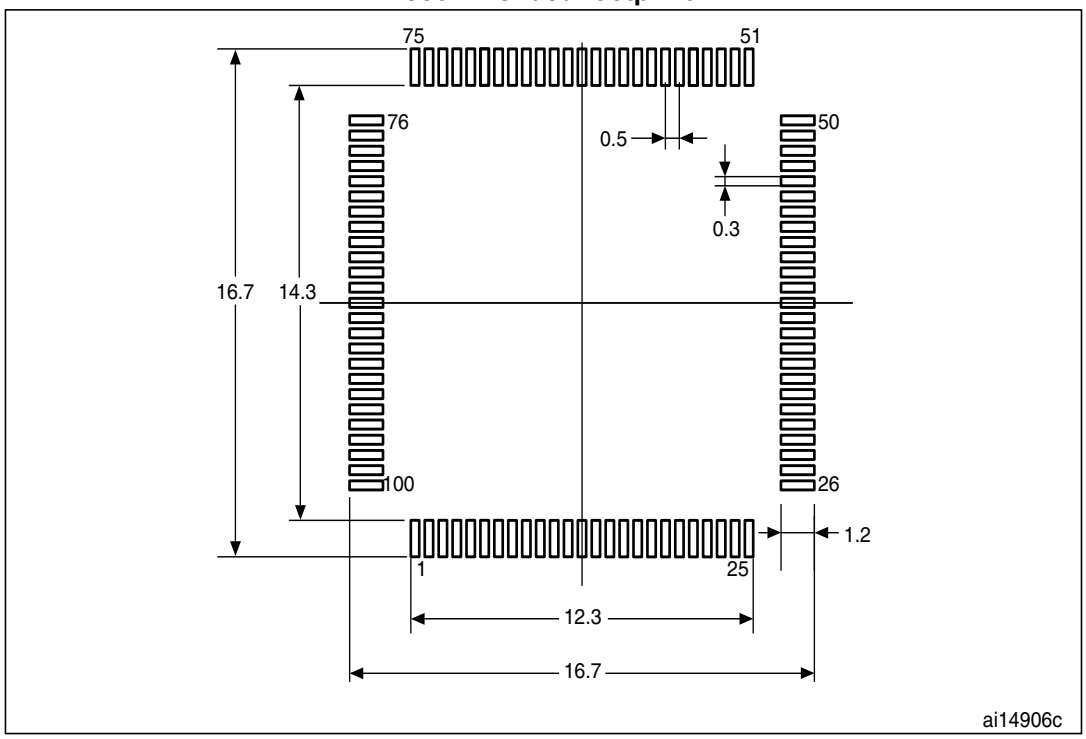
1. Guaranteed by characterization results.

Table 124. Dynamic characteristics: eMMC characteristics, V_{DD}=1.71V to 1.9V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDMMC_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	fpp =50 MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50 MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	fpp =50 MHz	3	-	-	ns
t_{IH}	Input hold time HS	fpp =50 MHz	4	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	fpp =50 MHz	-	11	15.5	ns
t_{OH}	Output hold time HS	fpp =50 MHz	9.5	-	-	

1. Guaranteed by characterization results.
2. Cload = 20 pF.

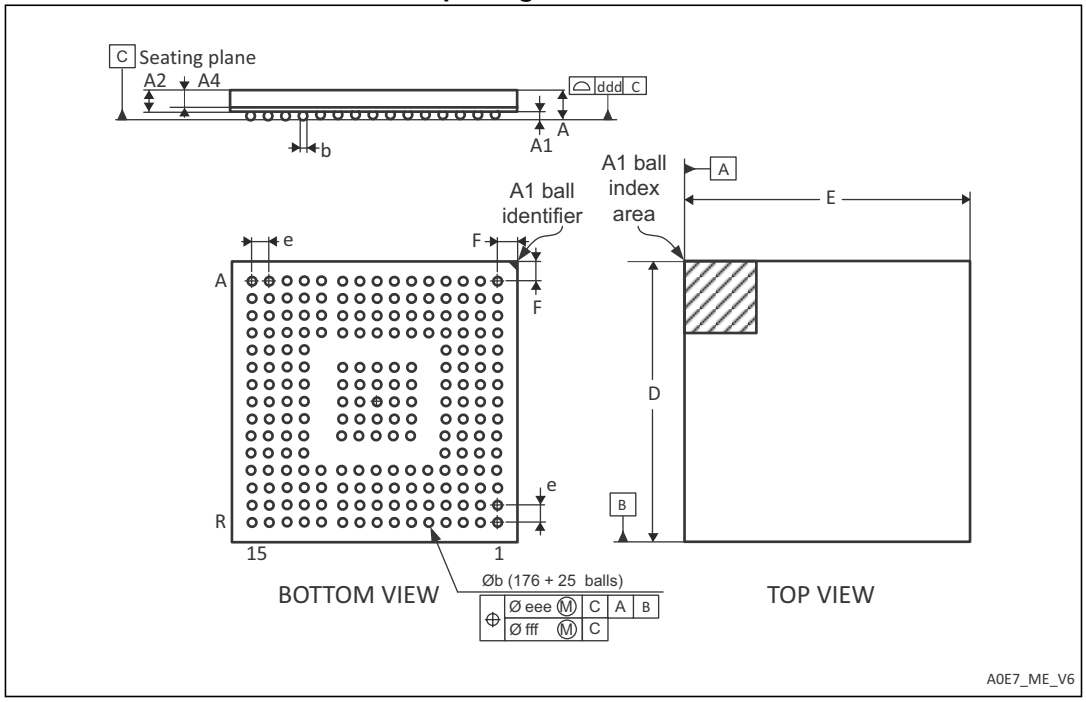
Figure 84. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

6.6 UFBGA176+25, 10 x 10, 0.65 mm ultra thin fine-pitch ball grid array package information

Figure 98. UFBGA176+25, 10 × 10 × 0.65 mm ultra thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 131. UFBGA176+25, 10 × 10 × 0.65 mm ultra thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.002	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	9.950	10.000	10.050	0.3917	0.3937	0.3957
E	9.950	10.000	10.050	0.3917	0.3937	0.3957
e	-	0.650	-	-	0.0256	-
F	0.400	0.450	0.500	0.0157	0.0177	0.0197
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.