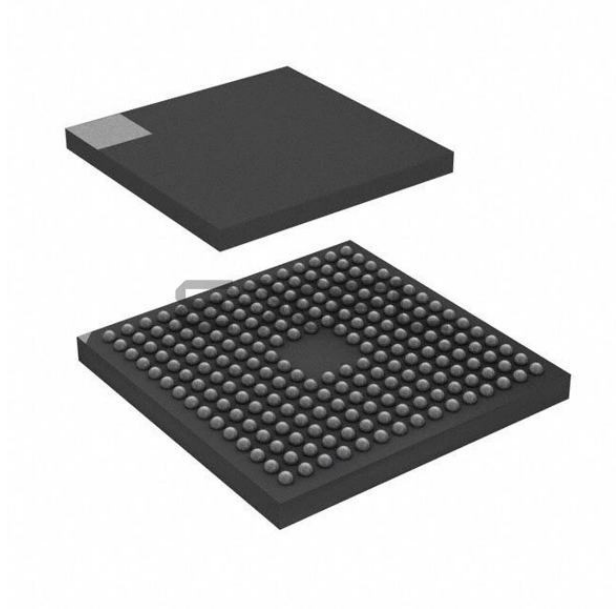

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	168
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	216-TFBGA
Supplier Device Package	216-TFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f767nih6

Table 2. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx features and peripheral counts (continued)

Peripherals	STM32F 765Vx	STM32F767 /769Vx	STM32F 765Zx	STM32F767 /769Zx	STM32F 769Ax	STM32F 768Ax	STM32F 765Ix	STM32F767 /769Ix	STM32F 765Bx	STM32F767 /769Bx	STM32F 765Nx	STM32F767 /769Nx
Chrom-ART Accelerator™ (DMA2D)	Yes											
JPEG codec	No	Yes	No	Yes			No	Yes	No	Yes	No	Yes
GPIOs	82		114		129		140	132	168	159	168	159
DFSDM1	Yes (4 filters)											
12-bit ADC	3											
Number of channels	16		24									
12-bit DAC Number of channels	Yes 2											
Maximum CPU frequency	216 MHz(5)											
Operating voltage	1.7 to 3.6 V(6)											
Operating temperatures	Ambient temperatures: –40 to +85 °C /–40 to +105 °C											
	Junction temperature: –40 to + 125 °C											
Package	LQFP100		LQFP144		WLCSP180		UFBGA176(7) LQFP176		LQFP208		TFBGA216	

1. For the LQFP100 package, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.
2. The SPI1, SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. SDMMC2 supports a dedicated power rail for clock, command and data 0..4 lines, feature available starting from 144 pin package.
4. DSI host interface is only available on STM32F769x sales types.
5. 216 MHz maximum frequency for - 40°C to + 85°C ambient temperature range (200 MHz maximum frequency for - 40°C to + 105°C ambient temperature range).
6. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the internal reset is OFF (refer to *Section 2.18.2: Internal reset OFF*).
7. UFBGA176 is not available for STM32F769x sales types.

2.31 SD/SDIO/MMC card host interface (SDMMC)

SDMMC host interfaces are available, that support the MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 50 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDMMC Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDMMC/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

The SDMMC can be served by the DMA controller

2.32 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

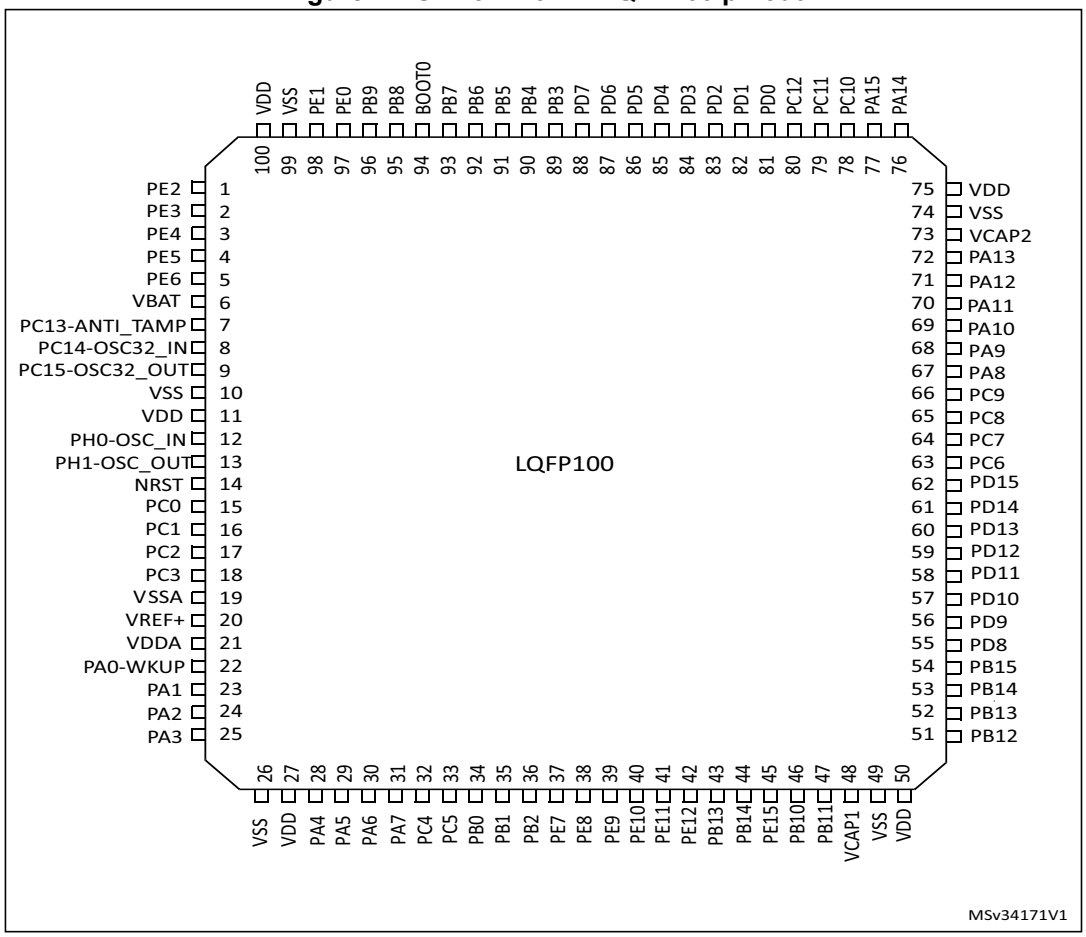
The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

3 Pinouts and pin description

Figure 11. STM32F76xxx LQFP100 pinout



1. The above figure shows the package top view.

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	-	-	-	60	L6	-	-	60	L6	VSS	S	-	-	-	-
34	46	R5	56	61	R5	P10	56	61	R5	PB0	I/O	FT	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, DFSDM1_CKOUT, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, LCD_G1, EVENTOUT	ADC1_IN8, ADC2_IN8
35	47	R4	57	62	R4	J8	57	62	R4	PB1	I/O	FT	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN1, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, LCD_G0, EVENTOUT	ADC1_IN9, ADC2_IN9
36	48	M6	58	63	M5	J7	58	63	M5	PB2	I/O	FT	-	SAI1_SD_A, SPI3_MOSI/I2S3_SD, QUADSPI_CLK, DFSDM1_CKIN1, EVENTOUT	-
-	-	-	-	64	G4	NC	-	64	G4	PI15	I/O	FT	-	LCD_G2, LCD_R0, EVENTOUT	-
-	-	-	-	65	R6	NC	-	65	R6	PJ0	I/O	FT	-	LCD_R7, LCD_R1, EVENTOUT	-
-	-	-	-	66	R7	NC	-	66	R7	PJ1	I/O	FT	-	LCD_R2, EVENTOUT	-
-	-	-	-	67	P7	NC	-	67	P7	PJ2	I/O	FT	-	DSI_TE, LCD_R3, EVENTOUT	-
-	-	-	-	68	N8	NC	-	68	N8	PJ3	I/O	FT	-	LCD_R4, EVENTOUT	-
-	-	-	-	69	M9	NC	-	69	M9	PJ4	I/O	FT	-	LCD_R5, EVENTOUT	-
-	49	R6	59	70	P8	N9	59	70	P8	PF11	I/O	FT	-	SPI5_MOSI, SAI2_SD_B, FMC_SDNRAS, DCMI_D12, EVENTOUT	-
-	50	P6	60	71	M6	K7	60	71	M6	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
96	140	B4	168	199	B4	D9	168	199	B4	PB9	I/O	FT	-	I2C4_SDA, TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, DFSDM1_DATIN7, UART5_TX, CAN1_TX, SDMMC2_D5, I2C4_SMBA, SDMMC1_D5, DCMI_D7, LCD_B7, EVENTOUT	-
97	141	A4	169	200	A6	C9	169	200	A6	PE0	I/O	FT	-	TIM4_ETR, LPTIM1_ETR, UART8_RX, SAI2_MCLK_A, FMC_NBL0, DCMI_D2, EVENTOUT	-
98	142	A3	170	201	A5	B10	170	201	A5	PE1	I/O	FT	-	LPTIM1_IN2, UART8_TX, FMC_NBL1, DCMI_D3, EVENTOUT	-
99	-	D5	-	202	F6	A11	-	202	F6	VSS	S	-	-	-	-
-	143	C6	171	203	E5	C10	171	203	E5	PDR_ON	S	-	-	-	-
100	144	C5	172	204	E7	B11	172	204	E7	VDD	S	-	-	-	-
-	-	D4	173	205	C3	D10	173	205	C3	PI4	I/O	FT	-	TIM8_BKIN, SAI2_MCLK_A, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	C4	174	206	D3	D11	174	206	D3	PI5	I/O	FT	-	TIM8_CH1, SAI2_SCK_A, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-
-	-	C3	175	207	D6	C11	175	207	D6	PI6	I/O	FT	-	TIM8_CH2, SAI2_SD_A, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	C2	176	208	D4	B12	176	208	D4	PI7	I/O	FT	-	TIM8_CH3, SAI2_FS_A, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-

Table 12. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM1/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	FMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	-	FMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	-	FMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A5	-	-	EVENTOUT
	PF6	-	-	-	TIM10_CH1	-	SPI5_NSS	SAI1_SD_B	-	UART7_Rx	QUADSPI_BK1_IO3	-	-	-	-	-	EVENTOUT
	PF7	-	-	-	TIM11_CH1	-	SPI5_SCK	SAI1_MCLK_B	-	UART7_Tx	QUADSPI_BK1_IO2	-	-	-	-	-	EVENTOUT
	PF8	-	-	-	-	-	SPI5_MISO	SAI1_SCK_B	-	UART7_RTS	TIM13_CH1	QUADSPI_BK1_IO0	-	-	-	-	EVENTOUT
	PF9	-	-	-	-	-	SPI5_MOSI	SAI1_FS_B	-	UART7_CTS	TIM14_CH1	QUADSPI_BK1_IO1	-	-	-	-	EVENTOUT
	PF10	-	-	-	-	-	-	-	-	-	QUADSPI_CLK	-	-	-	DCMI_D11	LCD_DE	EVENTOUT
	PF11	-	-	-	-	-	SPI5_MOSI	-	-	-	-	SAI2_SD_B	-	FMC_SDNRAS	DCMI_D12	-	EVENTOUT

Table 13. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx register boundary addresses(1) (continued)

Bus	Boundary address	Peripheral
	0x4001 7C00 - 0x4001 FFFF	Reserved
APB2	0x4001 7800 - 0x4001 7BFF	MDIOS
	0x4001 7400 - 0x4001 77FF	DFSDM1
	0x4001 6C00 - 0x4001 73FF	DSI Host
	0x4001 6800 - 0x4001 6BFF	LCD-TFT
	0x4001 6000 - 0x4001 67FF	Reserved
	0x4001 5C00 - 0x4001 5FFF	SAI2
	0x4001 5800 - 0x4001 5BFF	SAI1
	0x4001 5400 - 0x4001 57FF	SPI6
	0x4001 5000 - 0x4001 53FF	SPI5
	0x4001 4C00 - 0x4001 4FFF	Reserved
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4
	0x4001 3000 - 0x4001 33FF	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	SDMMC1
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1 - ADC2 - ADC3
	0x4001 1C00 - 0x4001 1FFF	SDMMC2
	0x4001 1800 - 0x4001 1BFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1

Table 28. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (Dual bank mode), regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					TA= 25 °C	TA=85 °C	TA=105 °C	
I_{DD}	Supply current in RUN mode	All peripherals enabled(2)(3)	216	176	194	240	-	mA
			200	164	181	227	255	
			180	149	163	198	220	
			168	133	145	178	198	
			144	106	116	143	161	
			60	54	60	87	105	
			25	27	31	58	76	
		All peripherals disabled(3)	216	77	88	135	-	
			200	72	82	129	157	
			180	67	75	110	131	
			168	60	67	99	120	
			144	50	56	83	101	
			60	29	34	60	78	
			25	15	19	45	63	

1. Guaranteed by characterization results, unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 39. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ)(1)			Unit
		Scale 1	Scale 2	Scale 3	
APB2 (up to 108 MHz)	TIM1	24.1	23.8	19.6	µA/MHz
	TIM8	24.5	24.2	20.0	
	USART1	17.7	17.4	14.3	
	USART6	11.9	11.8	9.4	
	ADC1(5)	4.5	4.7	3.5	
	ADC2(5)	4.5	4.7	3.3	
	ADC3(5)	4.5	4.6	3.3	
	SDMMC1	8.4	8.3	6.9	
	SDMMC2	8.2	8.2	6.4	
	SPI1/I2S1(3)	3.9	3.6	3.1	
	SPI4	3.9	3.6	3.1	
	SYSCFG	2.5	2.2	1.9	
	TIM9	8.0	8.0	6.2	
	TIM10	5.0	5.1	3.7	
	TIM11	6.9	6.9	5.3	
	SPI5	2.7	2.8	1.8	
	SPI6	3.1	3.2	2.2	
	SAI1	3.2	3.3	2.2	
	DFSDM1	10.9	10.7	9.0	
	SAI2	3.9	3.9	2.8	
	MDIO	7.1	7.0	5.8	
	LTDC	51.2	50.3	41.8	
	DSI	8.5	8.4	8.1	

1. When the I/O compensation cell is ON, I_{DD} typical value increases by 0.22 mA.
2. The BusMatrix is automatically active when at least one master is ON.
3. To enable an I2S peripheral, first set the I2SMOD bit and then the I2SE bit in the SPI_I2SCFGR register.
4. When the DAC is ON and EN1/2 bits are set in DAC_CR register, add an additional power consumption of 0.75 mA per DAC channel for the analog part.
5. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 52. MIPI D-PHY AC characteristics LP mode and HS/LP transitions(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	-	62+52*UI	-	-	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of an HS transmission burst.	-	60	-	-	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	-	40+4*UI	-	85+6*UI	
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE+}$ Time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	-	145+10*UI	-	-	
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	-	Max (n*8*UI, 60+n*4*UI)	-	-	
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	-	100	-	-	
T_{REOT}	30%-85% rise time and fall time	-	-	-	35	
T_{EOT}	Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$, to the start of the LP-11 state following a HS burst.	-	-	-	105+ n*12UI	

1. Guaranteed based on test during characterization.

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 61. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}] 8/200 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, TFBGA216 package, conforming to IEC61967-2 ART/L1-cache ON, over-drive ON, all peripheral clocks enabled, clock dithering disabled.	0.1 to 30 MHz	5	dBµV
			30 to 130 MHz	10	
			130 MHz to 1 GHz	18	
			1 GHz to 2 GHz	10	
			EMI Level	3.5	-
		V_{DD} = 3.6 V, T_A = 25 °C, TFBGA216 package, conforming to IEC61967-2 ART/L1-cache ON, over-drive ON, all peripheral clocks enabled, clock dithering enabled.	0.1 to 30 MHz	2	dBµV
			30 to 130 MHz	9	
			130 MHz to 1 GHz	14	
			1 GHz to 2 GHz	9	
			EMI Level	3	-

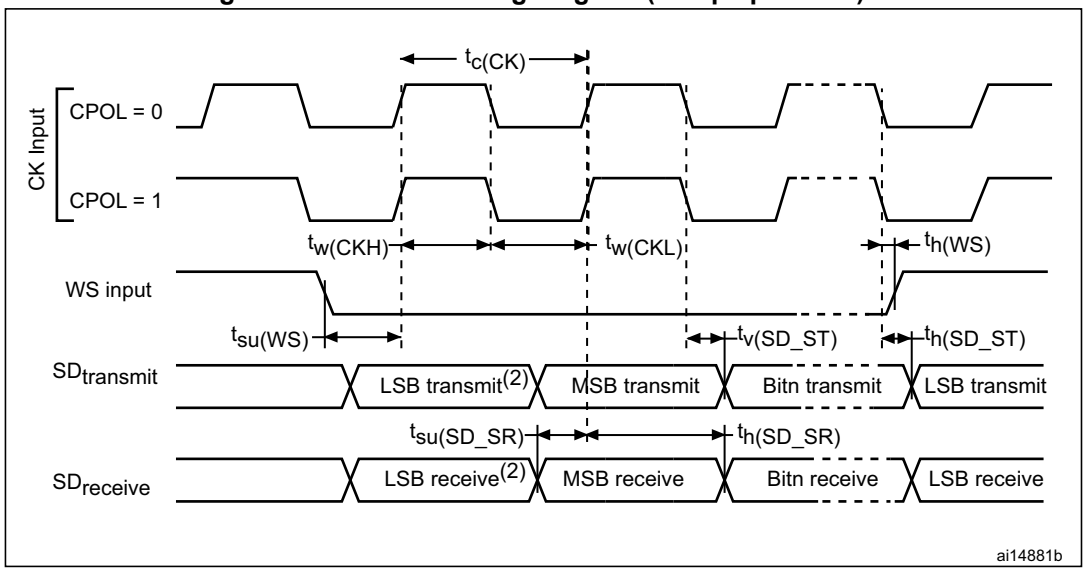
5.3.18 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

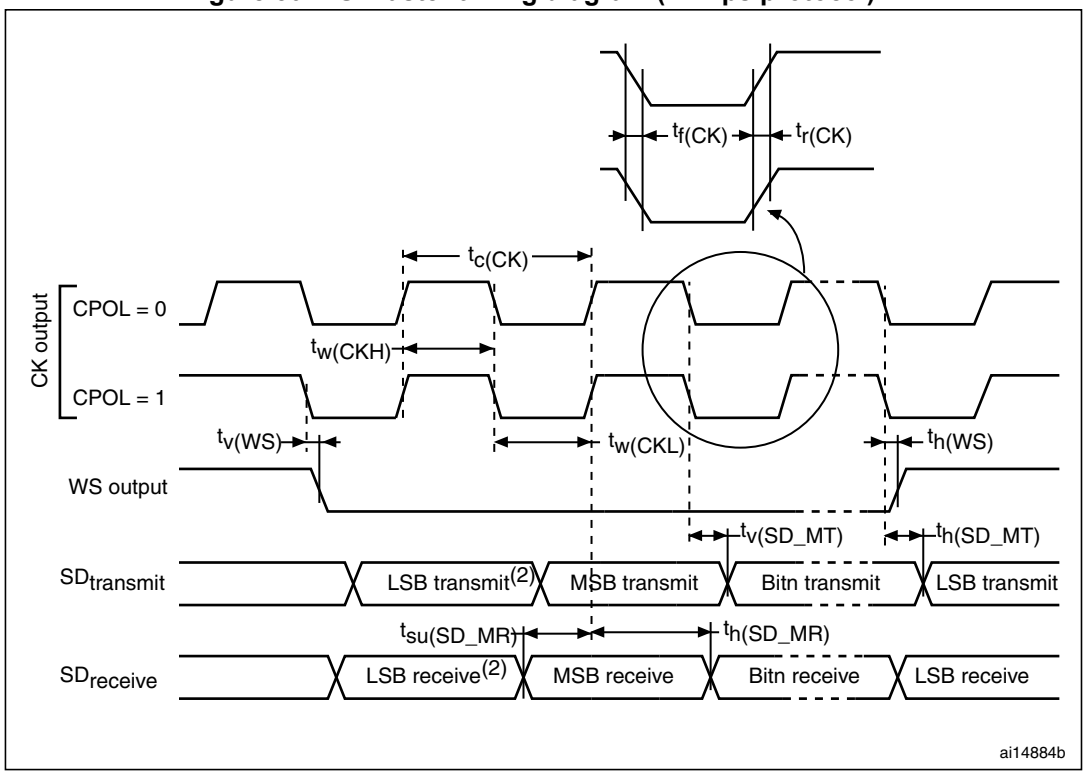
Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/ESDA/JEDEC JS-001-2012 and ANSI/ESD S5.3.1-2009 standards.

Figure 49. I²S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 50. I²S master timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

JATG/SWD characteristics

Unless otherwise specified, the parameters given in *Table 87* for JTAG/SWD are derived from tests performed under the ambient temperature, f_{HCLK} frequency and VDD supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: $0.5V_{DD}$

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 87. Dynamics characteristics: JTAG characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	TCK clock frequency	2.7V <VDD< 3.6V	-	-	40	MHz
$1/t_{c(TCK)}$		1.71 <VDD< 3.6V	-	-	35	
$t_{w(TCKH)}$	SCK high and low time	-	T_{PCLK} − 1	T_{PCLK}	T_{PCLK} + 1	ns
$t_{w(TCKL)}$						
$t_{su(TMS)}$	TMS input setup time	-	3	-	-	
$t_{h(TMS)}$	TMS input hold time	-	0	-	-	
$t_{su(TDI)}$	TDI input setup time	-	0.5	-	-	
$t_{h(TDI)}$	TDI input hold time	-	2	-	-	
$t_{ov\ (TDO)}$	TDO output valid time	2.7V <VDD< 3.6V	-	9	11	
		1.71 <VDD< 3.6V	-	9	13	
$t_{oh(TDO)}$	TDO output hold time	-	7.5	-	-	

Figure 56. ULPI timing diagram

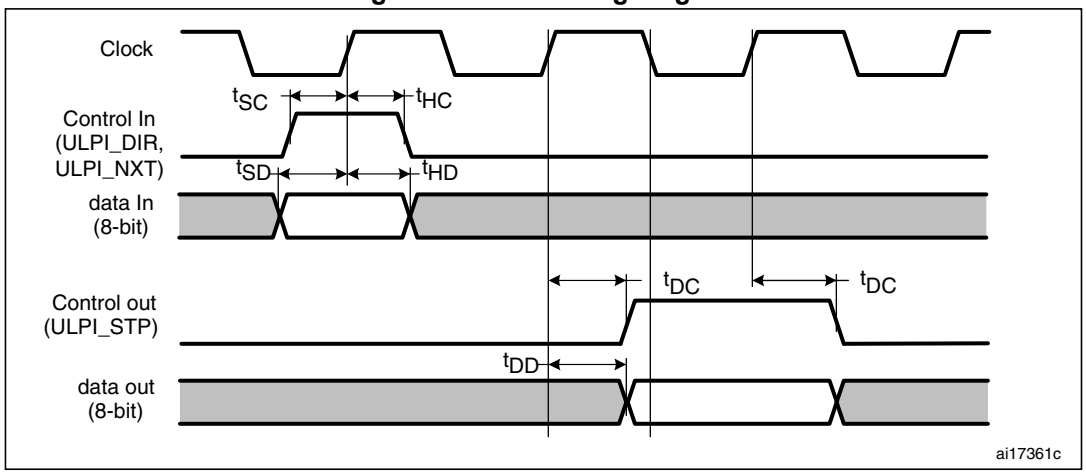


Table 95. Dynamic characteristics: USB ULPI(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{SC}	Control in (ULPI_DIR, ULPI_NXT) setup time	-	2	-	-	ns
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	-	1.5	-	-	
t_{SD}	Data in setup time	-	2	-	-	
t_{HD}	Data in hold time	-	1	-	-	
t_{DC}/t_{DD}	Data/control output delay	2.7 V < V_{DD} < 3.6 V, C_L = 20 pF	-	6.5	8	
		-	-	6.5	11	
		1.7 V < V_{DD} < 3.6 V, C_L = 15 pF	-			

1. Guaranteed by characterization results.

Ethernet characteristics

Unless otherwise specified, the parameters given in *Table 96*, *Table 97* and *Table 98* for SMI, RMII and MII are derived from tests performed under the ambient temperature, f_{HCLK} frequency summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output characteristics.

Table 96 gives the list of Ethernet MAC signals for the SMI (station management interface) and *Figure 57* shows the corresponding timing diagram.

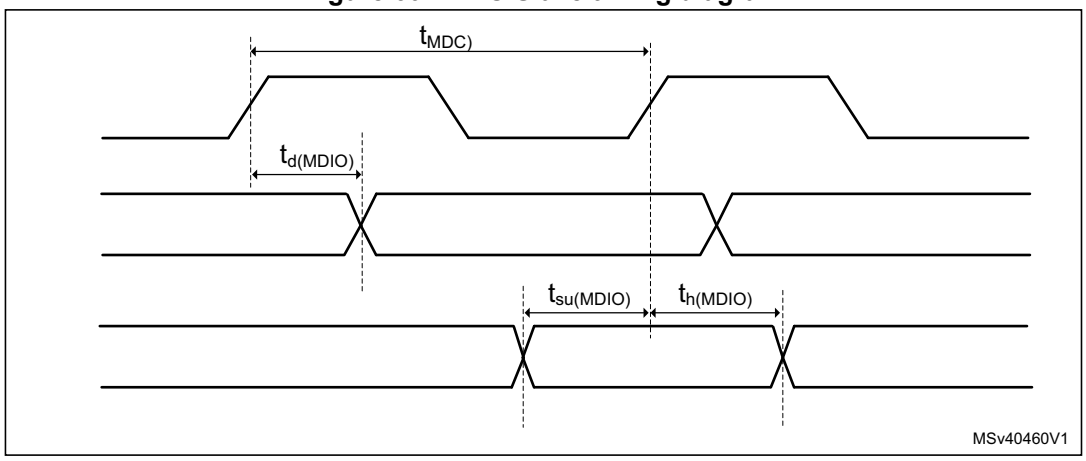
1. Guaranteed by characterization results.

Table 99. MDIO Slave timing parameters

Symbol	Parameter	Min	Typ	Max	Unit
F_{sDC}	Management Data clock	-	-	40	MHz
$t_{d(MDIO)}$	Management Data input/output **output valid time**	7	8	20	ns
$t_{su(MDIO)}$	Management Data input/output **setup time**	4	-	-	
$t_{h(MDIO)}$	Management Data input/output **hold time**	1	-	-	

The MDIO controller is mapped on APB2 domain. The frequency of the APB bus should at least 1.5 times the MDC frequency: $F_{PCLK2} \geq 1.5 * F_{MDC}$

Figure 60. MDIO Slave timing diagram



CAN (controller area network) interface

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (CANx_TX and CANx_RX).

5.3.30 FMC characteristics

Unless otherwise specified, the parameters given in *Table 100* to *Table 113* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Table 108. Synchronous multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}$ – 0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH\_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	T_{HCLK} + 0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	T_{HCLK} – 0.5	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	1.5	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	3.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. Guaranteed by characterization results.

Table 117. LPSDR SDRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK} + 0.5$	ns
$t_{d(SDCLKL\_Data)}$	Data output valid time	-	2.5	
$t_{h(SDCLKL\_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	2.5	
$t_{d(SDCLKL-SDNWE)}$	SDNWE valid time	-	2.5	
$t_{h(SDCLKL-SDNWE)}$	SDNWE hold time	0	-	
$t_{d(SDCLKL-SDNE)}$	Chip select valid time	-	0.5	
$t_{h(SDCLKL-SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL-SDNRAS)}$	SDNRAS valid time	-	1.5	
$t_{h(SDCLKL-SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

5.3.31 Quad-SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 118* and *Table 119* for Quad-SPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in *Table 17: General operating conditions*, with the following configuration:

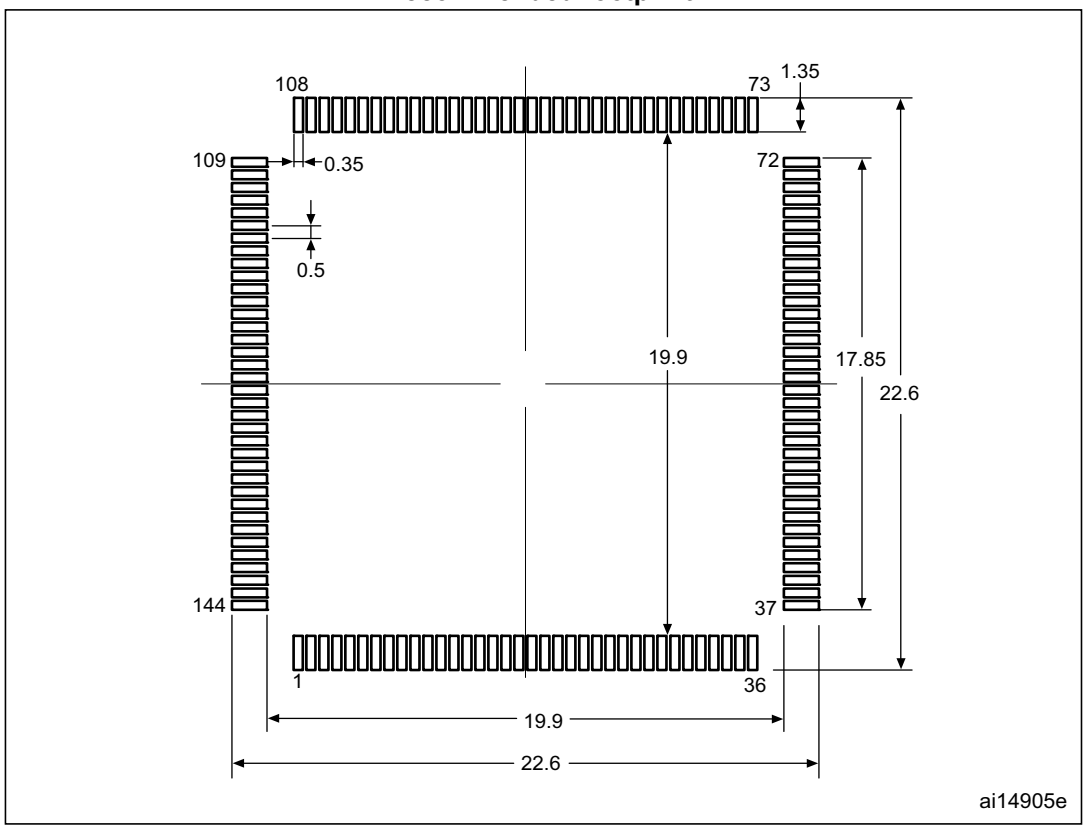
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 118. Quad-SPI characteristics in SDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Fck1/t(CK)	Quad-SPI clock frequency	2.7 V≤ V_{DD}<3.6 V CL=20 pF	-	-	108	MHz
		1.71 V<V_{DD}<3.6 V CL=15 pF	-	-	100	

Figure 87. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package recommended footprint



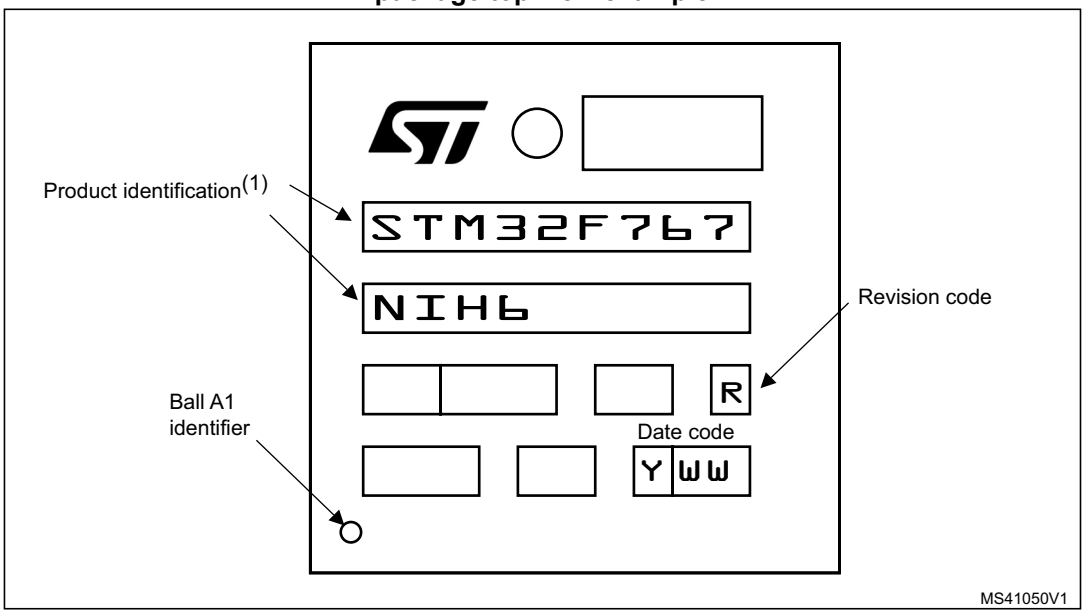
1. Dimensions are expressed in millimeters.

TFBGA216 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 103. TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.