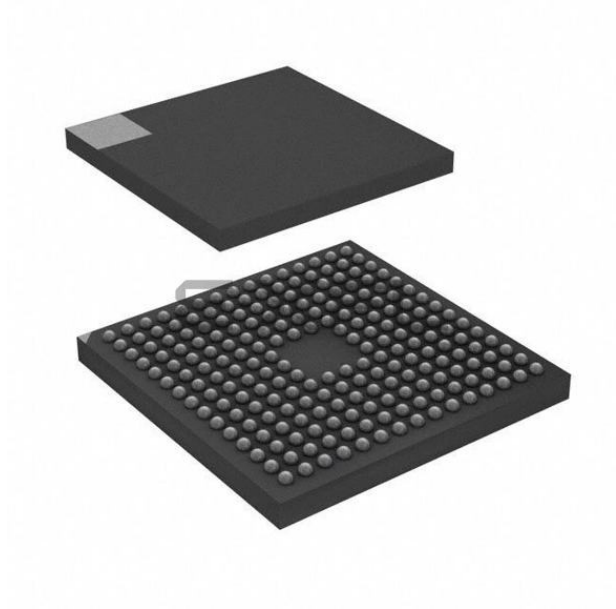

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

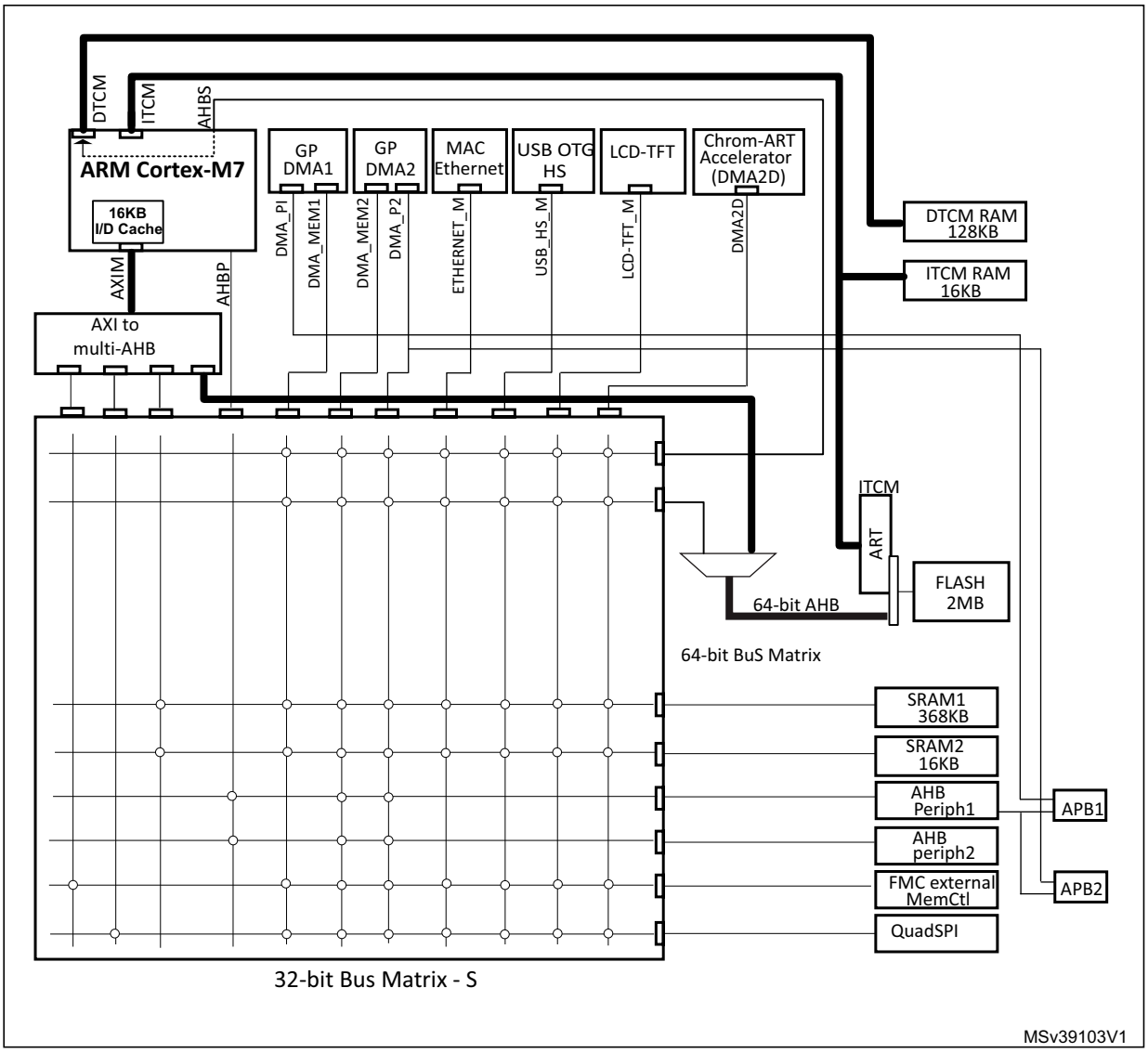
| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M7 |
| Core Size | 32-Bit Single-Core |
| Speed | 216MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 168 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.7V ~ 3.6V |
| Data Converters | A/D 24x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 216-TFBGA |
| Supplier Device Package | 216-TFBGA (13x13) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f767nih7 |

## 2.6 AXI-AHB bus matrix

The STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx system architecture is based on 2 sub-systems:

- An AXI to multi AHB bridge converting AXI4 protocol to AHB-Lite protocol:
  - 3x AXI to 32-bit AHB bridges connected to AHB bus matrix
  - 1x AXI to 64-bit AHB bridge connected to the embedded Flash memory
- A multi-AHB Bus-Matrix
  - The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS, LCD-TFT, and DMA2D) and the slaves (Flash memory, RAM, FMC, Quad-SPI, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

**Figure 3. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx AXI-AHB bus matrix architecture(1)**




1. The above figure has large wires for 64-bits bus and thin wires for 32-bits bus.

## 2.33 Controller area network (bxCAN)

The three CANs are compliant with the 2.0A and B (active) specifications with a bit rate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated for CAN1 and CAN2. 512 bytes of SRAM are dedicated for CAN3.

## 2.34 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 1.28 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 1 bidirectional control endpoint + 5 IN endpoints + 5 OUT endpoints
- 12 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Battery Charging Specification Revision 1.2 support
- Internal FS OTG PHY support
- HNP/SNP/IP inside (no need for any external resistor)

For the OTG/Host modes, a power switch is needed in case bus-powered devices are connected

## 2.35 Universal serial bus on-the-go high-speed (OTG_HS)

The devices embed a USB OTG high-speed (up to 480 Mbit/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 Mbit/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 Mbit/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 4 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 8 bidirectional endpoints
- 16 host channels with periodic OUT support

## 2.44 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- Two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Input voltage reference $V_{REF+}$

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

## 2.45 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

## 2.46 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F76xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

**Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)**

| Pin Number | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32F765xx STM32F767xx | | | | | | STM32F768Ax STM32F769xx | | | | | | | | | |
| LQFP100 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | WLCSP180[1] | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| 40 | 63 | R9 | 73 | 84 | R9 | J6 | 73 | 84 | R9 | PE10 | I/O | FT | - | TIM1_CH2N, DFSDM1_DATIN4, UART7_CTS, QUADSPI_BK2_IO3, FMC_D7, EVENTOUT | - |
| 41 | 64 | P10 | 74 | 85 | P10 | K6 | 74 | 85 | P10 | PE11 | I/O | FT | - | TIM1_CH2, SPI4_NSS, DFSDM1_CKIN4, SAI2_SD_B, FMC_D8, LCD_G3, EVENTOUT | - |
| 42 | 65 | R10 | 75 | 86 | R10 | L6 | 75 | 86 | R10 | PE12 | I/O | FT | - | TIM1_CH3N, SPI4_SCK, DFSDM1_DATIN5, SAI2_SCK_B, FMC_D9, LCD_B4, EVENTOUT | - |
| 43 | 66 | N11 | 76 | 87 | R12 | P6 | 76 | 87 | R12 | PE13 | I/O | FT | - | TIM1_CH3, SPI4_MISO, DFSDM1_CKIN5, SAI2_FS_B, FMC_D10, LCD_DE, EVENTOUT | - |
| 44 | 67 | P11 | 77 | 88 | P11 | N6 | 77 | 88 | P11 | PE14 | I/O | FT | - | TIM1_CH4, SPI4_MOSI, SAI2_MCLK_B, FMC_D11, LCD_CLK, EVENTOUT | - |
| 45 | 68 | R11 | 78 | 89 | R11 | M6 | 78 | 89 | R11 | PE15 | I/O | FT | - | TIM1_BKIN, FMC_D12, LCD_R7, EVENTOUT | - |
| 46 | 69 | R12 | 79 | 90 | P12 | K5 | 79 | 90 | P12 | PB10 | I/O | FT | - | TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, DFSDM1_DATIN7, USART3_TX, QUADSPI_BK1_NCS, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT | - |

**Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)**

| Pin Number | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32F765xx STM32F767xx | | | | | | STM32F768Ax STM32F769xx | | | | | | | | | |
| LQFP100 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | WLCSP180[1] | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| 47 | 70 | R13 | 80 | 91 | R13 | L5 | 80 | 91 | R13 | PB11 | I/O | FT | - | TIM2_CH4, I2C2_SDA, DFSDM1_CKIN7, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_RMII_TX_EN, DSI_TE, LCD_G5, EVENTOUT | - |
| 48 | 71 | M10 | 81 | 92 | L11 | P5 | 81 | 92 | L11 | VCAP_1 | S | - | - | - | - |
| 49 | - | - | - | 93 | K9 | N5 | - | 93 | K9 | VSS | S | - | - | - | - |
| 50 | 72 | N10 | 82 | 94 | L10 | P4 | 82 | 94 | L10 | VDD | S | - | - | - | - |
| - | - | - | - | 95 | M14 | NC | - | 95 | M14 | PJ5 | I/O | FT | - | LCD_R6, EVENTOUT | - |
| - | - | M11 | 83 | 96 | P13 | NC | 83 | 96 | P13 | PH6 | I/O | FT | - | I2C2_SMBA, SPI5_SCK, TIM12_CH1, ETH_MII_RXD2, FMC_SDNE1, DCMI_D8, EVENTOUT | - |
| - | - | N12 | 84 | 97 | N13 | NC | 84 | 97 | N13 | PH7 | I/O | FT | - | I2C3_SCL, SPI5_MISO, ETH_MII_RXD3, FMC_SDCKE1, DCMI_D9, EVENTOUT | - |
| - | - | M12 | 85 | 98 | P14 | M5 | - | 98 | P14 | PH8 | I/O | FT | - | I2C3_SDA, FMC_D16, DCMI_HSYNC, LCD_R2, EVENTOUT | - |
| - | - | M13 | 86 | 99 | N14 | K4 | - | 99 | N14 | PH9 | I/O | FT | - | I2C3_SMBA, TIM12_CH2, FMC_D17, DCMI_D0, LCD_R3, EVENTOUT | - |
| - | - | L13 | 87 | 100 | P15 | L4 | - | 100 | P15 | PH10 | I/O | FT | - | TIM5_CH1, I2C4_SMBA, FMC_D18, DCMI_D1, LCD_R4, EVENTOUT | - |
| - | - | L12 | 88 | 101 | N15 | M4 | - | 101 | N15 | PH11 | I/O | FT | - | TIM5_CH2, I2C4_SCL, FMC_D19, DCMI_D2, LCD_R5, EVENTOUT | - |

**Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)**

| Pin Number | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32F765xx STM32F767xx | | | | | | STM32F768Ax STM32F769xx | | | | | | | | | |
| LQFP100 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | WLCSP180[1] | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| - | 89 | K14 | 108 | 131 | N12 | G1 | 112 | 131 | N12 | PG4 | I/O | FT | - | FMC_A14/FMC_BA0, EVENTOUT | - |
| - | 90 | K13 | 109 | 132 | N11 | G2 | 113 | 132 | N11 | PG5 | I/O | FT | - | FMC_A15/FMC_BA1, EVENTOUT | - |
| - | 91 | J15 | 110 | 133 | J15 | G3 | 114 | 133 | J15 | PG6 | I/O | FT | - | FMC_NE3, DCMI_D12, LCD_R7, EVENTOUT | - |
| - | 92 | J14 | 111 | 134 | J14 | G4 | 115 | 134 | J14 | PG7 | I/O | FT | - | SAI1_MCLK_A, USART6_CK, FMC_INT, DCMI_D13, LCD_CLK, EVENTOUT | - |
| - | 93 | H14 | 112 | 135 | H14 | G5 | 116 | 135 | H14 | PG8 | I/O | FT | - | SPI6_NSS, SPDIF_RX2, USART6_RTS, ETH_PPS_OUT, FMC_SDCLK, LCD_G7, EVENTOUT | - |
| - | 94 | G12 | 113 | 136 | G10 | F1 | 117 | 136 | G10 | VSS | S | | - | - | - |
| - | 95 | H13 | 114 | 137 | G11 | F2 | 118 | 137 | G11 | VDDUSB | S | | - | - | - |
| 63 | 96 | H15 | 115 | 138 | H15 | G6 | 119 | 138 | H15 | PC6 | I/O | FT | - | TIM3_CH1, TIM8_CH1, I2S2_MCK, DFSDM1_CKIN3, USART6_TX, FMC_NWAIT, SDMMC2_D6, SDMMC1_D6, DCMI_D0, LCD_HSYNC, EVENTOUT | - |
| 64 | 97 | G15 | 116 | 139 | G15 | F3 | 120 | 139 | G15 | PC7 | I/O | FT | - | TIM3_CH2, TIM8_CH2, I2S3_MCK, DFSDM1_DATIN3, USART6_RX, FMC_NE1, SDMMC2_D7, SDMMC1_D7, DCMI_D1, LCD_G6, EVENTOUT | - |

**Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)**

| Pin Number | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32F765xx STM32F767xx | | | | | | STM32F768Ax STM32F769xx | | | | | | | | | |
| LQFP100 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | WLCSP180[1] | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| 81 | 114 | B12 | 142 | 164 | B12 | A4 | 142 | 164 | B12 | PD0 | I/O | FT | - | DFSDM1_CKIN6, DFSDM1_DATIN7, UART4_RX, CAN1_RX, FMC_D2, EVENTOUT | - |
| 82 | 115 | C12 | 143 | 165 | C12 | D5 | 143 | 165 | C12 | PD1 | I/O | FT | - | DFSDM1_DATIN6, DFSDM1_CKIN7, UART4_TX, CAN1_TX, FMC_D3, EVENTOUT | -- |
| 83 | 116 | D12 | 144 | 166 | D12 | D6 | 144 | 166 | D12 | PD2 | I/O | FT | - | TRACED2, TIM3_ETR, UART5_RX, SDMMC1_CMD, DCMI_D11, EVENTOUT | - |
| 84 | 117 | D11 | 145 | 167 | C11 | B5 | 145 | 167 | C11 | PD3 | I/O | FT | - | DFSDM1_CKOUT, SPI2_SCK/I2S2_CK, DFSDM1_DATIN0, USART2_CTS, FMC_CLK, DCMI_D5, LCD_G7, EVENTOUT | - |
| 85 | 118 | D10 | 146 | 168 | D11 | A5 | 146 | 168 | D11 | PD4 | I/O | FT | - | DFSDM1_CKIN0, USART2_RTS, FMC_NOE, EVENTOUT | - |
| 86 | 119 | C11 | 147 | 169 | C10 | C5 | 147 | 169 | C10 | PD5 | I/O | FT | - | USART2_TX, FMC_NWE, EVENTOUT | - |
| - | 120 | D8 | 148 | 170 | F8 | B6 | 148 | 170 | F8 | VSS | S | - | - | - | - |
| - | 121 | C8 | 149 | 171 | E9 | A6 | 149 | 171 | E9 | VDDSDMMC | S | - | - | - | - |
| 87 | 122 | B11 | 150 | 172 | B11 | E6 | 150 | 172 | B11 | PD6 | I/O | FT | - | DFSDM1_CKIN4, SPI3_MOSI/I2S3_SD, SAI1_SD_A, USART2_RX, DFSDM1_DATIN1, SDMMC2_CK, FMC_NWAIT, DCMI_D10, LCD_B2, EVENTOUT | - |

**Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)**

| Pin Number | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32F765xx STM32F767xx | | | | | | STM32F768Ax STM32F769xx | | | | | | | | | |
| LQFP100 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | WLCSP180[1] | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| 91 | 135 | A6 | 163 | 194 | A8 | A9 | 163 | 194 | A8 | PB5 | I/O | FT | - | UART5_RX, TIM3_CH2, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, SPI6_MOSI, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, FMC_SDCKE1, DCMI_D10, LCD_G7, EVENTOUT | - |
| 92 | 136 | B6 | 164 | 195 | B6 | B9 | 164 | 195 | B6 | PB6 | I/O | FT | - | UART5_TX, TIM4_CH1, HDMI_CEC, I2C1_SCL, DFSDM1_DATIN5, USART1_TX, CAN2_TX, QUADSPI_BK1_NCS, I2C4_SCL, FMC_SDNE1, DCMI_D5, EVENTOUT | - |
| 93 | 137 | B5 | 165 | 196 | B5 | C8 | 165 | 196 | B5 | PB7 | I/O | FT | - | TIM4_CH2, I2C1_SDA, DFSDM1_CKIN5, USART1_RX, I2C4_SDA, FMC_NL, DCMI_VSYNC, EVENTOUT | - |
| 94 | 138 | D6 | 166 | 197 | E6 | A10 | 166 | 197 | E6 | BOOT0 | I | B | - | - | VPP |
| 95 | 139 | A5 | 167 | 198 | A7 | E9 | 167 | 198 | A7 | PB8 | I/O | FT | - | I2C4_SCL, TIM4_CH3, TIM10_CH1, I2C1_SCL, DFSDM1_CKIN7, UART5_RX, CAN1_RX, SDMMC2_D4, ETH_MII_TXD3, SDMMC1_D4, DCMI_D6, LCD_B6, EVENTOUT | - |

**Table 12. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1/DFSDM1/CEC | I2C1/2/3/4/USART1/CEC | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF | CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD | SAI2/QUADSPI/SDMMC2/DFSDM1/OTG2_HS/OTG1_FS/LCD | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMMC1/MDIOS/OTG2_FS | DCMI/LCD/DSI | LCD | SYS |
| Port E | PE4 | TRACED1 | - | - | - | - | SPI4_NSS | SAI1_FS_A | - | - | - | DFSDM1_DATAIN3 | - | FMC_A20 | DCMI_D4 | LCD_B0 | EVENTOUT |
| | PE5 | TRACED2 | - | - | TIM9_CH1 | - | SPI4_MISO | SAI1_SCK_A | - | - | - | DFSDM1_CKIN3 | - | FMC_A21 | DCMI_D6 | LCD_G0 | EVENTOUT |
| | PE6 | TRACED3 | TIM1_BKIN2 | - | TIM9_CH2 | - | SPI4_MOSI | SAI1_SD_A | - | - | - | SAI2_MCK_B | - | FMC_A22 | DCMI_D7 | LCD_G1 | EVENTOUT |
| | PE7 | - | TIM1_ETR | - | - | - | - | DFSDM1_DATAIN2 | - | UART7_Rx | - | QUADSPI_BK2_IO0 | - | FMC_D4 | - | - | EVENTOUT |
| | PE8 | - | TIM1_CH1N | - | - | - | - | DFSDM1_CKIN2 | - | UART7_Tx | - | QUADSPI_BK2_IO1 | - | FMC_D5 | - | - | EVENTOUT |
| | PE9 | - | TIM1_CH1 | - | - | - | - | DFSDM1_CKOUT | - | UART7_RTS | - | QUADSPI_BK2_IO2 | - | FMC_D6 | - | - | EVENTOUT |
| | PE10 | - | TIM1_CH2N | - | - | - | - | DFSDM1_DATAIN4 | - | UART7_CTS | - | QUADSPI_BK2_IO3 | - | FMC_D7 | - | - | EVENTOUT |
| | PE11 | - | TIM1_CH2 | - | - | - | SPI4_NSS | DFSDM1_CKIN4 | - | - | - | SAI2_SD_B | - | FMC_D8 | - | LCD_G3 | EVENTOUT |
| | PE12 | - | TIM1_CH3N | - | - | - | SPI4_SCK | DFSDM1_DATAIN5 | - | - | - | SAI2_SCK_B | - | FMC_D9 | - | LCD_B4 | EVENTOUT |
| | PE13 | - | TIM1_CH3 | - | - | - | SPI4_MISO | DFSDM1_CKIN5 | - | - | - | SAI2_FS_B | - | FMC_D10 | - | LCD_DE | EVENTOUT |
| | PE14 | - | TIM1_CH4 | - | - | - | SPI4_MOSI | - | - | - | - | SAI2_MCK_B | - | FMC_D11 | - | LCD_CLK | EVENTOUT |
| | PE15 | - | TIM1_BKIN | - | - | - | - | - | - | - | - | - | - | FMC_D12 | - | LCD_R7 | EVENTOUT |

1. Guaranteed by design.
2. The reset temporization is measured from the power-on (POR reset or wakeup from $V_{BAT}$) to the instant when first instruction is read by the user application code.

### 5.3.6 Over-drive switching characteristics

When the over-drive mode switches from enabled to disabled or disabled to enabled, the system clock is stalled during the internal voltage set-up.

The over-drive switching characteristics are given in *Table 23*. They are subject to general operating conditions for $T_A$.

**Table 23. Over-drive switching characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Tod_swen | Over_drive switch enable time | HSI | - | 45 | - | µs |
| | | HSE max for 4 MHz and min for 26 MHz | 45 | - | 100 | |
| | | External HSE 50 MHz | - | 40 | - | |
| Tod_swdis | Over_drive switch disable time | HSI | - | 20 | - | |
| | | HSE max for 4 MHz and min for 26 MHz. | 20 | - | 80 | |
| | | External HSE 50 MHz | - | 15 | - | |

1. Guaranteed by design.

### 5.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 26: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

**Table 34. Typical and maximum current consumption in Sleep mode, regulator OFF**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | | Max(1) | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | TA= 25 °C | | TA= 85 °C | | TA= 105 °C | | |
| | | | | IDD12 | IDD | IDD12 | IDD | IDD12 | IDD | IDD12 | IDD | |
| IDD12/ IDD | Supply current in RUN mode from V12 and $V_{DD}$ supply | All Peripherals Enabled(2) | 180 | 102 | 1 | 114 | 2 | 148 | 2 | 168 | 2 | mA |
| | | | 168 | 91 | 1 | 101 | 2 | 132 | 2 | 152 | 2 | |
| | | | 144 | 71 | 1 | 78 | 2 | 105 | 2 | 122 | 2 | |
| | | | 60 | 32 | 1 | 37 | 2 | 64 | 2 | 81 | 2 | |
| | | | 25 | 16 | 1 | 20 | 2 | 46 | 2 | 64 | 2 | |
| | | All Peripherals Disabled | 180 | 13 | 1 | 18 | 2 | 53 | 2 | 73 | 2 | |
| | | | 168 | 12 | 1 | 16 | 2 | 47 | 2 | 67 | 2 | |
| | | | 144 | 9 | 1 | 13 | 2 | 39 | 2 | 56 | 2 | |
| | | | 60 | 5 | 1 | 9 | 2 | 35 | 2 | 52 | 2 | |
| | | | 25 | 3 | 1 | 7 | 2 | 33 | 2 | 50 | 2 | |

1. Guaranteed by characterization results, unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.

**Table 35. Typical and maximum current consumptions in Stop mode**

| Symbol | Parameter | Conditions | Typ | Max(1) | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ = 3.6 V | | | |
| | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD\_STOP\_NM}$ (normal mode) | Supply current in Stop mode, main regulator in Run mode | Flash memory in Stop mode, all oscillators OFF, no IWDG | 0.55 | 3 | 18 | 27 | mA |
| | | Flash memory in Deep power down mode, all oscillators OFF | 0.5 | 3 | 18 | 27 | |
| | Supply current in Stop mode, main regulator in Low-power mode | Flash memory in Stop mode, all oscillators OFF, no IWDG | 0.42 | 2.5 | 15 | 24 | |
| | | Flash memory in Deep power down mode, all oscillators OFF, no IWDG | 0.37 | 2.5 | 15 | 24 | |
| $I_{DD\_STOP\_UDM}$ (under-drive mode) | Supply current in Stop mode, main regulator in Low voltage and under-drive modes | Regulator in Run mode, Flash memory in Deep power down mode, all oscillators OFF, no IWDG | 0.18 | 1.2 | 6 | 10 | |
| | | Regulator in Low-power mode, Flash memory in Deep power down mode, all oscillators OFF, no IWDG | 0.13 | 1.1 | 6 | 10 | |

1. Data based on characterization, tested in production.

## 5.3.9 External clock source characteristics

### High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 65: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 28*.

The characteristics given in *Table 41* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 17*.

**Table 41. High-speed external user clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE\_ext}$ | External user clock source frequency(1) | - | 1 | - | 50 | MHz |
| $V_{HSEH}$ | OSC_IN input pin high level voltage | | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_{HSEL}$ | OSC_IN input pin low level voltage | | $V_{SS}$ | - | $0.3V_{DD}$ | |
| $t_{w(HSE)}$ $t_{w(HSE)}$ | OSC_IN high or low time(1) | | 5 | - | - | ns |
| $t_{r(HSE)}$ $t_{f(HSE)}$ | OSC_IN rise or fall time(1) | | - | - | 10 | |
| $C_{in(HSE)}$ | OSC_IN input capacitance(1) | - | - | 5 | - | pF |
| $DuCy_{(HSE)}$ | Duty cycle | - | 45 | - | 55 | % |
| $I_L$ | OSC_IN Input leakage current | $V_{SS} \le V_{IN} \le V_{DD}$ | - | - | ±1 | µA |

1. Guaranteed by design.

### Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 65: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 29*.

The characteristics given in *Table 42* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 17*.

### 5.3.11 PLL characteristics

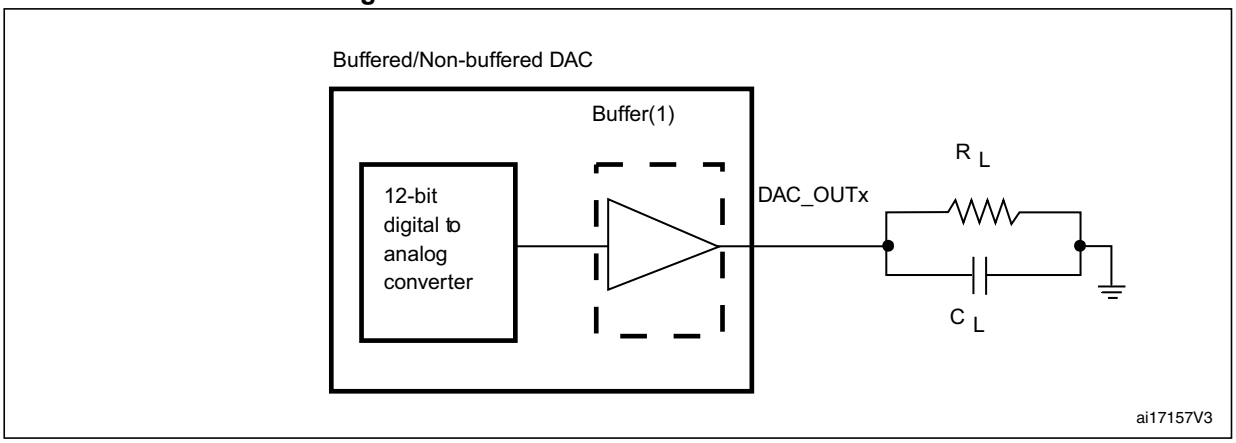
The parameters given in *Table 47* and *Table 48* are derived from tests performed under temperature and $V_{DD}$ supply voltage conditions summarized in *Table 17*.

**Table 47. Main PLL characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{PLL\_IN}$ | PLL input clock(1) | - | | 0.95(2) | 1 | 2.10 | MHz |
| $f_{PLL\_OUT}$ | PLL multiplier output clock | - | | 24 | - | 216 | |
| $f_{PLL48\_OUT}$ | 48 MHz PLL multiplier output clock | - | | - | 48 | 75 | |
| $f_{VCO\_OUT}$ | PLL VCO output | - | | 100 | - | 432 | |
| $t_{LOCK}$ | PLL lock time | VCO freq = 192 MHz | | 75 | - | 200 | µs |
| | | VCO freq = 432 MHz | | 100 | - | 300 | |
| Jitter(3) | Cycle-to-cycle jitter | System clock 216 MHz | RMS | - | 25 | - | ps |
| | | | peak to peak | - | ±150 | - | |
| | Period Jitter | | RMS | - | 15 | - | |
| | | | peak to peak | - | ±200 | - | |
| | Main clock output (MCO) for RMII Ethernet | Cycle to cycle at 50 MHz on 1000 samples | | - | 32 | - | |
| | Main clock output (MCO) for MII Ethernet | Cycle to cycle at 25 MHz on 1000 samples | | - | 40 | - | |
| | Bit Time CAN jitter | Cycle to cycle at 1 MHz on 1000 samples | | - | 330 | - | |
| $I_{DD(PLL)}$(4) | PLL power consumption on $V_{DD}$ | VCO freq = 192 MHz<br>VCO freq = 432 MHz | | 0.15<br>0.45 | - | 0.40<br>0.75 | mA |
| $I_{DDA(PLL)}$(4) | PLL power consumption on $V_{DDA}$ | VCO freq = 192 MHz<br>VCO freq = 432 MHz | | 0.30<br>0.55 | - | 0.40<br>0.85 | mA |

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design.
3. The use of 2 PLLs in parallel could degraded the Jitter up to +30%.
4. Guaranteed by characterization results.

**Figure 45. 12-bit buffered /non-buffered DAC**




1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

## 5.3.29 Communications interfaces

### I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.
- Fast-mode Plus (Fm+): with a bit rate up to 1Mbit/s.

The I²C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0410 reference manual) and when the I2CCLK frequency is greater than the minimum shown in the table below:

**Table 83. Minimum I2CCLK frequency in all I2C modes**

| Symbol | Parameter | Condition | | Min | Unit |
|---|---|---|---|---|---|
| f(I2CCLK) | I2CCLK frequency | Standard-mode | | 2 | MHz |
| | | Fast-mode | Analog filter ON DNF=0 | 8 | |
| | | | Analog filter OFF DNF=1 | 9 | |
| | | Fast-mode Plus | Analog filter ON DNF=0 | 16 | |
| | | | Analog filter OFF DNF=1 | 16 | |

**Table 117. LPSDR SDRAM write timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(SDCLK)}$ | FMC_SDCLK period | $2T_{HCLK} - 0.5$ | $2T_{HCLK} + 0.5$ | ns |
| $t_{d(SDCLKL\_Data)}$ | Data output valid time | - | 2.5 | |
| $t_{h(SDCLKL\_Data)}$ | Data output hold time | 0 | - | |
| $t_{d(SDCLKL\_Add)}$ | Address valid time | - | 2.5 | |
| $t_{d(SDCLKL-SDNWE)}$ | SDNWE valid time | - | 2.5 | |
| $t_{h(SDCLKL-SDNWE)}$ | SDNWE hold time | 0 | - | |
| $t_{d(SDCLKL-SDNE)}$ | Chip select valid time | - | 0.5 | |
| $t_{h(SDCLKL-SDNE)}$ | Chip select hold time | 0 | - | |
| $t_{d(SDCLKL-SDNRAS)}$ | SDNRAS valid time | - | 1.5 | |
| $t_{h(SDCLKL-SDNRAS)}$ | SDNRAS hold time | 0 | - | |
| $t_{d(SDCLKL-SDNCAS)}$ | SDNCAS valid time | - | 1.5 | |
| $t_{d(SDCLKL-SDNCAS)}$ | SDNCAS hold time | 0 | - | |

1. Guaranteed by characterization results.

## 5.3.31 Quad-SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 118* and *Table 119* for Quad-SPI are derived from tests performed under the ambient temperature, $f_{AHB}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 17: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics.

**Table 118. Quad-SPI characteristics in SDR mode(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Fck1/t(CK) | Quad-SPI clock frequency | 2.7 V≤ $V_{DD}$<3.6 V CL=20 pF | - | - | 108 | MHz |
| | | 1.71 V<$V_{DD}$<3.6 V CL=15 pF | - | - | 100 | |

### 5.3.34 Digital filter for Sigma-Delta Modulators (DFSDM) characteristics

Unless otherwise specified, the parameters given in *Table 122* for DFSDM are derived from tests performed under the ambient temperature, $f_{PCLK2}$ frequency and $V_{DD}$ supply voltage summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30pF
- Measurement points are done at CMOS levels: 0.5 x VDD

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (DFSDM1_CKINx, DFSDM1_DATINx, DFSDM1_CKOUT for DFSDM1).

**Table 122. DFSDM measured timing 1.71-3.6V**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{DFSDMCLK}$ | DFSDM clock | 1.71 < $V_{DD}$ < 3.6 V | - | - | $f_{SYSCLK}$ | MHz |
| $f_{CKIN}$ ($1/T_{CKIN}$) | Input clock frequency | SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < $V_{DD}$ < 3.6 V | - | - | 20 ($f_{DFSDMCLK}$/4) | |
| | | SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 2.7 < $V_{DD}$ < 3.6 V | - | - | 20 ($f_{DFSDMCLK}$/4) | |
| | | SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), 1.71 < $V_{DD}$ < 3.6 V | - | - | 20 ($f_{DFSDMCLK}$/4) | |
| | | SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), 2.7 < $V_{DD}$ < 3.6 V | - | - | 20 ($f_{DFSDMCLK}$/4) | |
| $f_{CKOUT}$ | Output clock frequency | 1.71 < $V_{DD}$ < 3.6 V | - | - | 20 | |
| $DuCy_{CKOUT}$ | Output clock frequency duty cycle | 1.71 < $V_{DD}$ < 3.6 V | 45 | 50 | 55 | % |

### 5.3.35 DFSDM timing diagrams

**Figure 80. Channel transceiver timing diagrams**

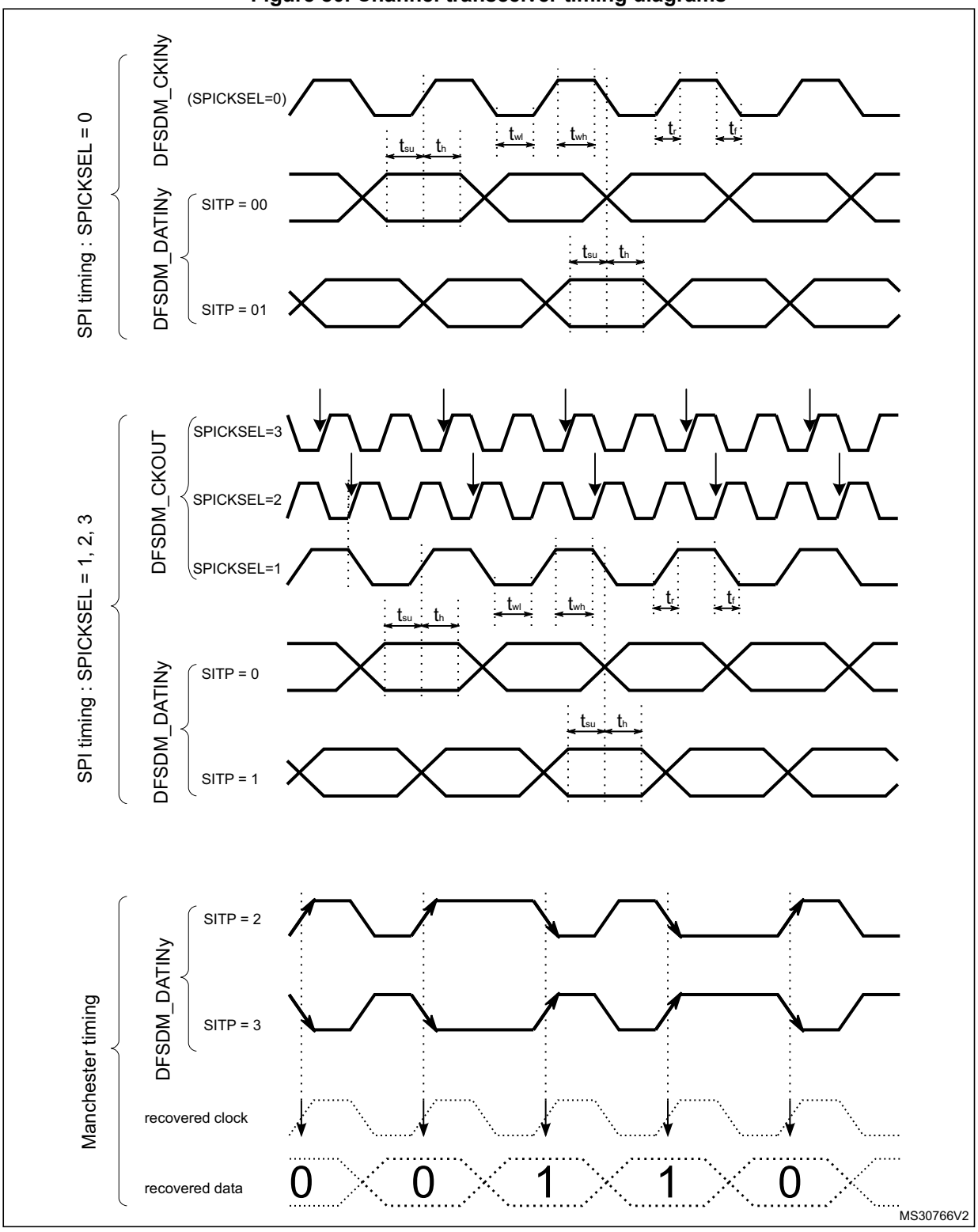
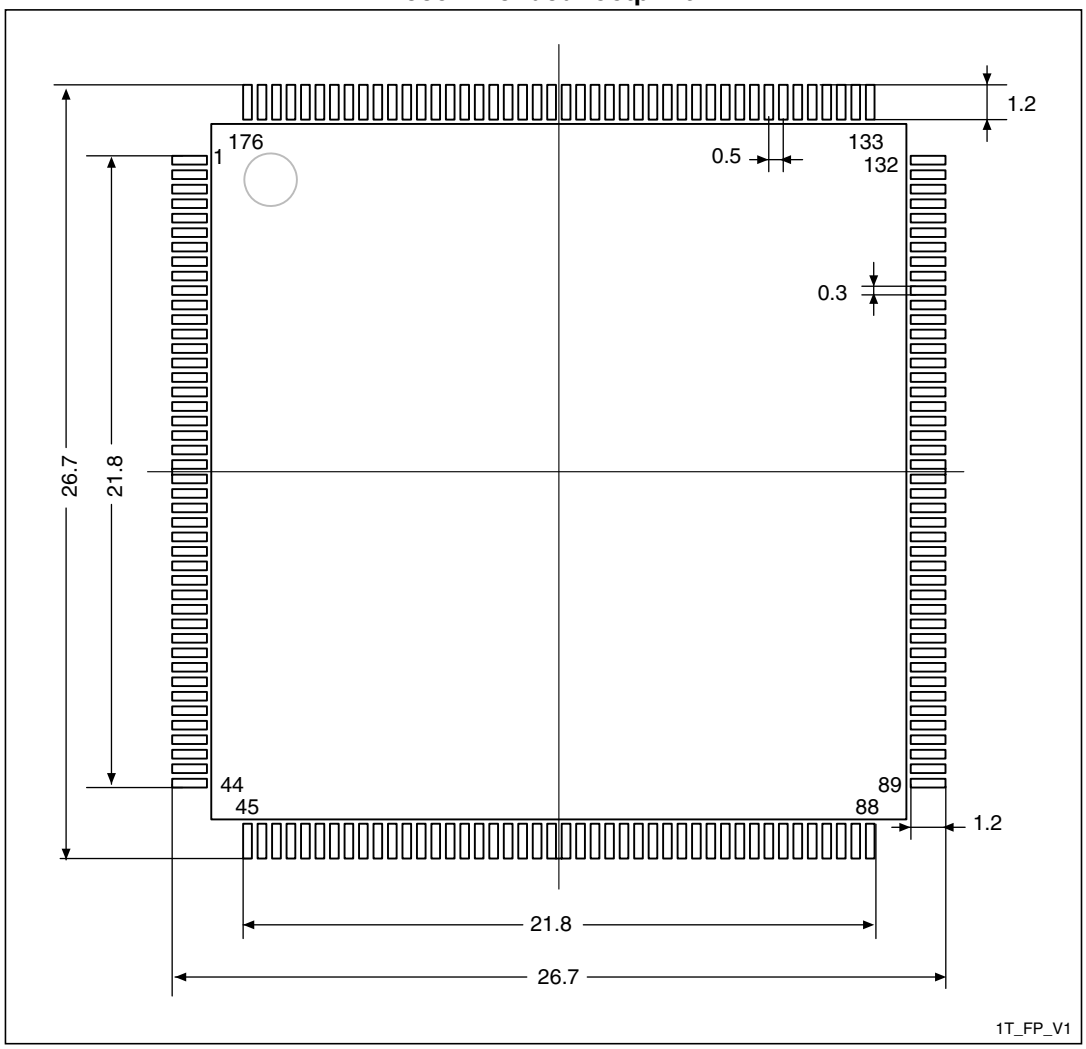


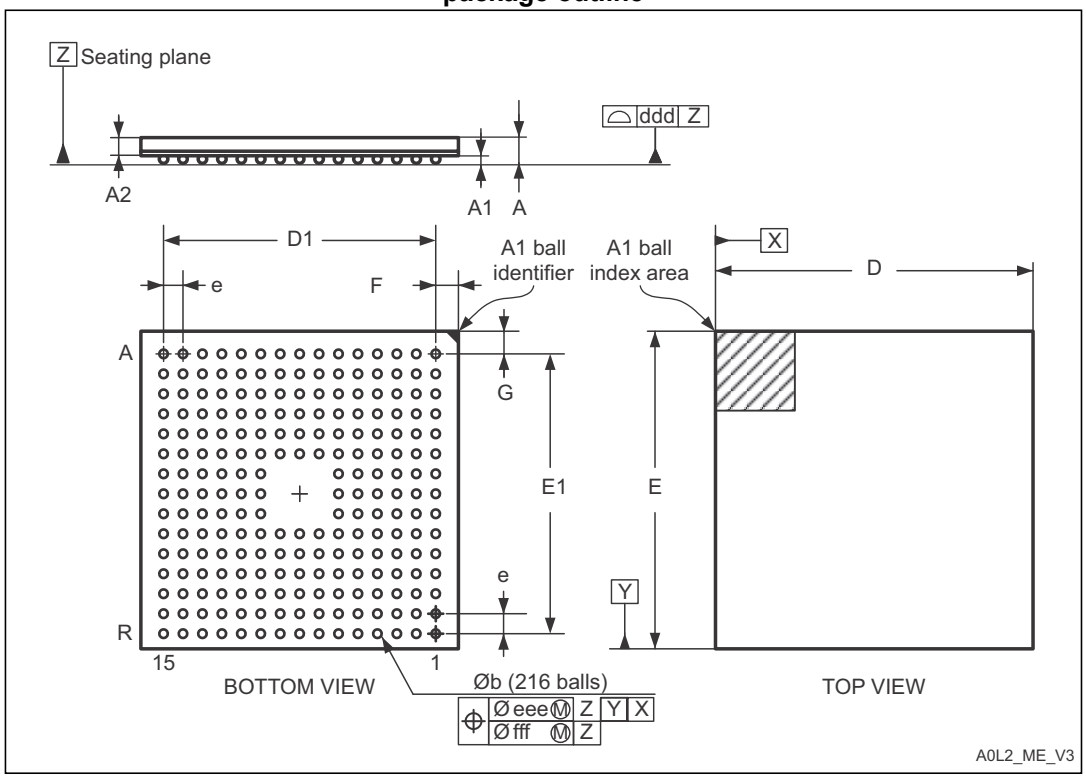
**Figure 90. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package recommended footprint**




1. Dimensions are expressed in millimeters.

## 6.7 TFBGA216, 13 x 13 x 0.8 mm thin fine-pitch ball grid array package information

**Figure 101. TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package outline**




1. Drawing is not to scale.

**Table 133. TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.100 | - | - | 0.0433 |
| A1 | 0.150 | - | - | 0.0059 | - | - |
| A2 | - | 0.760 | - | - | 0.0299 | - |
| b | 0.350 | 0.400 | 0.450 | 0.0138 | 0.0157 | 0.0177 |
| D | 12.850 | 13.000 | 13.150 | 0.5118 | 0.5118 | 0.5177 |
| D1 | - | 11.200 | - | - | 0.4409 | - |
| E | 12.850 | 13.000 | 13.150 | 0.5118 | 0.5118 | 0.5177 |
| E1 | - | 11.200 | - | - | 0.4409 | - |
| e | - | 0.800 | - | - | 0.0315 | - |
| F | - | 0.900 | - | - | 0.0354 | - |