E·XFL **STMicroelectronics - STM32F767VGT7 Datasheet**

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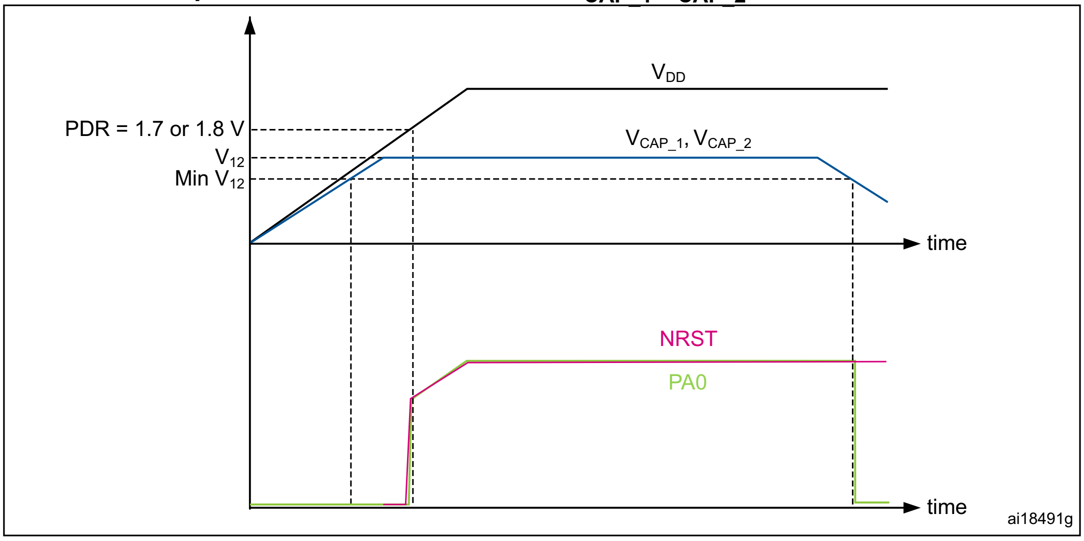
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

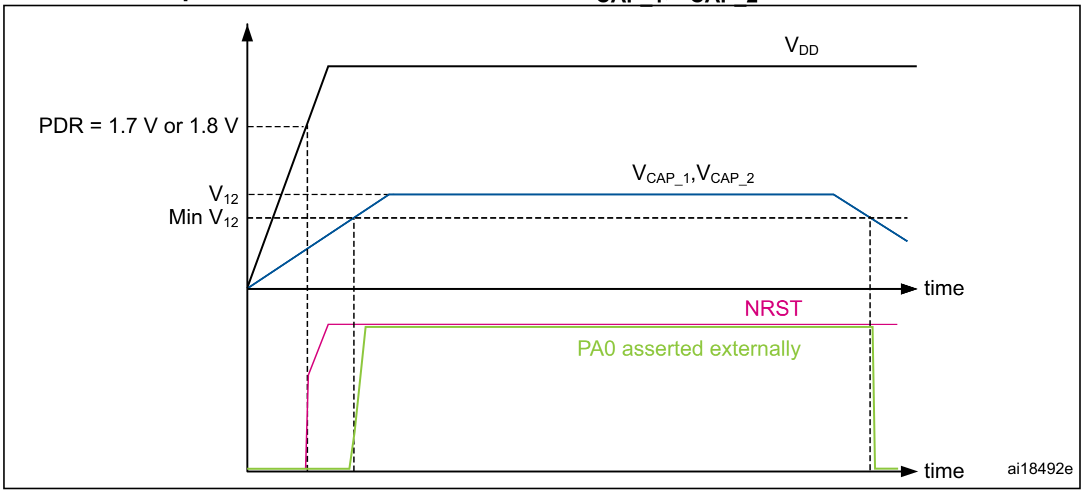
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f767vgt7

Figure 9. Startup in regulator OFF: slow V_{DD} slope - power-down reset risen after V_{CAP_1},V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

Figure 10. Startup in regulator OFF mode: fast V_{DD} slope - power-down reset risen before V_{CAP_1},V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

SAI1 and SAI2 can be served by the DMA controller

2.28 SPDIFRX Receiver Interface (SPDIFRX)

The SPDIFRX peripheral, is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC-61937. These standards support simple stereo streams up to high sample rate, and compressed multi-channel surround sound, such as those defined by Dolby or DTS (up to 5.1).

The main features of the SPDIFRX are the following:

- Up to 4 inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 kHz supported
- Supports Audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIFRX receiver provides all the necessary features to detect the symbol rate, and decode the incoming data stream. The user can select the wanted SPDIF input, and when a valid signal will be available, the SPDIFRX will re-sample the incoming signal, decode the manchester stream, recognize frames, sub-frames and blocks elements. It delivers to the CPU decoded data, and associated status flags.

The SPDIFRX also offers a signal named spdif_frame_sync, which toggles at the S/PDIF sub-frame rate that will be used to compute the exact sample rate for clock drift algorithms.

2.29 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I^2S and SAI applications. It allows to achieve error-free I^2S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I^2S/SAI sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I^2S/SAI flow with an external PLL (or Codec output).

2.30 Audio and LCD PLL (PLLSAI)

An additional PLL dedicated to audio and LCD-TFT is used for SAI1 peripheral in case the PLLI2S is programmed to achieve another audio sampling frequency (49.152 MHz or 11.2896 MHz) and the audio application requires both sampling frequencies simultaneously.

The PLLSAI is also used to generate the LCD-TFT clock.

2.44 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- Two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

2.45 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.46 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F76xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

- 16-bit RGB, configurations 1, 2, and 3
- 18-bit RGB, configurations 1 and 2
- 24-bit RGB

- Programmable polarity of all LTDC interface signals
- Extended resolutions beyond the DPI standard
- Maximum resolution of 800x480 pixels:
- Maximum resolution is limited by available DSI physical link bandwidth:
  - Number of lanes: 2
  - Maximum speed per lane: 500 Mbps1Gbps

Adapted interface features

Support for sending large amounts of data through the memory_write_start(WMS) and memory_write_continue(WMC) DCS commands

- LTDC interface color coding mappings into 24-bit interface:
  - 16-bit RGB, configurations 1, 2, and 3
  - 18-bit RGB, configurations 1 and 2
  - 24-bit RGB

Video mode pattern generator:

- Vertical and horizontal color bar generation without LTDC stimuli
- BER pattern without LTDC stimuli

Table 9. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TTa	3.3 V tolerant I/O directly connected to ADC
	B	Dedicated BOOT pin
	RST	Bidirectional reset pin with weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
1	1	A2	1	1	A3	E10	1	1	A3	PE2	I/O	FT	-	TRACECLK, SPI4_SCK, SAI1_MCLK_A, QUADSPI_BK1_IO2, ETH_MII_TXD3, FMC_A23, EVENTOUT	-
2	2	A1	2	2	A2	F10	2	2	A2	PE3	I/O	FT	-	TRACED0, SAI1_SD_B, FMC_A19, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
28	40	N4	50	53	N4	L9	50	53	N4	PA4	I/O	TTa	-	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, SPI6_NSS, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC1_IN4, ADC2_IN4, DAC_OUT1
29	41	P4	51	54	P4	P11	51	54	P4	PA5	I/O	TTa	-	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, SPI6_SCK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT	ADC1_IN5, ADC2_IN5, DAC_OUT2
30	42	P3	52	55	P3	N10	52	55	P3	PA6	I/O	FT	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, SPI6_MISO, TIM13_CH1, MDIOS_MDC, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC1_IN6, ADC2_IN6
31	43	R3	53	56	R3	M9	53	56	R3	PA7	I/O	FT	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, SPI6_MOSI, TIM14_CH1, ETH_MII_RX_DV/ETH_RMII_CRS_DV, FMC_SDNWE, EVENTOUT	ADC1_IN7, ADC2_IN7
32	44	N5	54	57	N5	NC	54	57	N5	PC4	I/O	FT	-	DFSDM1_CKIN2, I2S1_MCK, SPDIF_RX2, ETH_MII_RXD0/ETH_RMII_RXD0, FMC_SDNE0, EVENTOUT	ADC1_IN14, ADC2_IN14
33	45	P5	55	58	P5	NC	55	58	P5	PC5	I/O	FT	-	DFSDM1_DATIN2, SPDIF_RX3, ETH_MII_RXD1/ETH_RMII_RXD1, FMC_SDCKE0, EVENTOUT	ADC1_IN15, ADC2_IN15
-	-	-	-	59	L7	-	-	59	L7	VDD	S	-	-	-	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180(1)	LQFP176	LQFP208	TFBGA216						
-	51	M8	61	72	K7	P9	61	72	K7	VSS	S		-	-	-
-	52	N8	62	73	L8	M8	62	73	L8	VDD	S		-	-	-
-	53	N6	63	74	N6	L8	63	74	N6	PF13	I/O	FT	-	I2C4_SMBA, DFSDM1_DATIN6, FMC_A7, EVENTOUT	-
-	54	R7	64	75	P6	K8	64	75	P6	PF14	I/O	FT	-	I2C4_SCL, DFSDM1_CKIN6, FMC_A8, EVENTOUT	-
-	55	P7	65	76	M8	P8	65	76	M8	PF15	I/O	FT	-	I2C4_SDA, FMC_A9, EVENTOUT	-
-	56	N7	66	77	N7	N8	66	77	N7	PG0	I/O	FT	-	FMC_A10, EVENTOUT	-
-	57	M7	67	78	M7	L7	67	78	M7	PG1	I/O	FT	-	FMC_A11, EVENTOUT	-
37	58	R8	68	79	R8	M7	68	79	R8	PE7	I/O	FT	-	TIM1_ETR, DFSDM1_DATIN2, UART7_RX, QUADSPI_BK2_IO0, FMC_D4, EVENTOUT	-
38	59	P8	69	80	N9	N7	69	80	N9	PE8	I/O	FT	-	TIM1_CH1N, DFSDM1_CKIN2, UART7_TX, QUADSPI_BK2_IO1, FMC_D5, EVENTOUT	-
39	60	P9	70	81	P9	P7	70	81	P9	PE9	I/O	FT	-	TIM1_CH1, DFSDM1_CKOUT, UART7_RTS, QUADSPI_BK2_IO2, FMC_D6, EVENTOUT	-
-	61	M9	71	82	K8	-	71	82	K8	VSS	S	-	-	-	-
-	62	N9	72	83	L9	-	72	83	L9	VDD	S	-	-	-	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180(1)	LQFP176	LQFP208	TFBGA216						
96	140	B4	168	199	B4	D9	168	199	B4	PB9	I/O	FT	-	I2C4_SDA, TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, DFSDM1_DATIN7, UART5_TX, CAN1_TX, SDMMC2_D5, I2C4_SMBA, SDMMC1_D5, DCMI_D7, LCD_B7, EVENTOUT	-
97	141	A4	169	200	A6	C9	169	200	A6	PE0	I/O	FT	-	TIM4_ETR, LPTIM1_ETR, UART8_RX, SAI2_MCLK_A, FMC_NBL0, DCMI_D2, EVENTOUT	-
98	142	A3	170	201	A5	B10	170	201	A5	PE1	I/O	FT	-	LPTIM1_IN2, UART8_TX, FMC_NBL1, DCMI_D3, EVENTOUT	-
99	-	D5	-	202	F6	A11	-	202	F6	VSS	S	-	-	-	-
-	143	C6	171	203	E5	C10	171	203	E5	PDR_ON	S	-	-	-	-
100	144	C5	172	204	E7	B11	172	204	E7	VDD	S	-	-	-	-
-	-	D4	173	205	C3	D10	173	205	C3	PI4	I/O	FT	-	TIM8_BKIN, SAI2_MCLK_A, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	C4	174	206	D3	D11	174	206	D3	PI5	I/O	FT	-	TIM8_CH1, SAI2_SCK_A, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-
-	-	C3	175	207	D6	C11	175	207	D6	PI6	I/O	FT	-	TIM8_CH2, SAI2_SD_A, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	C2	176	208	D4	B12	176	208	D4	PI7	I/O	FT	-	TIM8_CH3, SAI2_FS_A, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-

Table 11. FMC pin definition

Pin name	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PF0	A0	-	-	A0
PF1	A1	-	-	A1
PF2	A2	-	-	A2
PF3	A3	-	-	A3
PF4	A4	-	-	A4
PF5	A5	-	-	A5
PF12	A6	-	-	A6
PF13	A7	-	-	A7
PF14	A8	-	-	A8
PF15	A9	-	-	A9
PG0	A10	-	-	A10
PG1	A11	-	-	A11
PG2	A12	-	-	A12
PG3	A13	-	-	-
PG4	A14	-	-	BA0
PG5	A15	-	-	BA1
PD11	A16	A16	CLE	-
PD12	A17	A17	ALE	-
PD13	A18	A18	-	-
PE3	A19	A19	-	-
PE4	A20	A20	-	-
PE5	A21	A21	-	-
PE6	A22	A22	-	-
PE2	A23	A23	-	-
PG13	A24	A24	-	-
PG14	A25	A25	-	-
PD14	D0	DA0	D0	D0
PD15	D1	DA1	D1	D1
PD0	D2	DA2	D2	D2
PD1	D3	DA3	D3	D3
PE7	D4	DA4	D4	D4
PE8	D5	DA5	D5	D5
PE9	D6	DA6	D6	D6
PE10	D7	DA7	D7	D7

Table 12. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM1/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port A	PA0	-	TIM2_CH1/TIM2_ETR	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS	UART4_TX	-	SAI2_SD_B	ETH_MII_CRS	-	-	-	EVENTOUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS	UART4_RX	QUADSPI_BK1_IO3	SAI2_MCK_B	ETH_MII_RX_CLK/ETH_RMII_REF_CLK	-	-	LCD_R2	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_TX	SAI2_SCK_B	-	-	ETH_MDIO	MDIOS_MDIO	-	LCD_R1	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	-	USART2_RX	-	LCD_B2	OTG_HS_ULPI_D0	ETH_MII_COL	-	-	LCD_B5	EVENTOUT
	PA4	-	-	-	-	-	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART2_CK	SPI6_NSS	-	-	-	OTG_HS_SOF	DCMI_HSYNC	LCD_VSYNC	EVENTOUT
	PA5	-	TIM2_CH1/TIM2_ETR	-	TIM8_CH1N	-	SPI1_SCK/I2S1_CK	-	-	SPI6_SCK	-	OTG_HS_ULPI_CK	-	-	-	LCD_R4	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	-	SPI6_MISO	TIM13_CH1	-	-	MDIOS_MDC	DCMI_PIXCLK	LCD_G2	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI/I2S1_SD	-	-	SPI6_MOSI	TIM14_CH1	-	ETH_MII_RX_DV/ETH_RMII_CRS_DV	FMC_SDNWE	-	-	EVENTOUT
	PA8	MCO1	TIM1_CH1	-	TIM8_BKIN2	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	CAN3_RX	UART7_RX	LCD_B3	LCD_R6	EVENTOUT
	PA9	-	TIM1_CH2	-	-	I2C3_SMBA	SPI2_SCK/I2S2_CK	-	USART1_TX	-	-	-	-	-	DCMI_D0	LCD_R5	EVENTOUT
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_RX	-	LCD_B4	OTG_FS_ID	-	MDIOS_MDIO	DCMI_D1	LCD_B1	EVENTOUT

Table 13. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx register boundary addresses(1)

Bus	Boundary address	Peripheral
	0xE00F FFFF - 0xFFFF FFFF	Reserved
Cortex-M7	0xE000 0000 - 0xE00F FFFF	Cortex-M7 internal peripherals
AHB3	0xD000 0000 - 0xDFFF FFFF	FMC bank 6
	0xC000 0000 - 0xCFFF FFFF	FMC bank 5
	0xA000 2000 - 0xBFFF FFFF	Reserved
	0xA000 1000 - 0xA000 1FFF	Quad-SPI control register
	0xA000 0000- 0xA000 0FFF	FMC control register
	0x9000 0000 - 0x9FFF FFFF	Quad-SPI
	0x8000 0000 - 0x8FFF FFFF	FMC bank 3
	0x7000 0000 - 0x7FFF FFFF	FMC bank 2
	0x6000 0000 - 0x6FFF FFFF	FMC bank 1
	0x5006 0C00- 0x5FFF FFFF	Reserved
AHB2	0x5006 0800 - 0x5006 0BFF	RNG
	0x5005 2000 - 0x5005 FFFF	Reserved
	0x5005 1000 - 0x5005 1FFF	JPEG codec
	0x5005 0000 - 0x5005 03FF	DCMI
	0x5004 0000- 0x5004 FFFF	Reserved
	0x5000 0000 - 0x5003 FFFF	USB OTG FS

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 39: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 38. Switching output I/O current consumption(1)

Symbol	Parameter	Conditions	I/O toggling frequency (fsw) MHz	Typ V_{DD} = 3.3 V	Typ V_{DD} = 1.8 V	Unit
I_{DDIO}	I/O switching Current	C_{EXT} = 0 pF $C = C_{INT} + C_S + C_{EXT}$	2	0.1	0.1	mA
			8	0.4	0.2	
			25	1.1	0.7	
			50	2.4	1.3	
			60	3.1	1.6	
			84	4.3	2.4	
			90	4.9	2.6	
			100	5.4	2.8	
		C_{EXT} = 10 pF $C = C_{INT} + C_S + C_{EXT}$	2	0.2	0.1	
			8	0.6	0.3	
			25	1.8	1.1	
			50	3.1	2.3	
			60	4.6	3.4	
			84	9.7	3.6	
			90	10.12	5.2	
			100	14.92	5.4	

Table 49. PLLISAI characteristics (continued)

<table>
<tr><th>Symbol</th><th>Parameter</th><th colspan="2">Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td rowspan="2">t_{LOCK}</td><td rowspan="2">PLLSAI lock time</td><td colspan="2">VCO freq = 192 MHz</td><td>75</td><td>-</td><td>200</td><td rowspan="2">µs</td></tr>
<tr><td colspan="2">VCO freq = 432 MHz</td><td>100</td><td>-</td><td>300</td></tr>
<tr><td rowspan="4">Jitter[3]</td><td rowspan="3">Master SAI clock jitter</td><td rowspan="2">Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5</td><td>RMS</td><td>-</td><td>90</td><td>-</td><td></td></tr>
<tr><td>peak to peak</td><td>-</td><td>±280</td><td>-</td><td>ps</td></tr>
<tr><td colspan="2">Average frequency of 12.288 MHz
N = 432, R = 5
on 1000 samples</td><td>-</td><td>90</td><td>-</td><td>ps</td></tr>
<tr><td>FS clock jitter</td><td colspan="2">Cycle to cycle at 48 KHz
on 1000 samples</td><td>-</td><td>400</td><td>-</td><td>ps</td></tr>
<tr><td>$I_{DD(PLLSAI)}$[4]</td><td>PLLSAI power consumption on V_{DD}</td><td colspan="2">VCO freq = 192 MHz
VCO freq = 432 MHz</td><td>0.15
0.45</td><td>-</td><td>0.40
0.75</td><td>mA</td></tr>
<tr><td>$I_{DDA(PLLSAI)}$[4]</td><td>PLLSAI power consumption on V_{DDA}</td><td colspan="2">VCO freq = 192 MHz
VCO freq = 432 MHz</td><td>0.30
0.55</td><td>-</td><td>0.40
0.85</td><td>mA</td></tr>
</table>

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

5.3.12 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see *Table 61: EMI characteristics*). It is available only on the main PLL.

Table 50. SSCG parameters constraint

Symbol	Parameter	Min	Typ	Max[1]	Unit
f_{Mod}	Modulation frequency	-	-	10	KHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP	-	-	-	$2^{15} - 1$	-

1. Guaranteed by design.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$\mathrm{MODEPER} = \mathrm{round}[f_{PLL\_IN} / (4 \times f_{Mod})]$$

f_{PLL_IN} and f_{Mod} must be expressed in Hz.

As an example:

Table 51. MIPI D-PHY characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Output low level voltage	-	1.1	1.2	1.2	V
$V_{IL-ULPS}$	Output high level voltage	-	-50	-	50	mV
V_{IH}	Output impedance of LP transmitter	-	110	-	-	Ω
V_{hys}	15%-85% rise and fall time	-	-	-	25	ns
LP Contention Detector Characteristics						
V_{ILCD}	Logic 0 contention threshold	-	-	-	200	mV
V_{IHCD}	Logic 0 contention threshold	-	450	-	-	mV

1. Guaranteed based on test during characterization.

Table 52. MIPI D-PHY AC characteristics LP mode and HS/LP transitions[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{LPX}	Transmitted length of any Low-Power state period	-	50	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	-	38	-	95	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Time that the transmitter drives the HS-0 state prior to starting the clock.	-	300	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	-	8	-	-	UI

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

5.3.17 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 60*. They are based on the EMS levels and classes defined in application note AN1709.

Table 60. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 216 MHz, conforms to IEC 61000-4-2	2B
V_{FTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A =+25 °C, f_{HCLK} = 168 MHz, conforms to IEC 61000-4-2	5A

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 61. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}] 8/200 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, TFBGA216 package, conforming to IEC61967-2 ART/L1-cache ON, over-drive ON, all peripheral clocks enabled, clock dithering disabled.	0.1 to 30 MHz	5	dBµV
			30 to 130 MHz	10	
			130 MHz to 1 GHz	18	
			1 GHz to 2 GHz	10	
			EMI Level	3.5	-
		V_{DD} = 3.6 V, T_A = 25 °C, TFBGA216 package, conforming to IEC61967-2 ART/L1-cache ON, over-drive ON, all peripheral clocks enabled, clock dithering enabled.	0.1 to 30 MHz	2	dBµV
			30 to 130 MHz	9	
			130 MHz to 1 GHz	14	
			1 GHz to 2 GHz	9	
			EMI Level	3	-

5.3.18 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/ESDA/JEDEC JS-001-2012 and ANSI/ESD S5.3.1-2009 standards.

Table 65. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
I_{lkg}	I/O input leakage current (4)		$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA
	I/O FT input leakage current (5)		$V_{IN} = 5$ V	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(6)	All pins except for PA10/PB12 (OTG_FS_ID,OTG_HS_ID)	$V_{IN} = V_{SS}$	30	40	50	kΩ
		PA10/PB12 (OTG_FS_ID,OTG_HS_ID)		7	10	14	
R_{PD}	Weak pull-down equivalent resistor(7)	All pins except for PA10/PB12 (OTG_FS_ID,OTG_HS_ID)	$V_{IN} = V_{DD}$	30	40	50	
		PA10/PB12 (OTG_FS_ID,OTG_HS_ID)		7	10	14	
C_{IO}(8)	I/O pin capacitance		-	-	5	-	pF

1. Guaranteed by design.
2. Tested in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 64: I/O current injection susceptibility*
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 64: I/O current injection susceptibility*
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 38*.

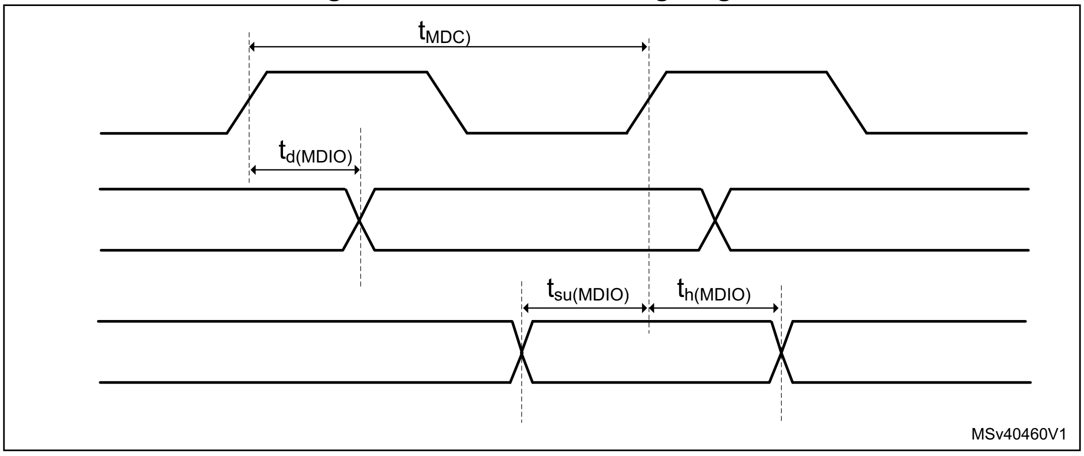
1. Guaranteed by characterization results.

Table 99. MDIO Slave timing parameters

Symbol	Parameter	Min	Typ	Max	Unit
F_{sDC}	Management Data clock	-	-	40	MHz
$t_{d(MDIO)}$	Management Data input/output **output valid time**	7	8	20	ns
$t_{su(MDIO)}$	Management Data input/output **setup time**	4	-	-	
$t_{h(MDIO)}$	Management Data input/output **hold time**	1	-	-	

The MDIO controller is mapped on APB2 domain. The frequency of the APB bus should at least 1.5 times the MDC frequency: $F_{PCLK2} \geq 1.5 * F_{MDC}$

Figure 60. MDIO Slave timing diagram



CAN (controller area network) interface

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (CANx_TX and CANx_RX).

5.3.30 FMC characteristics

Unless otherwise specified, the parameters given in *Table 100* to *Table 113* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Figure 67. Synchronous non-multiplexed NOR/PSRAM read timings

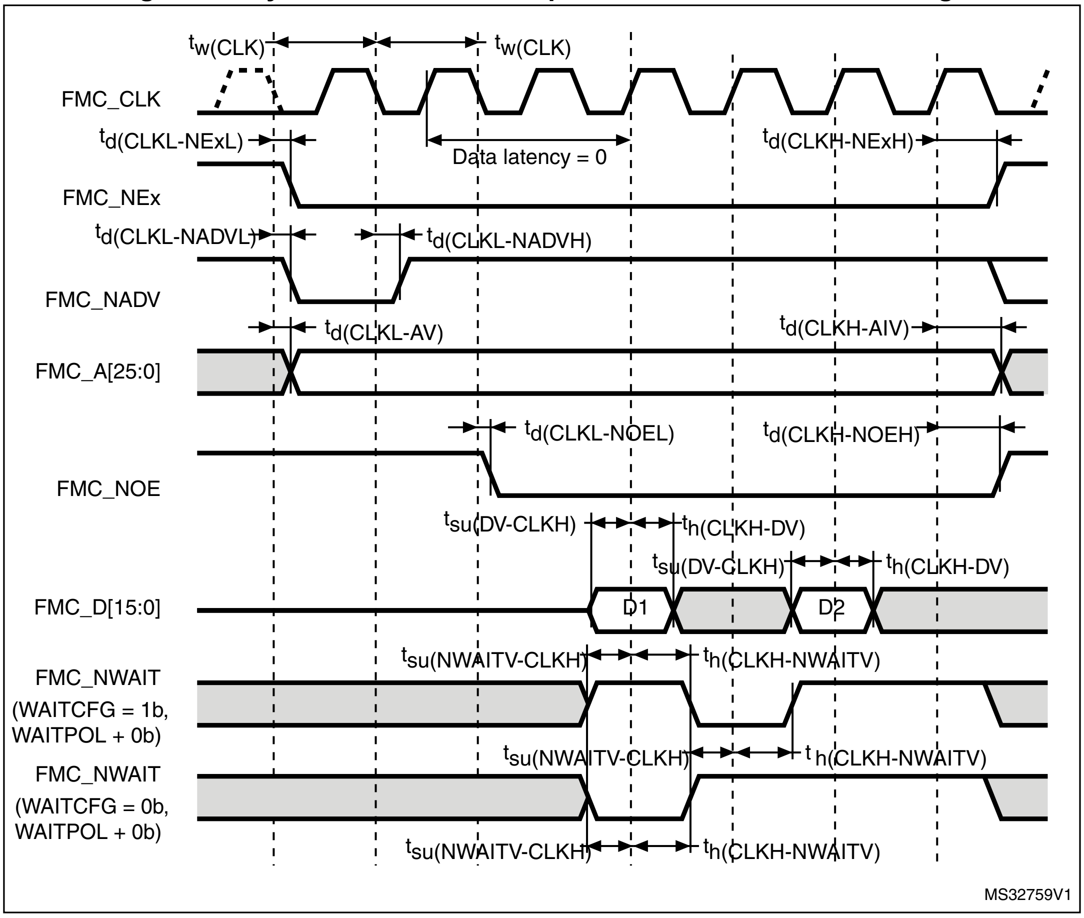


Table 110. Synchronous non-multiplexed NOR/PSRAM read timings(1)

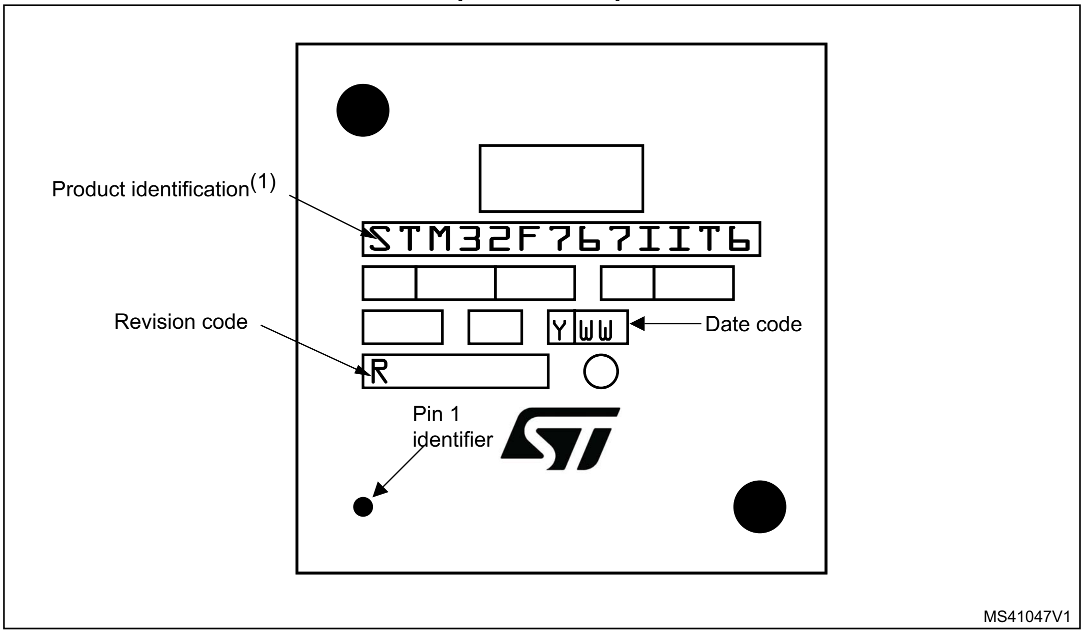
Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK} - 0.5$	-	ns
$t_{(CLKL\text{-}NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH\text{-}NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{HCLK} + 0.5$	-	
$t_{d(CLKL\text{-}NADVL)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL\text{-}NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL\text{-}AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2.5	
$t_{d(CLKH\text{-}AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL\text{-}NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH\text{-}NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{HCLK} + 0.5$	-	
$t_{su(DV\text{-}CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	1.5	-	
$t_{h(CLKH\text{-}DV)}$	FMC_D[15:0] valid data after FMC_CLK high	3.5	-	
$t_{(NWAIT\text{-}CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH\text{-}NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

LQFP176 device marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 91. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.