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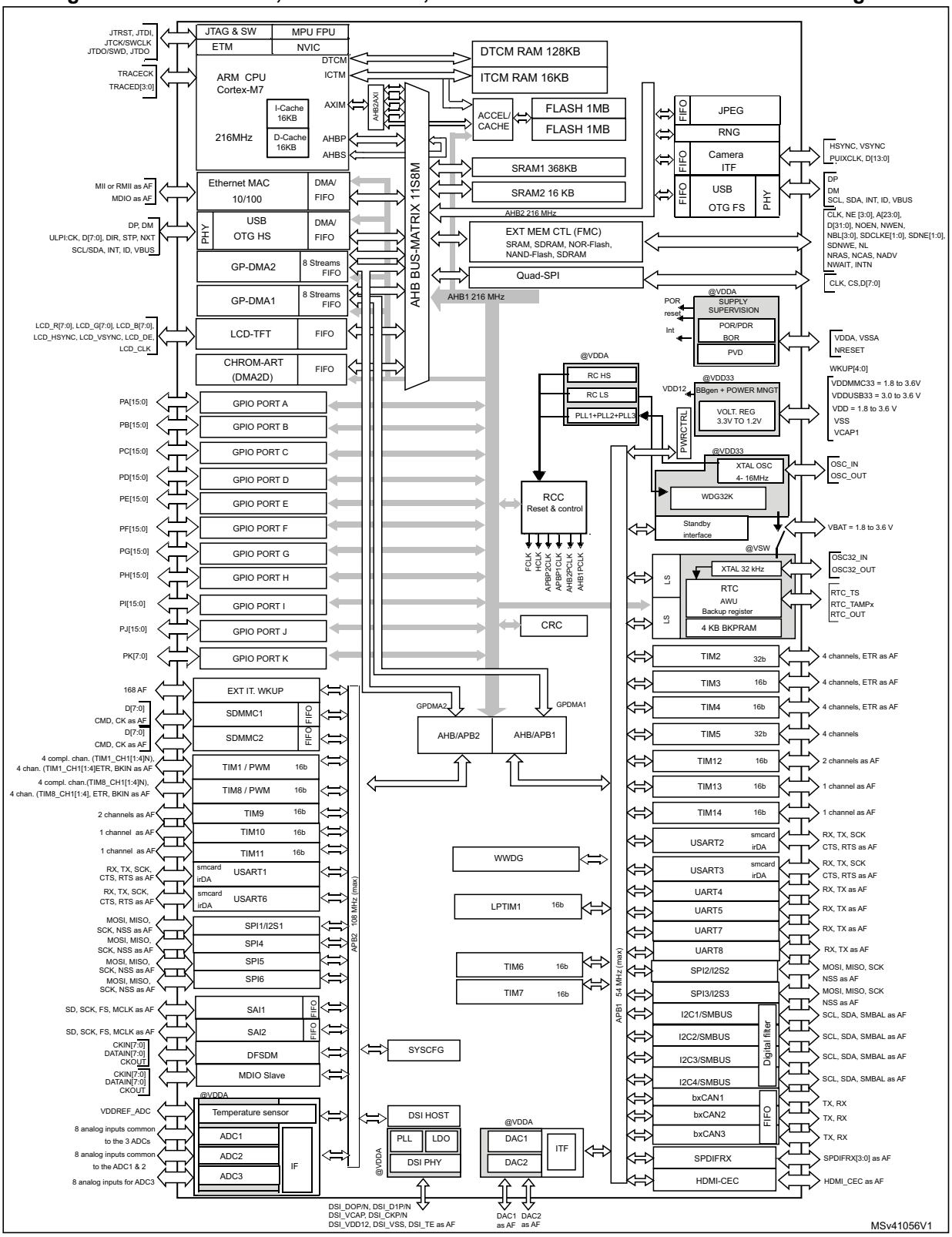
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

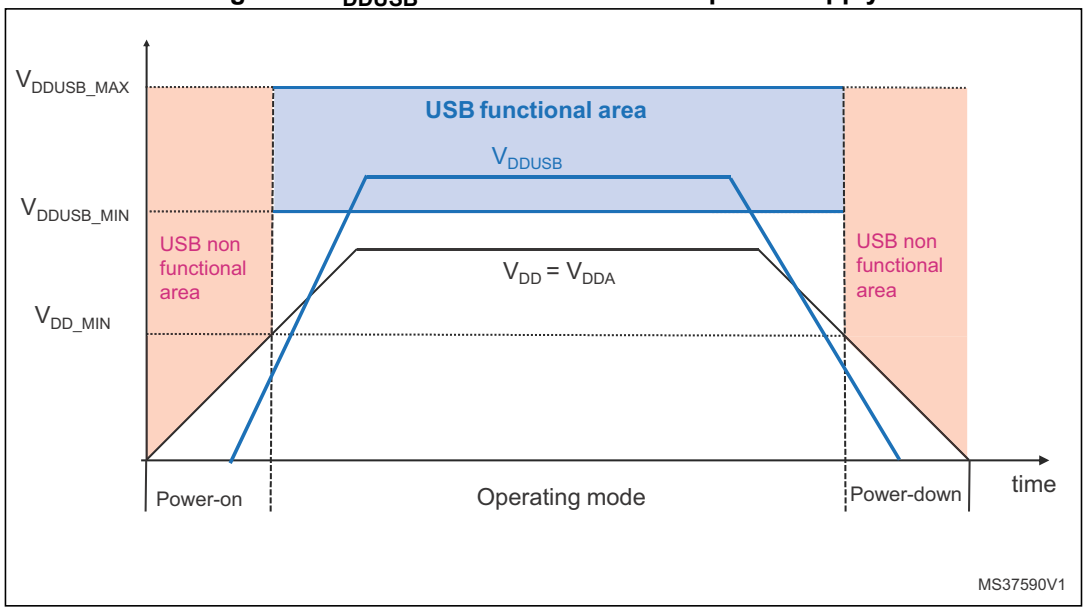
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	159
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f769bit6

Figure 2. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 216 MHz, while the timers connected to APB1 are clocked from TIMxCLK either up to 108 MHz or 216 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

Figure 5. V_{DDUSB} connected to external power supply



The DSI (Display Serial Interface) sub-system uses several power supply pins which are independent from the other supply pins:

- V_{DDDSI} is an independent DSI power supply dedicated for DSI Regulator and MIPI D-PHY. This supply must be connected to global V_{DD}.
- The V_{CAPDSI} pin is the output of DSI Regulator (1.2V) which must be connected externally to $V_{DD12DSI}$.
- The $V_{DD12DSI}$ pin is used to supply the MIPI D-PHY, and to supply the clock and data lanes pins. An external capacitor of 2.2 uF must be connected on the $V_{DD12DSI}$ pin.
- The V_{SSDSI} pin is an isolated supply ground used for DSI sub-system.
- If the DSI functionality is not used at all, then:
  - The V_{DDDSI} pin must be connected to global V_{DD}.
  - The V_{CAPDSI} pin must be connected externally to $V_{DD12DSI}$ but the external capacitor is no more needed.
  - The V_{SSDSI} pin must be grounded.

2.18 Power supply supervisor

2.18.1 Internal reset ON

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On the other packages, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR thresholds, or to disable BOR permanently. Three BOR thresholds are available through

2.23.4 Low-power timer (LPTIM1)

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one-shot mode
- Selectable software / hardware input trigger
- Selectable clock source:
- Internal clock source: LSE, LSI, HSI or APB clock
- External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

2.23.5 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

2.23.6 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

2.23.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.42 Digital filter for Sigma-Delta Modulators (DFSDM)

The devices embed one DFSDM with 4 digital filters modules and 8 external input serial channels (transceivers) or alternately 8 internal parallel inputs support. The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs). The DFSDM can also interface PDM (Pulse Density Modulation) microphones and perform PDM to PCM conversion and filtering in hardware. The DFSDM features optional parallel data stream inputs from microcontrollers memory (through DMA/CPU transfers into DFSDM). The DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators). The DFSDM digital filter modules perform digital processing according user selected filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripheral supports:

- 8 multiplexed input digital serial channels:
  - Configurable SPI interface to connect various SD modulator(s)
  - Configurable Manchester coded 1 wire interface support
  - PDM (Pulse Density Modulation) microphone input support
  - Maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
  - Clock output for SD modulator(s): 0..20 MHz
- Alternative inputs from 8 internal digital parallel channels (up to 16 bit input resolution):
  - internal sources: device memory data streams (DMA)
- 4 digital filter modules with adjustable digital signal processing:
  - Sincxfilter: filter order/type (1..5), oversampling ratio (up to 1..1024)
  - integrator: oversampling ratio (1..256)
- Up to 24-bit output data resolution, signed output data format
- Automatic data offset correction (offset stored in register by user)
- Continuous or single conversion
- Start-of-conversion triggered by:
  - Software trigger
  - Internal timers
  - External events
  - Start-of-conversion synchronously with first digital filter module (DFSDM0)
- Analog watchdog feature:
  - Low value and high value data threshold registers
  - Dedicated configurable Sincx digital filter (order = 1..3, oversampling ratio = 1..32)
  - Input from final output data or from selected input digital serial channels
  - Continuous monitoring independently from standard conversion
- Short circuit detector to detect saturated analog input values (bottom and top range):
  - Up to 8-bit counter to detect 1..256 consecutive 0's or 1's on serial data stream
  - Monitoring continuously each input serial channel
- Break signal generation on analog watchdog event or on short circuit detector event
- Extremes detector:
  - Storage of minimum and maximum values of final conversion data

  - 16-bit RGB, configurations 1, 2, and 3
  - 18-bit RGB, configurations 1 and 2
  - 24-bit RGB
- Programmable polarity of all LTDC interface signals
- Extended resolutions beyond the DPI standard
- Maximum resolution of 800x480 pixels:
- Maximum resolution is limited by available DSI physical link bandwidth:
  - Number of lanes: 2
  - Maximum speed per lane: 500 Mbps1Gbps

Adapted interface features

Support for sending large amounts of data through the memory_write_start(WMS) and memory_write_continue(WMC) DCS commands

- LTDC interface color coding mappings into 24-bit interface:
  - 16-bit RGB, configurations 1, 2, and 3
  - 18-bit RGB, configurations 1 and 2
  - 24-bit RGB

Video mode pattern generator:

- Vertical and horizontal color bar generation without LTDC stimuli
- BER pattern without LTDC stimuli

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
28	40	N4	50	53	N4	L9	50	53	N4	PA4	I/O	TT a	-	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, SPI6_NSS, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC1_IN4, ADC2_IN4, DAC_OUT1
29	41	P4	51	54	P4	P11	51	54	P4	PA5	I/O	TT a	-	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, SPI6_SCK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT	ADC1_IN5, ADC2_IN5, DAC_OUT2
30	42	P3	52	55	P3	N10	52	55	P3	PA6	I/O	FT	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, SPI6_MISO, TIM13_CH1, MDIOS_MDC, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC1_IN6, ADC2_IN6
31	43	R3	53	56	R3	M9	53	56	R3	PA7	I/O	FT	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, SPI6_MOSI, TIM14_CH1, ETH_MII_RX_DV/ETH_RMII_CRS_DV, FMC_SDNWE, EVENTOUT	ADC1_IN7, ADC2_IN7
32	44	N5	54	57	N5	NC	54	57	N5	PC4	I/O	FT	-	DFSDM1_CKIN2, I2S1_MCK, SPDIF_RX2, ETH_MII_RXD0/ETH_RMII_RXD0, FMC_SDNE0, EVENTOUT	ADC1_IN14, ADC2_IN14
33	45	P5	55	58	P5	NC	55	58	P5	PC5	I/O	FT	-	DFSDM1_DATIN2, SPDIF_RX3, ETH_MII_RXD1/ETH_RMII_RXD1, FMC_SDCKE0, EVENTOUT	ADC1_IN15, ADC2_IN15
-	-	-	-	59	L7	-	-	59	L7	VDD	S	-	-	-	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	-	K12	89	102	M15	P3	-	102	M15	PH12	I/O	FT	-	TIM5_CH3, I2C4_SDA, FMC_D20, DCMI_D3, LCD_R6, EVENTOUT	-
-	-	H12	90	-	K10	N4	-	-	K10	VSS	S		-	-	-
-	-	J12	91	103	K11	-	-	103	K11	VDD	S		-	-	-
51	73	P12	92	104	L13	H8	85	104	L13	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, DFSDM1_DATIN1, USART3_CK, UART5_RX, CAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_RMII_TXD0, OTG_HS_ID, EVENTOUT	-
52	74	P13	93	105	K14	J5	86	105	K14	PB13	I/O	FT	-	TIM1_CH1N, SPI2_SCK/I2S2_CK, DFSDM1_CKIN1, USART3_CTS, UART5_TX, CAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, EVENTOUT	OTG_HS_VBUS
53	75	R14	94	106	R14	N3	87	106	R14	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, USART1_TX, SPI2_MISO, DFSDM1_DATIN2, USART3_RTS, UART4_RTS, TIM12_CH1, SDMMC2_D0, OTG_HS_DM, EVENTOUT	-
54	76	R15	95	107	R15	N2	88	107	R15	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, USART1_RX, SPI2_MOSI/I2S2_SD, DFSDM1_CKIN2, UART4_CTS, TIM12_CH2, SDMMC2_D1, OTG_HS_DP, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	-	C13	134	157	C13	D3	134	157	C13	PI3	I/O	FT	-	TIM8_ETR, SPI2_MOSI/I2S2_SD, FMC_D27, DCMI_D10, EVENTOUT	-
-	-	D9	135	-	F9	-	135	-	F9	VSS	S	-	-	-	
-	-	C9	136	158	E10	-	136	158	E10	VDD	S	-	-	-	--
76	109	A14	137	159	A14	A3	137	159	A14	PA14(JTCK-SWCLK)	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
77	110	A13	138	160	A13	F8	138	160	A13	PA15(JTDI)	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, HDMI_CEC, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SPI6_NSS, UART4_RTS, CAN3_TX, UART7_TX, EVENTOUT	-
78	111	B14	139	161	B14	B4	139	161	B14	PC10	I/O	FT	-	DFSDM1_CKIN5, SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDMMC1_D2, DCMI_D8, LCD_R2, EVENTOUT	-
79	112	B13	140	162	B13	C4	140	162	B13	PC11	I/O	FT	-	DFSDM1_DATIN5, SPI3_MISO, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SDMMC1_D3, DCMI_D4, EVENTOUT	-
80	113	A12	141	163	A12	D4	141	163	A12	PC12	I/O	FT	-	TRACED3, SPI3_MOSI/I2S3_SD, USART3_CK, UART5_TX, SDMMC1_CK, DCMI_D9, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
96	140	B4	168	199	B4	D9	168	199	B4	PB9	I/O	FT	-	I2C4_SDA, TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, DFSDM1_DATIN7, UART5_TX, CAN1_TX, SDMMC2_D5, I2C4_SMBA, SDMMC1_D5, DCMI_D7, LCD_B7, EVENTOUT	-
97	141	A4	169	200	A6	C9	169	200	A6	PE0	I/O	FT	-	TIM4_ETR, LPTIM1_ETR, UART8_RX, SAI2_MCLK_A, FMC_NBL0, DCMI_D2, EVENTOUT	-
98	142	A3	170	201	A5	B10	170	201	A5	PE1	I/O	FT	-	LPTIM1_IN2, UART8_TX, FMC_NBL1, DCMI_D3, EVENTOUT	-
99	-	D5	-	202	F6	A11	-	202	F6	VSS	S	-	-	-	-
-	143	C6	171	203	E5	C10	171	203	E5	PDR_ON	S	-	-	-	-
100	144	C5	172	204	E7	B11	172	204	E7	VDD	S	-	-	-	-
-	-	D4	173	205	C3	D10	173	205	C3	PI4	I/O	FT	-	TIM8_BKIN, SAI2_MCLK_A, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	C4	174	206	D3	D11	174	206	D3	PI5	I/O	FT	-	TIM8_CH1, SAI2_SCK_A, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-
-	-	C3	175	207	D6	C11	175	207	D6	PI6	I/O	FT	-	TIM8_CH2, SAI2_SD_A, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	C2	176	208	D4	B12	176	208	D4	PI7	I/O	FT	-	TIM8_CH3, SAI2_FS_A, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	-	F6	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	F7	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	F8	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	F9	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	F10	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	G6	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	G7	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	G8	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	G9	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	G10	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	H6	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	H7	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	H8	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	H9	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	H10	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	J6	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	J7	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	J8	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	J9	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	J10	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	K6	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	K7	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	K8	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	K9	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	K10	-	-	-	-	-	-	-	VSS	S	-	-	-	-

Table 12. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM1/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port E	PE4	TRACED1	-	-	-	-	SPI4_NSS	SAI1_FS_A	-	-	-	DFSDM1_DATAIN3	-	FMC_A20	DCMI_D4	LCD_B0	EVENTOUT
	PE5	TRACED2	-	-	TIM9_CH1	-	SPI4_MISO	SAI1_SCK_A	-	-	-	DFSDM1_CKIN3	-	FMC_A21	DCMI_D6	LCD_G0	EVENTOUT
	PE6	TRACED3	TIM1_BKIN2	-	TIM9_CH2	-	SPI4_MOSI	SAI1_SD_A	-	-	-	SAI2_MCK_B	-	FMC_A22	DCMI_D7	LCD_G1	EVENTOUT
	PE7	-	TIM1_ETR	-	-	-	-	DFSDM1_DATAIN2	-	UART7_Rx	-	QUADSPI_BK2_IO0	-	FMC_D4	-	-	EVENTOUT
	PE8	-	TIM1_CH1N	-	-	-	-	DFSDM1_CKIN2	-	UART7_Tx	-	QUADSPI_BK2_IO1	-	FMC_D5	-	-	EVENTOUT
	PE9	-	TIM1_CH1	-	-	-	-	DFSDM1_CKOUT	-	UART7_RTS	-	QUADSPI_BK2_IO2	-	FMC_D6	-	-	EVENTOUT
	PE10	-	TIM1_CH2N	-	-	-	-	DFSDM1_DATAIN4	-	UART7_CTS	-	QUADSPI_BK2_IO3	-	FMC_D7	-	-	EVENTOUT
	PE11	-	TIM1_CH2	-	-	-	SPI4_NSS	DFSDM1_CKIN4	-	-	-	SAI2_SD_B	-	FMC_D8	-	LCD_G3	EVENTOUT
	PE12	-	TIM1_CH3N	-	-	-	SPI4_SCK	DFSDM1_DATAIN5	-	-	-	SAI2_SCK_B	-	FMC_D9	-	LCD_B4	EVENTOUT
	PE13	-	TIM1_CH3	-	-	-	SPI4_MISO	DFSDM1_CKIN5	-	-	-	SAI2_FS_B	-	FMC_D10	-	LCD_DE	EVENTOUT
	PE14	-	TIM1_CH4	-	-	-	SPI4_MOSI	-	-	-	-	SAI2_MCK_B	-	FMC_D11	-	LCD_CLK	EVENTOUT
	PE15	-	TIM1_BKIN	-	-	-	-	-	-	-	-	-	-	FMC_D12	-	LCD_R7	EVENTOUT

Table 13. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx register boundary addresses(1) (continued)

Bus	Boundary address	Peripheral
	0x4001 7C00 - 0x4001 FFFF	Reserved
APB2	0x4001 7800 - 0x4001 7BFF	MDIOS
	0x4001 7400 - 0x4001 77FF	DFSDM1
	0x4001 6C00 - 0x4001 73FF	DSI Host
	0x4001 6800 - 0x4001 6BFF	LCD-TFT
	0x4001 6000 - 0x4001 67FF	Reserved
	0x4001 5C00 - 0x4001 5FFF	SAI2
	0x4001 5800 - 0x4001 5BFF	SAI1
	0x4001 5400 - 0x4001 57FF	SPI6
	0x4001 5000 - 0x4001 53FF	SPI5
	0x4001 4C00 - 0x4001 4FFF	Reserved
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4
	0x4001 3000 - 0x4001 33FF	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	SDMMC1
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1 - ADC2 - ADC3
	0x4001 1C00 - 0x4001 1FFF	SDMMC2
	0x4001 1800 - 0x4001 1BFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1

Table 34. Typical and maximum current consumption in Sleep mode, regulator OFF

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ		Max(1)						Unit
						TA= 25 °C		TA= 85 °C		TA= 105 °C		
				IDD12	IDD	IDD12	IDD	IDD12	IDD	IDD12	IDD	
IDD12/ IDD	Supply current in RUN mode from V12 and V_{DD} supply	All Peripherals Enabled(2)	180	102	1	114	2	148	2	168	2	mA
			168	91	1	101	2	132	2	152	2	
			144	71	1	78	2	105	2	122	2	
			60	32	1	37	2	64	2	81	2	
			25	16	1	20	2	46	2	64	2	
		All Peripherals Disabled	180	13	1	18	2	53	2	73	2	
			168	12	1	16	2	47	2	67	2	
			144	9	1	13	2	39	2	56	2	
			60	5	1	9	2	35	2	52	2	
			25	3	1	7	2	33	2	50	2	

1. Guaranteed by characterization results, unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.

Table 35. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max(1)			Unit
				V_{DD} = 3.6 V			
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
$I_{DD\_STOP\_NM}$ (normal mode)	Supply current in Stop mode, main regulator in Run mode	Flash memory in Stop mode, all oscillators OFF, no IWDG	0.55	3	18	27	mA
		Flash memory in Deep power down mode, all oscillators OFF	0.5	3	18	27	
	Supply current in Stop mode, main regulator in Low-power mode	Flash memory in Stop mode, all oscillators OFF, no IWDG	0.42	2.5	15	24	
		Flash memory in Deep power down mode, all oscillators OFF, no IWDG	0.37	2.5	15	24	
$I_{DD\_STOP\_UDM}$ (under-drive mode)	Supply current in Stop mode, main regulator in Low voltage and under-drive modes	Regulator in Run mode, Flash memory in Deep power down mode, all oscillators OFF, no IWDG	0.18	1.2	6	10	
		Regulator in Low-power mode, Flash memory in Deep power down mode, all oscillators OFF, no IWDG	0.13	1.1	6	10	

1. Data based on characterization, tested in production.

Table 44. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_m_crit_max	Maximum critical crystal g_m	LSEDRV[1:0]=00 Low drive capability	-	-	0.48	µA/V
		LSEDRV[1:0]=10 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0]=01 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0]=11 High drive capability	-	-	2.7	
t_{SU}(2)	start-up time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Guaranteed by characterization results. t_{SU} is the start-up time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 31. Typical application with a 32.768 kHz crystal

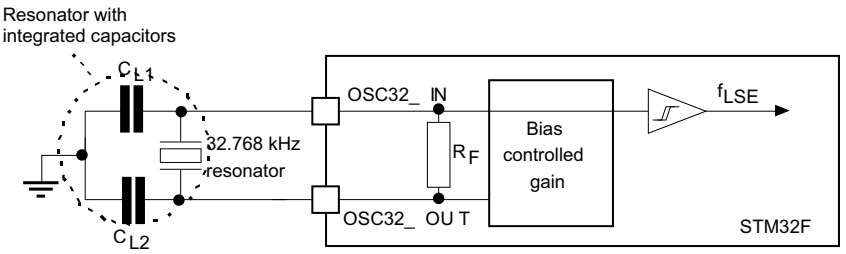


Table 51. MIPI D-PHY characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Output low level voltage	-	1.1	1.2	1.2	V
$V_{IL-ULPS}$	Output high level voltage	-	-50	-	50	mV
V_{IH}	Output impedance of LP transmitter	-	110	-	-	Ω
V_{hys}	15%-85% rise and fall time	-	-	-	25	ns
LP Contention Detector Characteristics						
V_{ILCD}	Logic 0 contention threshold	-	-	-	200	mV
V_{IHCD}	Logic 0 contention threshold	-	450	-	-	

1. Guaranteed based on test during characterization.

Table 52. MIPI D-PHY AC characteristics LP mode and HS/LP transitions(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{LPX}	Transmitted length of any Low-Power state period	-	50	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	-	38	-	95	
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Time that the transmitter drives the HS-0 state prior to starting the clock.	-	300	-	-	
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	-	8	-	-	UI

Table 80. internal reference voltage (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{Coeff}(2)	Temperature coefficient	-	-	30	50	ppm/°C
t_{START}(2)	Startup time	-	-	6	10	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

Table 81. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C V_{DDA} = 3.3 V	0x1FF0 F44A - 0x1FF0 F44B

5.3.28 DAC electrical characteristics

Table 82. DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	1.7(1)	-	3.6	V	-
V_{REF+}	Reference supply voltage	1.7(1)	-	3.6	V	$V_{REF+} \leq V_{DDA}$
V_{SSA}	Ground	0	-	0	V	-
R_{LOAD}(2)	Resistive load with buffer ON	5	-	-	kΩ	-
R_O(2)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(2)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x1C7) to (0xE38) at V_{REF+} = 1.7 V
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer OFF	-	-	V_{REF+} – 1LSB	V	
I_{VREF+}(4)	DAC DC V_{REF} current consumption in quiescent mode (Standby mode)	-	170	240	µA	With no load, worst code (0x800) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
		-	50	75		With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 85* for the SPI interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 85. SPI dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode SPI1,4,5,6 2.7≤VDD≤3.6	-	-	54(2)	MHz
		Master mode SPI1,4,5,6 1.71≤VDD≤3.6			27	
		Master transmitter mode SPI1,4,5,6 1.71≤VDD≤3.6			54	
		Slave receiver mode SPI1,4,5,6 1.71≤VDD≤3.6			54	
		Slave mode transmitter/full duplex SPI1,4,5,6 2.7≤VDD≤3.6			50(3)	
		Slave mode transmitter/full duplex SPI1,4,5,6 1.71≤VDD≤3.6			37(3)	
		Master & Slave mode SPI2,3 1.71≤VDD≤3.6			27	
tsu(NSS)	NSS setup time	Slave mode, SPI presc = 2	$4*T_{PLCK}$	-	-	ns
th(NSS)	NSS hold time	Slave mode, SPI presc = 2	$2*T_{PLCK}$	-	-	
tw(SCKH) tw(SCKL)	SCK high and low time	Master mode	$T_{PLCK} - 2$	T_{PLCK}	$T_{PLCK} + 2$	

Table 88. Dynamics characteristics: SWD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	SWCLK clock frequency	2.7V <VDD< 3.6V	-	-	80	MHz
$1/t_{c(SWCLK)}$		1.71 <VDD< 3.6V	-	-	50	
$t_{w(SWCLKH)}$	SCK high and low time	-	T_{PCLK} – 1	T_{PCLK}	T_{PCLK} + 1	ns
$t_{w(SWCLKL)}$						
$t_{su(SWDIO)}$	SWDIO input setup time	-	3.5	-	-	
$t_{h(SWDIO)}$	SWDIO input hold time	-	0	-	-	
$t_{ov\ (SWDIO)}$	SWDIO output valid time	2.7V <VDD< 3.6V	-	11	12	
		1.71 <VDD< 3.6V	-	11	16.5	
$t_{oh(SWDIO)}$	SWDIO output hold time	-	9	-	-	

JTAG/SWD timing diagrams

Figure 51. JTAG timing diagram

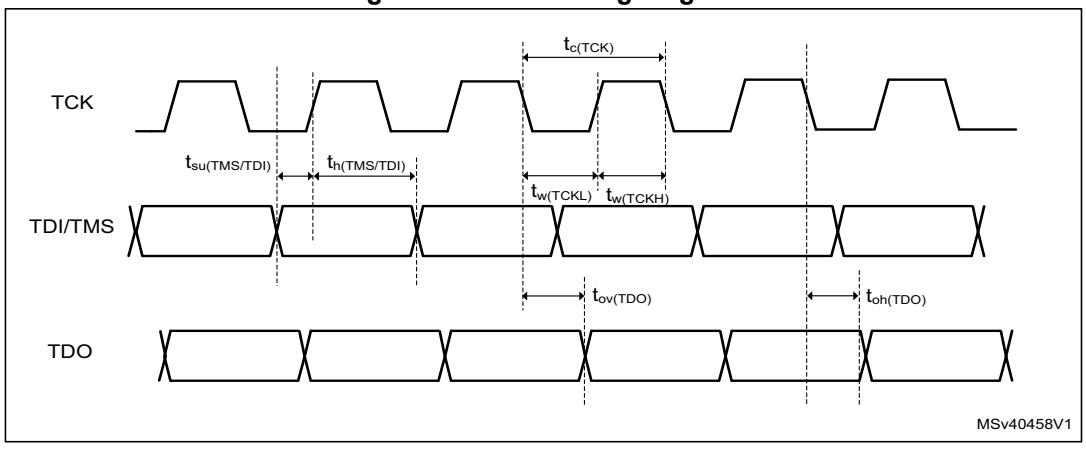


Figure 67. Synchronous non-multiplexed NOR/PSRAM read timings

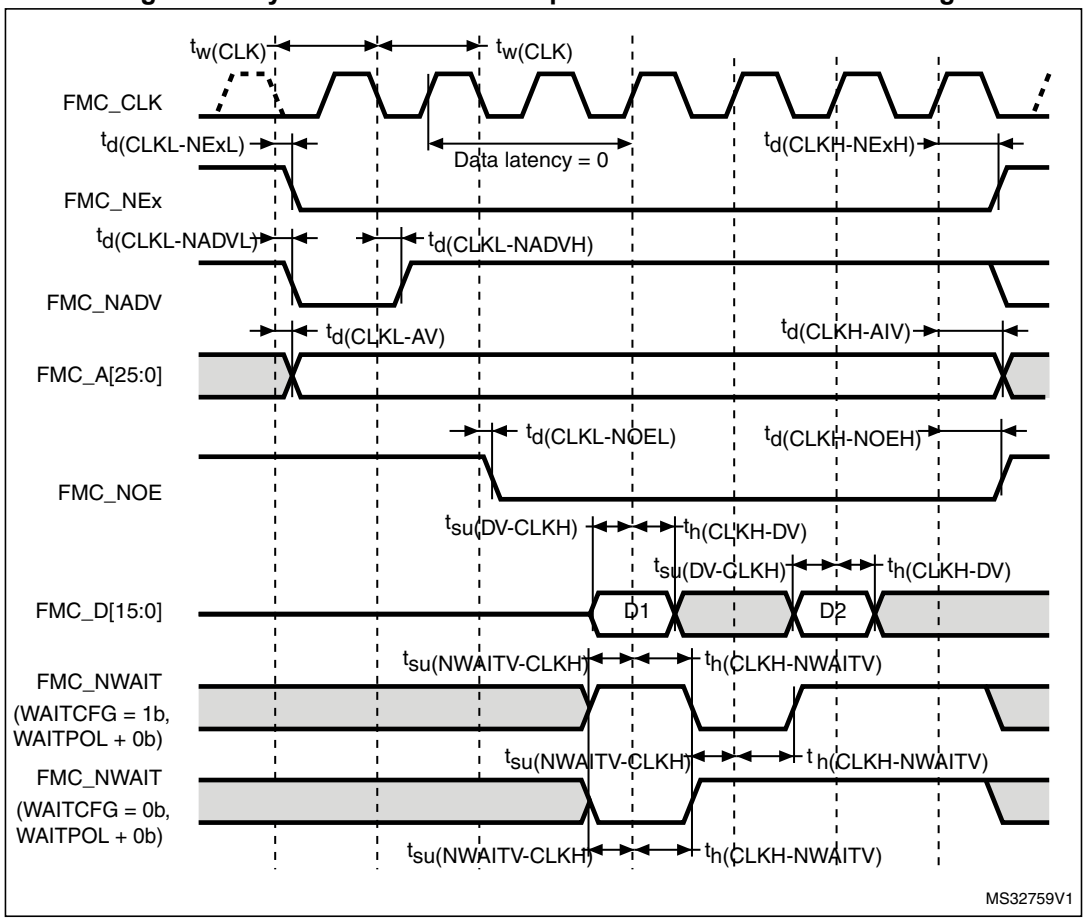


Table 110. Synchronous non-multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK} - 0.5$	-	ns
$t_{(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{HCLK} + 0.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{HCLK} + 0.5$	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	1.5	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	3.5	-	
$t_{(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	3.5	-	