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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	140
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f769iit6g

- LPR is used in the Stop modes:
  The LP regulator mode is configured by software when entering Stop mode.
  Like the MR mode, the LPR can be configured in two ways during stop mode:
  – LPR operates in normal mode (default mode when LPR is ON)
  – LPR operates in under-drive mode (reduced leakage mode).
- Power-down is used in Standby mode.
  The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Refer to *Table 3* for a summary of voltage regulator modes versus device operating modes.

Two external ceramic capacitors should be connected on V_{CAP_1} and V_{CAP_2} pin.

All packages have the regulator ON feature.

Table 3. Voltage regulator configuration mode versus device operating mode(1)

Voltage regulator configuration	Run mode	Sleep mode	Stop mode	Standby mode
Normal mode	MR	MR	MR or LPR	-
Over-drive mode(2)	MR	MR	-	-
Under-drive mode	-	-	MR or LPR	-
Power-down mode	-	-	-	Yes

1. '-' means that the corresponding configuration is not available.
2. The over-drive mode is not available when V_{DD} = 1.7 to 2.1 V.

2.19.2 Regulator OFF

This feature is available only on packages featuring the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a V_{12} voltage source through V_{CAP_1} and V_{CAP_2} pins.

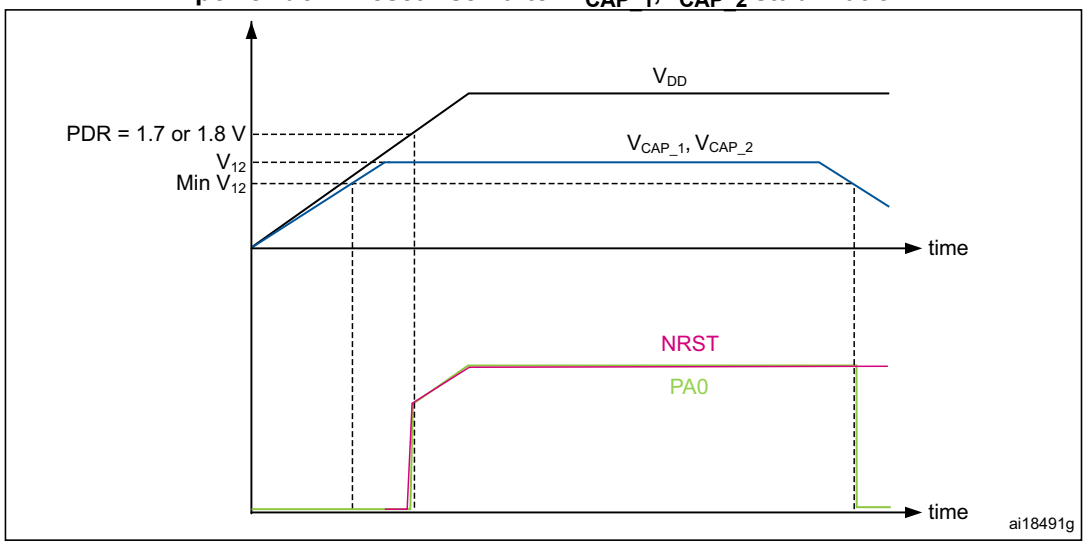
Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency.The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors.

When the regulator is OFF, there is no more internal monitoring on V_{12}. An external power supply supervisor should be used to monitor the V_{12} of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V_{12} power domain.

In the regulator OFF mode, the following features are no more supported:

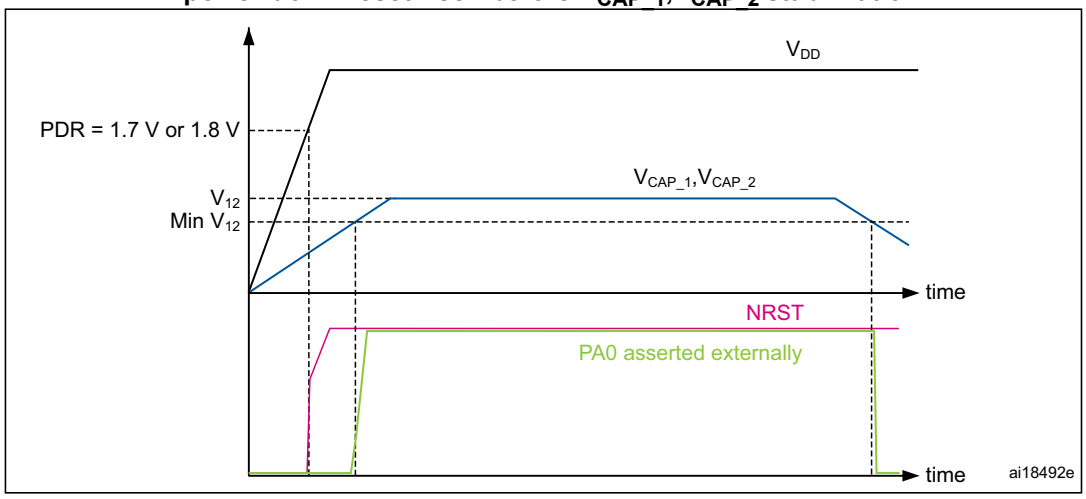
- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V_{12} logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The over-drive and under-drive modes are not available.
- The Standby mode is not available.

Figure 9. Startup in regulator OFF: slow V_{DD} slope - power-down reset risen after V_{CAP_1},V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

Figure 10. Startup in regulator OFF mode: fast V_{DD} slope - power-down reset risen before V_{CAP_1},V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator(LSE)
- The internal low power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32

The RTC is functional in V_{BAT} mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in V_{BAT} mode, but is functional in all low-power modes.

All RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

2.21 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

  The voltage regulator can be put either in main regulator mode (MR) or in low-power mode (LPR). Both modes can be configured as follows (see *Table 5: Voltage regulator modes in stop mode*):

  – Normal mode (default mode when MR or LPR is enabled)

  – Under-drive mode.

  The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup and LPTIM1 asynchronous interrupt).

Table 5. Voltage regulator modes in stop mode

Voltage regulator configuration	Main regulator (MR)	Low-power regulator (LPR)
Normal mode	MR ON	LPR ON
Under-drive mode	MR in under-drive mode	LPR in under-drive mode

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	51	M8	61	72	K7	P9	61	72	K7	VSS	S		-	-	-
-	52	N8	62	73	L8	M8	62	73	L8	VDD	S		-	-	-
-	53	N6	63	74	N6	L8	63	74	N6	PF13	I/O	FT	-	I2C4_SMBA, DFSDM1_DATIN6, FMC_A7, EVENTOUT	-
-	54	R7	64	75	P6	K8	64	75	P6	PF14	I/O	FT	-	I2C4_SCL, DFSDM1_CKIN6, FMC_A8, EVENTOUT	-
-	55	P7	65	76	M8	P8	65	76	M8	PF15	I/O	FT	-	I2C4_SDA, FMC_A9, EVENTOUT	-
-	56	N7	66	77	N7	N8	66	77	N7	PG0	I/O	FT	-	FMC_A10, EVENTOUT	-
-	57	M7	67	78	M7	L7	67	78	M7	PG1	I/O	FT	-	FMC_A11, EVENTOUT	-
37	58	R8	68	79	R8	M7	68	79	R8	PE7	I/O	FT	-	TIM1_ETR, DFSDM1_DATIN2, UART7_RX, QUADSPI_BK2_IO0, FMC_D4, EVENTOUT	-
38	59	P8	69	80	N9	N7	69	80	N9	PE8	I/O	FT	-	TIM1_CH1N, DFSDM1_CKIN2, UART7_TX, QUADSPI_BK2_IO1, FMC_D5, EVENTOUT	-
39	60	P9	70	81	P9	P7	70	81	P9	PE9	I/O	FT	-	TIM1_CH1, DFSDM1_CKOUT, UART7_RTS, QUADSPI_BK2_IO2, FMC_D6, EVENTOUT	-
-	61	M9	71	82	K8	-	71	82	K8	VSS	S	-	-	-	-
-	62	N9	72	83	L9	-	72	83	L9	VDD	S	-	-	-	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

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STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
55	77	P15	96	108	L15	M3	89	108	L15	PD8	I/O	FT	-	DFSDM1_CKIN3, USART3_TX, SPDIF_RX1, FMC_D13, EVENTOUT	-
56	78	P14	97	109	L14	L3	90	109	L14	PD9	I/O	FT	-	DFSDM1_DATIN3, USART3_RX, FMC_D14, EVENTOUT	-
57	79	N15	98	110	K15	M2	91	110	K15	PD10	I/O	FT	-	DFSDM1_CKOUT, USART3_CK, FMC_D15, LCD_B3, EVENTOUT	-
58	80	N14	99	111	N10	K3	92	111	N10	PD11	I/O	FT	-	I2C4_SMBA, USART3_CTS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16/FMC_CLE, EVENTOUT	-
59	81	N13	100	112	M10	J4	93	112	M10	PD12	I/O	FT	-	TIM4_CH1, LPTIM1_IN1, I2C4_SCL, USART3_RTS, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17/FMC_ALE, EVENTOUT	-
60	82	M15	101	113	M11	L2	94	113	M11	PD13	I/O	FT	-	TIM4_CH2, LPTIM1_OUT, I2C4_SDA, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18, EVENTOUT	-
-	83	-	102	114	J10	M1	95	114	J10	VSS	S		-	-	-
-	84	J13	103	115	J11	-	96	115	J11	VDD	S		-	-	-
61	85	M14	104	116	L12	L1	97	116	L12	PD14	I/O	FT	-	TIM4_CH3, UART8_CTS, FMC_D0, EVENTOUT	-
62	86	L14	105	117	K13	K2	98	117	K13	PD15	I/O	FT	-	TIM4_CH4, UART8_RTS, FMC_D1, EVENTOUT	-
-	-	-	-	118	K12	-	-	-	-	PJ6	I/O	FT	-	LCD_R7, EVENTOUT	-
-	-	-	-	119	J12	-	-	-	-	PJ7	I/O	FT	-	LCD_G0, EVENTOUT	-

Table 12. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM1	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM1/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM1/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port A	PA11	-	TIM1_CH4	-	-	-	SPI2_NSS/I2S2_WS	UART4_RX	USART1_CTS	-	CAN1_RX	OTG_FS_DM	-	-	-	LCD_R4	EVENTOUT
	PA12	-	TIM1_ETR	-	-	-	SPI2_SCK/I2S2_CK	UART4_TX	USART1_RTS	SAI2_FS_B	CAN1_TX	OTG_FS_DP	-	-	-	LCD_R5	EVENTOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM2_CH1/TIM2_ETR	-	-	HDMI-CEC	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	SPI6_NSS	UART4_RTS	-	-	CAN3_TX	UART7_TX	-	-	EVENTOUT
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	DFSDM1_CKOUT	-	UART4_CTS	LCD_R3	OTG_HS_ULPI_D1	ETH_MII_RXD2	-	-	LCD_G1	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	DFSDM1_DATIN1	-	-	LCD_R6	OTG_HS_ULPI_D2	ETH_MII_RXD3	-	-	LCD_G0	EVENTOUT
	PB2	-	-	-	-	-	-	SAI1_SD_A	SPI3_MOSI/I2S3_SD		QUADSPI_CLK	DFSDM1_CKIN1	-	-	-	-	EVENTOUT
	PB3	JTDO/TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	-	SPI6_SCK	-	SDMMC2_D2	CAN3_RX	UART7_RX	-	-	EVENTOUT
	PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	SPI2_NSS/I2S2_WS	SPI6_MISO	-	SDMMC2_D3	CAN3_TX	UART7_TX	-	-	EVENTOUT
	PB5	-	UART5_RX	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI/I2S1_SD	SPI3_MOSI/I2S3_SD	-	SPI6_MOSI	CAN2_RX	OTG_HS_ULPI_D7	ETH_PPS_OUT	FMC_SDCKE1	DCMI_D10	LCD_G7	EVENTOUT
	PB6	-	UART5_TX	TIM4_CH1	HDMI-CEC	I2C1_SCL	-	DFSDM1_DATIN5	USART1_TX	-	CAN2_TX	QUADSPI_BK1_NCS	I2C4_SCL	FMC_SDNE1	DCMI_D5	-	EVENTOUT

Table 30. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (Dual bank mode) on ITCM interface (ART disabled), regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					TA= 25 °C	TA=85 °C	TA=105 °C	
I_{DD}	Supply current in RUN mode	All peripherals enabled(2)(3)	216	191	218	255	-	mA
			200	178	195	241	269	
			180	164	179	214	236	
			168	147	160	192	212	
			144	121	130	157	175	
			60	60	66	93	111	
			25	28	33	59	77	
		All peripherals disabled(3)	216	93	104	150	-	
			200	87	97	144	171	
			180	83	92	126	148	
			168	75	82	114	134	
			144	65	71	97	115	
			60	35	40	66	84	
			25	16	20	47	64	

1. Guaranteed by characterization results, unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 37. Typical and maximum current consumptions in V_{BAT} mode

Symbol	Parameter	Conditions[1]	Typ			Max[2]		Unit
			T_A =25 °C			T_A =85 °C	T_A =105 °C	
			V_{BAT} = 1.7 V	V_{BAT}= 2.4 V	V_{BAT}= 3.3 V	V_{BAT} = 3.6 V		
I_{DD_VBAT}	Supply current in V_{BAT} mode	Backup SRAM OFF, RTC and LSE OFF	0.03	0.04	0.04	0.2	0.4	µA
		Backup SRAM ON, RTC and LSE OFF	0.77	0.78	0.83	3.2	7.4	
		Backup SRAM OFF, RTC ON and LSE in low drive mode	0.62	0.8	1.13	4.4	10.2	
		Backup SRAM OFF, RTC ON and LSE in medium low drive mode	0.65	0.83	1.17	4.6	10.6	
		Backup SRAM OFF, RTC ON and LSE in medium high drive mode	0.75	0.94	1.28	5.0	11.4	
		Backup SRAM OFF, RTC ON and LSE in high drive mode	0.9	1.08	1.43	5.5	12.8	
		Backup SRAM ON, RTC ON and LSE in low drive mode	1.35	1.54	1.91	7.3	17.2	
		Backup SRAM ON, RTC ON and LSE in Medium low drive mode	1.38	1.57	1.93	7.9	18.4	
		Backup SRAM ON, RTC ON and LSE in Medium high drive mode	1.53	1.73	2.11	8.0	18.7	
		Backup SRAM ON, RTC ON and LSE in High drive mode	1.67	1.87	2.26	9.0	21.0	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a C_L of 6 pF for typical values.
2. Guaranteed by characterization results.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate a current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 65: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Table 38. Switching output I/O current consumption(1) (continued)

Symbol	Parameter	Conditions	I/O toggling frequency (fsw) MHz	Typ V_{DD} = 3.3 V	Typ V_{DD} = 1.8 V	Unit
I_{DDIO}	I/O switching Current	C_{EXT} = 22 pF $C = C_{INT} + C_S + C_{EXT}$	2	0.3	0.1	mA
			8	1.0	0.5	
			25	3.5	1.6	
			50	5.9	4.2	
			60	10.0	4.4	
			84	19.12	5.8	
			90	19.6	-	
		C_{EXT} = 33 pF $C = C_{INT} + C_S + C_{EXT}$	2	0.3	0.2	
			8	1.3	0.7	
			25	3.5	2.3	
			50	10.26	5.19	
			60	16.53	-	

1. CINT + C_S, PCB board capacitance including the pad pin is estimated to15 pF.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- I/O compensation cell enabled.
- The ART/L1-cache is ON.
- Scale 1 mode selected, internal digital voltage V12 = 1.32 V.
- HCLK is the system clock. $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
  - f_{HCLK} = 216 MHz (Scale 1 + over-drive ON), f_{HCLK} = 168 MHz (Scale 2), f_{HCLK} = 144 MHz (Scale 3)
- Ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Table 39. Peripheral current consumption

Peripheral		I_{DD}(Typ)[1]			Unit
		Scale 1	Scale 2	Scale 3	
AHB1 (up to 216 MHz)	GPIOA	2.9	2.8	2.2	µA/MHz
	GPIOB	3.0	2.9	2.2	
	GPIOC	2.9	2.8	2.2	
	GPIOD	3.1	3.0	2.3	
	GPIOE	3.1	3.0	2.3	
	GPIOF	2.9	2.8	2.2	
	GPIOG	2.9	2.8	2.2	
	GPIOH	3.1	3.1	2.4	
	GPIOI	3.0	2.9	2.2	
	GPIOJ	2.9	2.9	2.2	
	GPIOK	2.8	2.8	2.4	
	CRC	1.0	0.9	0.8	
	BKPSRAM	0.9	0.9	0.7	
	DMA1	3.17 x N + 11.63	3.08 x N + 11.39	2.6 x N + 9.64	
	DMA2	3.33 x N + 12.84	3.27 x N + 11.84	2.75 x N + 10.10	
	DMA2D	77.7	76.3	63.5	
	ETH_MAC ETH_MAC_TX ETH_MAC_RX ETH_MAC_PTP	40.1	39.5	32.8	
	OTG_HS	58.5	57.4	48.1	
	OTG_HS+ULPI	58.5	57.4	48.1	
AHB2 (up to 216 MHz)	DCMI	2.9	2.8	2.1	µA/MHz
	JPEG	74.8	73.4	61.9	
	RNG	6.7	6.7	5.4	
	USB_OTG_FS	32.4	31.9	26.7	
AHB3 (up to 216 MHz)	FMC	18.6	18.2	15.1	µA/MHz
	QSPI	22.3	21.8	18.1	
Bus matrix[2]		3.94	3.25	2.12	µA/MHz

Table 39. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ)(1)			Unit
		Scale 1	Scale 2	Scale 3	
APB2 (up to 108 MHz)	TIM1	24.1	23.8	19.6	µA/MHz
	TIM8	24.5	24.2	20.0	
	USART1	17.7	17.4	14.3	
	USART6	11.9	11.8	9.4	
	ADC1(5)	4.5	4.7	3.5	
	ADC2(5)	4.5	4.7	3.3	
	ADC3(5)	4.5	4.6	3.3	
	SDMMC1	8.4	8.3	6.9	
	SDMMC2	8.2	8.2	6.4	
	SPI1/I2S1(3)	3.9	3.6	3.1	
	SPI4	3.9	3.6	3.1	
	SYSCFG	2.5	2.2	1.9	
	TIM9	8.0	8.0	6.2	
	TIM10	5.0	5.1	3.7	
	TIM11	6.9	6.9	5.3	
	SPI5	2.7	2.8	1.8	
	SPI6	3.1	3.2	2.2	
	SAI1	3.2	3.3	2.2	
	DFSDM1	10.9	10.7	9.0	
	SAI2	3.9	3.9	2.8	
	MDIO	7.1	7.0	5.8	
	LTDC	51.2	50.3	41.8	
	DSI	8.5	8.4	8.1	

1. When the I/O compensation cell is ON, I_{DD} typical value increases by 0.22 mA.
2. The BusMatrix is automatically active when at least one master is ON.
3. To enable an I2S peripheral, first set the I2SMOD bit and then the I2SE bit in the SPI_I2SCFGR register.
4. When the DAC is ON and EN1/2 bits are set in DAC_CR register, add an additional power consumption of 0.75 mA per DAC channel for the analog part.
5. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 42. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{f(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Figure 28. High-speed external clock source AC timing diagram

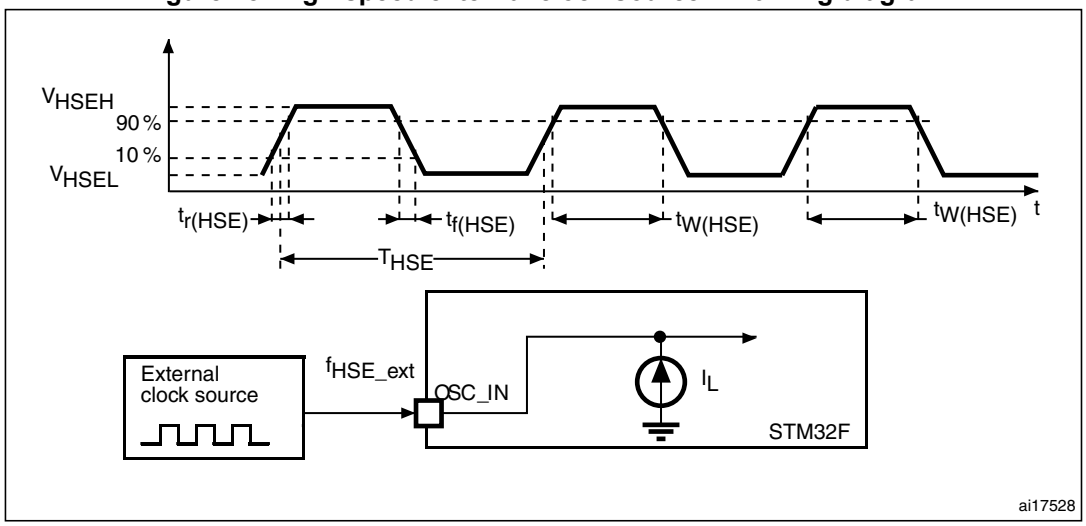
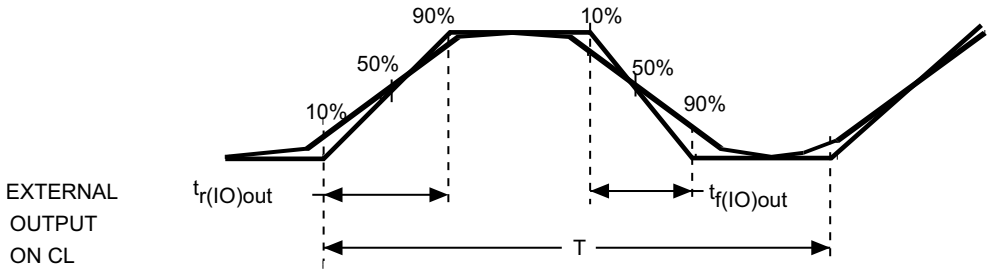


Table 67. I/O AC characteristics(1)(2) (continued)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 30 pF, V_{DD} ≥ 2.7 V	-	-	100(4)	MHz
			C_L = 30 pF, V_{DD} ≥ 1.8 V	-	-	50	
			C_L = 30 pF, V_{DD} ≥ 1.7 V	-	-	42.5	
			C_L = 10 pF, V_{DD}≥ 2.7 V	-	-	180(4)	
			C_L = 10 pF, V_{DD} ≥ 1.8 V	-	-	100	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	72.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 30 pF, V_{DD} ≥ 2.7 V	-	-	4	ns
			C_L = 30 pF, V_{DD} ≥1.8 V	-	-	6	
			C_L = 30 pF, V_{DD} ≥1.7 V	-	-	7	
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	2.5	
			C_L = 10 pF, V_{DD} ≥1.8 V	-	-	3.5	
			C_L = 10 pF, V_{DD} ≥1.7 V	-	-	4	
-	tEXTIpw	Pulse width of external signals detected by the EXTI controller	-	10	-	-	ns

1. Guaranteed by design.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F76xxx and STM32F77xxx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in *Figure 39*.
4. For maximum frequencies above 50 MHz and V_{DD} > 2.4 V, the compensation cell should be used.

Figure 39. I/O AC characteristics definition



Maximum frequency is achieved if (t_r + t_f) ≤ (2/3)T and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

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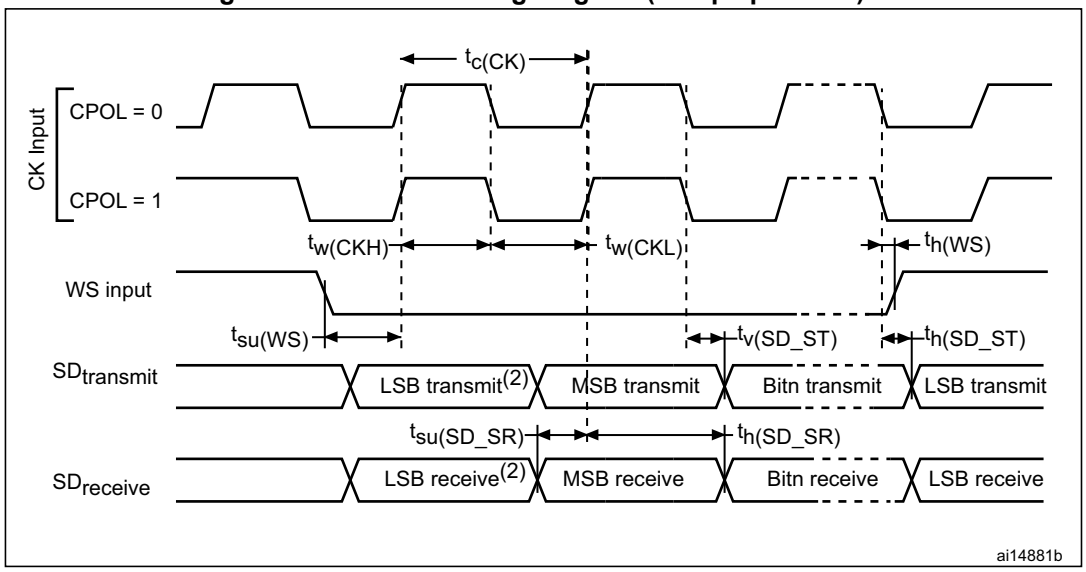
Table 71. ADC characteristics (continued)

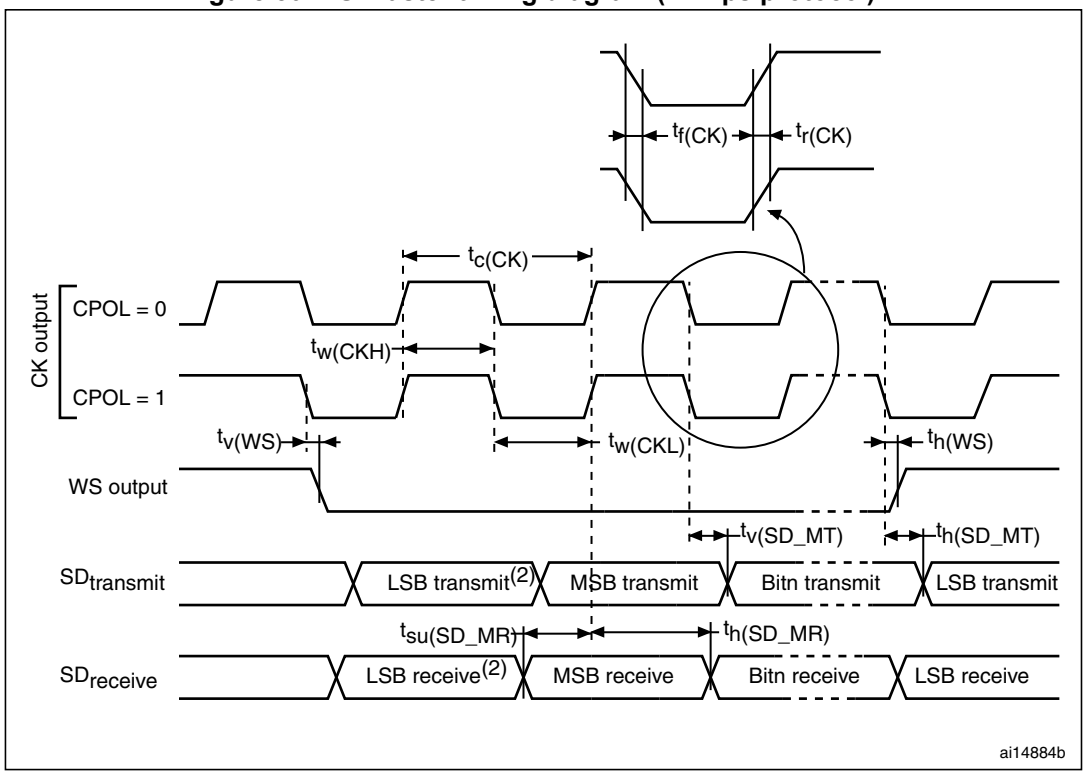
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 30 MHz, 12-bit resolution	-	-	1764	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* for details	-	-	50	kΩ
R_{ADC}(2)(4)	Sampling switch resistance	-	-	-	6	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	4	7	pF
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.100	µs
			-	-	3(5)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.067	µs
			-	-	2(5)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 30 MHz	0.100	-	16	µs
		-	3	-	480	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	-	2	3	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 30 MHz 12-bit resolution	0.50	-	16.40	µs
		f_{ADC} = 30 MHz 10-bit resolution	0.43	-	16.34	µs
		f_{ADC} = 30 MHz 8-bit resolution	0.37	-	16.27	µs
		f_{ADC} = 30 MHz 6-bit resolution	0.30	-	16.20	µs
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$
f_S(2)	Sampling rate (f_{ADC} = 36 MHz, and t_S = 3 ADC cycles)	12-bit resolution Single ADC	-	-	2.4	Msps
		12-bit resolution Interleave Dual ADC mode	-	-	4.5	Msps
		12-bit resolution Interleave Triple ADC mode	-	-	7.2	Msps

Figure 49. I²S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 50. I²S master timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 57. Ethernet SMI timing diagram

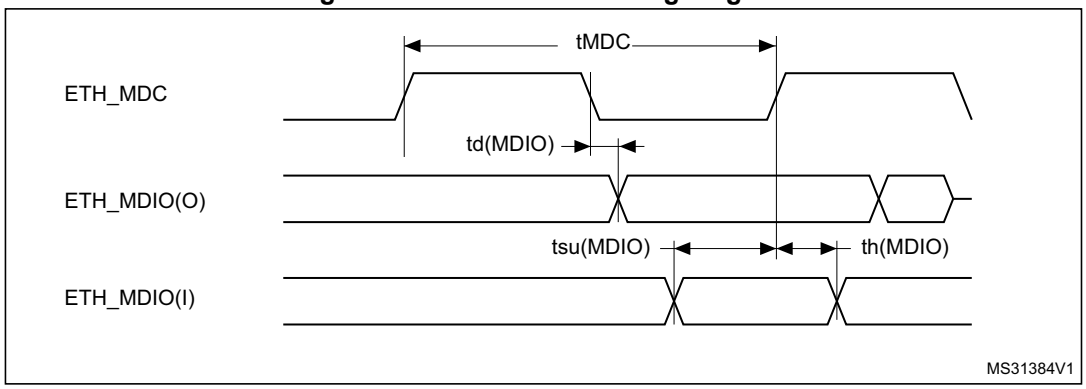


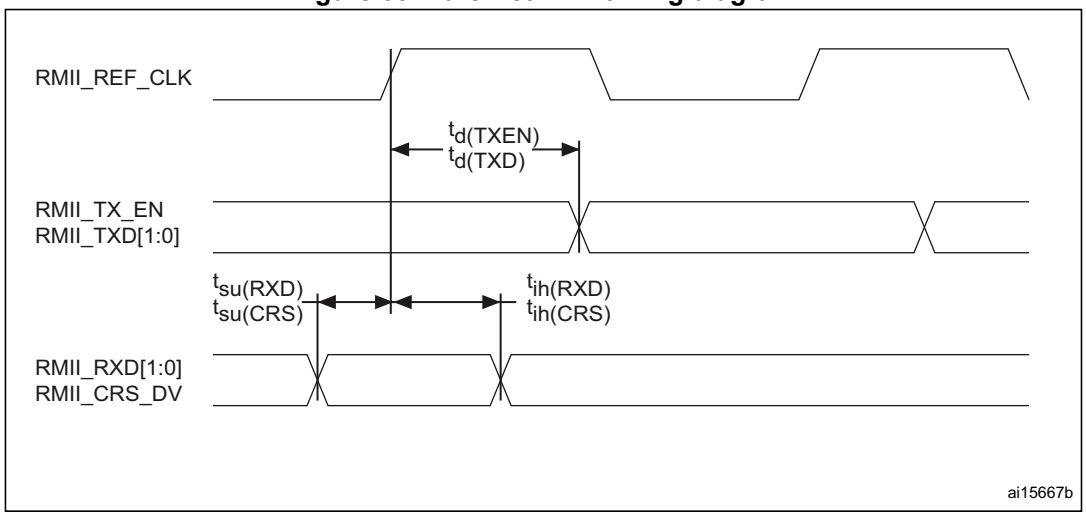
Table 96. Dynamics characteristics: Ethernet MAC signals for SMI(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time(2.38 MHz)	400	400	403	ns
$T_{d(MDIO)}$	Write data valid time	T_{HCLK} + 1	T_{HCLK} + 1.5	T_{HCLK} + 3	
$t_{su(MDIO)}$	Read data setup time	12.5	-	-	
$t_{h(MDIO)}$	Read data hold time	0	-	-	

1. Guaranteed by characterization results.

Table 97 gives the list of Ethernet MAC signals for the RMII and *Figure 58* shows the corresponding timing diagram.

Figure 58. Ethernet RMII timing diagram



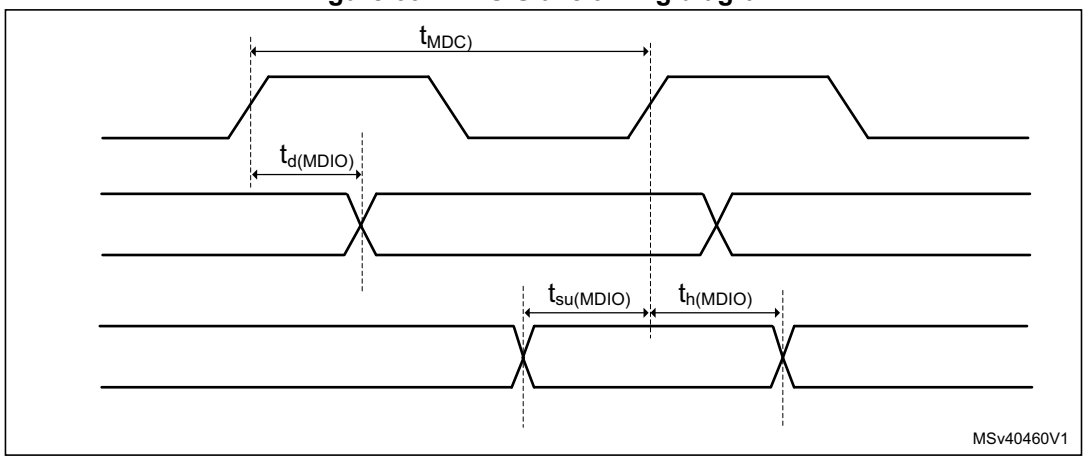
1. Guaranteed by characterization results.

Table 99. MDIO Slave timing parameters

Symbol	Parameter	Min	Typ	Max	Unit
F_{sDC}	Management Data clock	-	-	40	MHz
$t_{d(MDIO)}$	Management Data input/output **output valid time**	7	8	20	ns
$t_{su(MDIO)}$	Management Data input/output **setup time**	4	-	-	
$t_{h(MDIO)}$	Management Data input/output **hold time**	1	-	-	

The MDIO controller is mapped on APB2 domain. The frequency of the APB bus should at least 1.5 times the MDC frequency: $F_{PCLK2} \geq 1.5 * F_{MDC}$

Figure 60. MDIO Slave timing diagram



CAN (controller area network) interface

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (CANx_TX and CANx_RX).

5.3.30 FMC characteristics

Unless otherwise specified, the parameters given in *Table 100* to *Table 113* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$

1. Guaranteed by characterization results.

Table 107. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK} - 1$	$9T_{HCLK} + 1$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{HCLK} - 0.5$	$7T_{HCLK} + 0.5$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK} + 2$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK} - 1$	-	

1. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 65 through *Figure 68* represent synchronous waveforms and *Table 108* through *Table 111* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

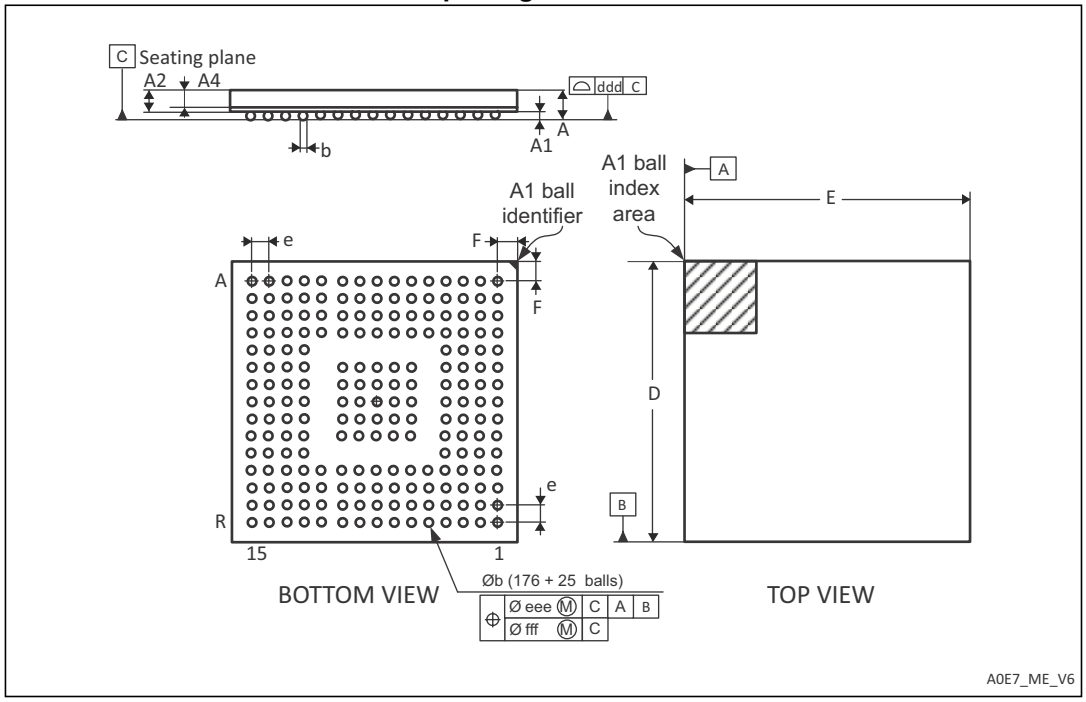
- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1;
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM
- CL = 30 pF on data and address lines. CL = 10 pF on FMC_CLK unless otherwise specified.

In all the timing tables, the T_{HCLK} is the HCLK clock period.

  - For 2.7 V≤ V_{DD}≤ 3.6 V, maximum FMC_CLK = 100 MHz at CL=20 pF or 90 MHz at CL=30 pF (on FMC_CLK).
  - For 1.71 V≤ V_{DD}<2.7 V, maximum FMC_CLK = 70 MHz at CL=10 pF (on FMC_CLK).

6.6 UFBGA176+25, 10 x 10, 0.65 mm ultra thin fine-pitch ball grid array package information

Figure 98. UFBGA176+25, 10 × 10 × 0.65 mm ultra thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 131. UFBGA176+25, 10 × 10 × 0.65 mm ultra thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.002	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	9.950	10.000	10.050	0.3917	0.3937	0.3957
E	9.950	10.000	10.050	0.3917	0.3937	0.3957
e	-	0.650	-	-	0.0256	-
F	0.400	0.450	0.500	0.0157	0.0177	0.0197
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.