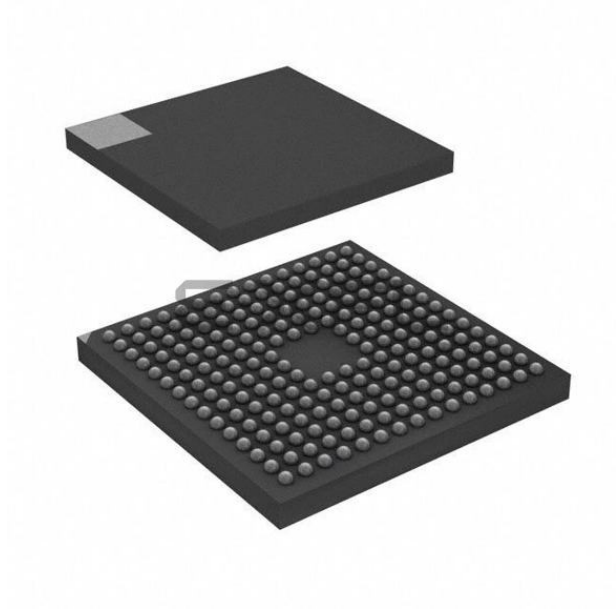

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	168
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	216-TFBGA
Supplier Device Package	216-TFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f769ngh6

The devices embed two dedicated PLL (PLLI2S and PLLSAI) which allow to achieve audio class performance. In this case, the I^2S and SAI master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

2.16 Boot modes

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDx option bytes, allowing to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF which includes:

- All Flash address space mapped on ITCM or AXIM interface
- All RAM address space: ITCM, DTCM RAMs and SRAMs mapped on AXIM interface
- The System memory bootloader

The boot loader is located in system memory. It is used to reprogram the Flash memory through a serial interface. Refer to *STM32 microcontroller system memory boot mode* application note (AN2606) for details.

2.17 Power supply schemes

- V_{DD} = 1.7 to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.7 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Note: V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the internal reset is OFF (refer to Section 2.18.2: Internal reset OFF). Refer to Table 3: Voltage regulator configuration mode versus device operating mode to identify the packages supporting this option.

- $V_{DDSDMMC}$ can be connected either to V_{DD} or an external independent power supply (1.8 to 3.6V) for SDMMC2 pins (clock, command, and 4-bit data). For example, when the device is powered at 1.8V, an independent power supply 2.7V can be connected to $V_{DDSDMMC}$.When the $V_{DDSDMMC}$ is connected to a separated power supply, it is independent from V_{DD} or V_{DDA} but it must be the last supply to be provided and the first to disappear. The following conditions $V_{DDSDMMC}$ must be respected:
  - During the power-on phase ($V_{DD} < V_{DD\_MIN}$), $V_{DDSDMMC}$ should be always lower than V_{DD}
  - During the power-down phase ($V_{DD} < V_{DD\_MIN}$), $V_{DDSDMMC}$ should be always lower than V_{DD}
  - The $V_{DDSDMMC}$ rising and falling time rate specifications must be respected (see *Table 20* and *Table 21*)
  - In operating mode phase, $V_{DDSDMMC}$ could be lower or higher than V_{DD}: All associated GPIOs powered by $V_{DDSDMMC}$ are operating between $V_{DDSDMMC\_MIN}$ and $V_{DDSDMMC\_MAX}$.
- V_{DDUSB} can be connected either to V_{DD} or an external independent power supply (3.0 to 3.6V) for USB transceivers (refer to *Figure 4* and *Figure 5*). For example, when the device is powered at 1.8V, an independent power supply 3.3V can be connected to V_{DDUSB}. When the V_{DDUSB} is connected to a separated power supply, it is independent from V_{DD} or V_{DDA} but it must be the last supply to be provided and the first to

2.31 SD/SDIO/MMC card host interface (SDMMC)

SDMMC host interfaces are available, that support the MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 50 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDMMC Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDMMC/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

The SDMMC can be served by the DMA controller

2.32 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

  - 16-bit RGB, configurations 1, 2, and 3
  - 18-bit RGB, configurations 1 and 2
  - 24-bit RGB
- Programmable polarity of all LTDC interface signals
- Extended resolutions beyond the DPI standard
- Maximum resolution of 800x480 pixels:
- Maximum resolution is limited by available DSI physical link bandwidth:
  - Number of lanes: 2
  - Maximum speed per lane: 500 Mbps1Gbps

Adapted interface features

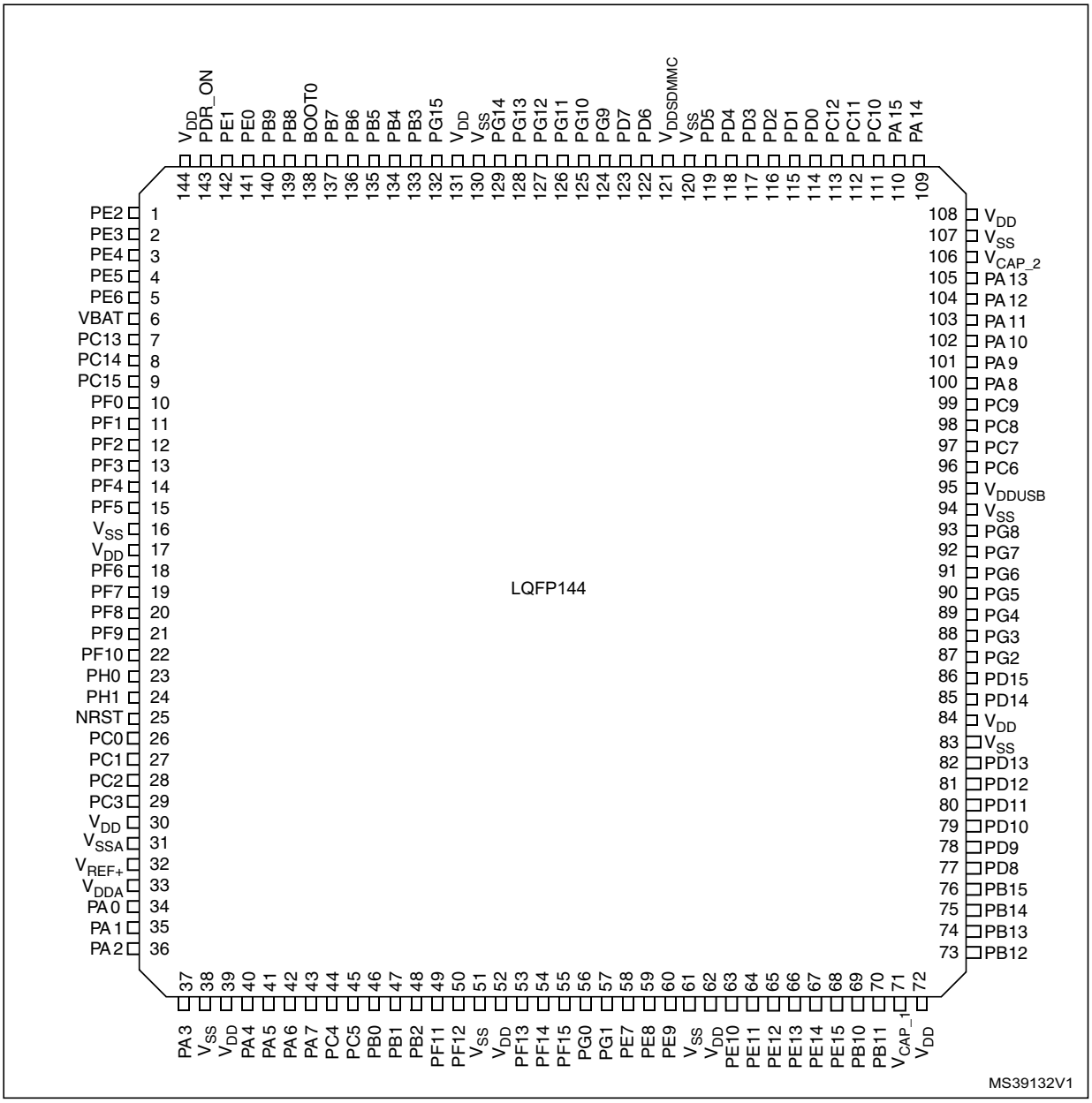
Support for sending large amounts of data through the memory_write_start(WMS) and memory_write_continue(WMC) DCS commands

- LTDC interface color coding mappings into 24-bit interface:
  - 16-bit RGB, configurations 1, 2, and 3
  - 18-bit RGB, configurations 1 and 2
  - 24-bit RGB

Video mode pattern generator:

- Vertical and horizontal color bar generation without LTDC stimuli
- BER pattern without LTDC stimuli

Figure 12. STM32F76xxx LQFP144 pinout



1. The above figure shows the package top view.

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	51	M8	61	72	K7	P9	61	72	K7	VSS	S		-	-	-
-	52	N8	62	73	L8	M8	62	73	L8	VDD	S		-	-	-
-	53	N6	63	74	N6	L8	63	74	N6	PF13	I/O	FT	-	I2C4_SMBA, DFSDM1_DATIN6, FMC_A7, EVENTOUT	-
-	54	R7	64	75	P6	K8	64	75	P6	PF14	I/O	FT	-	I2C4_SCL, DFSDM1_CKIN6, FMC_A8, EVENTOUT	-
-	55	P7	65	76	M8	P8	65	76	M8	PF15	I/O	FT	-	I2C4_SDA, FMC_A9, EVENTOUT	-
-	56	N7	66	77	N7	N8	66	77	N7	PG0	I/O	FT	-	FMC_A10, EVENTOUT	-
-	57	M7	67	78	M7	L7	67	78	M7	PG1	I/O	FT	-	FMC_A11, EVENTOUT	-
37	58	R8	68	79	R8	M7	68	79	R8	PE7	I/O	FT	-	TIM1_ETR, DFSDM1_DATIN2, UART7_RX, QUADSPI_BK2_IO0, FMC_D4, EVENTOUT	-
38	59	P8	69	80	N9	N7	69	80	N9	PE8	I/O	FT	-	TIM1_CH1N, DFSDM1_CKIN2, UART7_TX, QUADSPI_BK2_IO1, FMC_D5, EVENTOUT	-
39	60	P9	70	81	P9	P7	70	81	P9	PE9	I/O	FT	-	TIM1_CH1, DFSDM1_CKOUT, UART7_RTS, QUADSPI_BK2_IO2, FMC_D6, EVENTOUT	-
-	61	M9	71	82	K8	-	71	82	K8	VSS	S	-	-	-	-
-	62	N9	72	83	L9	-	72	83	L9	VDD	S	-	-	-	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
55	77	P15	96	108	L15	M3	89	108	L15	PD8	I/O	FT	-	DFSDM1_CKIN3, USART3_TX, SPDIF_RX1, FMC_D13, EVENTOUT	-
56	78	P14	97	109	L14	L3	90	109	L14	PD9	I/O	FT	-	DFSDM1_DATIN3, USART3_RX, FMC_D14, EVENTOUT	-
57	79	N15	98	110	K15	M2	91	110	K15	PD10	I/O	FT	-	DFSDM1_CKOUT, USART3_CK, FMC_D15, LCD_B3, EVENTOUT	-
58	80	N14	99	111	N10	K3	92	111	N10	PD11	I/O	FT	-	I2C4_SMBA, USART3_CTS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16/FMC_CLE, EVENTOUT	-
59	81	N13	100	112	M10	J4	93	112	M10	PD12	I/O	FT	-	TIM4_CH1, LPTIM1_IN1, I2C4_SCL, USART3_RTS, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17/FMC_ALE, EVENTOUT	-
60	82	M15	101	113	M11	L2	94	113	M11	PD13	I/O	FT	-	TIM4_CH2, LPTIM1_OUT, I2C4_SDA, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18, EVENTOUT	-
-	83	-	102	114	J10	M1	95	114	J10	VSS	S		-	-	-
-	84	J13	103	115	J11	-	96	115	J11	VDD	S		-	-	-
61	85	M14	104	116	L12	L1	97	116	L12	PD14	I/O	FT	-	TIM4_CH3, UART8_CTS, FMC_D0, EVENTOUT	-
62	86	L14	105	117	K13	K2	98	117	K13	PD15	I/O	FT	-	TIM4_CH4, UART8_RTS, FMC_D1, EVENTOUT	-
-	-	-	-	118	K12	-	-	-	-	PJ6	I/O	FT	-	LCD_R7, EVENTOUT	-
-	-	-	-	119	J12	-	-	-	-	PJ7	I/O	FT	-	LCD_G0, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	89	K14	108	131	N12	G1	112	131	N12	PG4	I/O	FT	-	FMC_A14/FMC_BA0, EVENTOUT	-
-	90	K13	109	132	N11	G2	113	132	N11	PG5	I/O	FT	-	FMC_A15/FMC_BA1, EVENTOUT	-
-	91	J15	110	133	J15	G3	114	133	J15	PG6	I/O	FT	-	FMC_NE3, DCMI_D12, LCD_R7, EVENTOUT	-
-	92	J14	111	134	J14	G4	115	134	J14	PG7	I/O	FT	-	SAI1_MCLK_A, USART6_CK, FMC_INT, DCMI_D13, LCD_CLK, EVENTOUT	-
-	93	H14	112	135	H14	G5	116	135	H14	PG8	I/O	FT	-	SPI6_NSS, SPDIF_RX2, USART6_RTS, ETH_PPS_OUT, FMC_SDCLK, LCD_G7, EVENTOUT	-
-	94	G12	113	136	G10	F1	117	136	G10	VSS	S		-	-	-
-	95	H13	114	137	G11	F2	118	137	G11	VDDUSB	S		-	-	-
63	96	H15	115	138	H15	G6	119	138	H15	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, I2S2_MCK, DFSDM1_CKIN3, USART6_TX, FMC_NWAIT, SDMMC2_D6, SDMMC1_D6, DCMI_D0, LCD_HSYNC, EVENTOUT	-
64	97	G15	116	139	G15	F3	120	139	G15	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, I2S3_MCK, DFSDM1_DATIN3, USART6_RX, FMC_NE1, SDMMC2_D7, SDMMC1_D7, DCMI_D1, LCD_G6, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	-	C13	134	157	C13	D3	134	157	C13	PI3	I/O	FT	-	TIM8_ETR, SPI2_MOSI/I2S2_SD, FMC_D27, DCMI_D10, EVENTOUT	-
-	-	D9	135	-	F9	-	135	-	F9	VSS	S	-	-	-	
-	-	C9	136	158	E10	-	136	158	E10	VDD	S	-	-	-	--
76	109	A14	137	159	A14	A3	137	159	A14	PA14(JTCK-SWCLK)	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
77	110	A13	138	160	A13	F8	138	160	A13	PA15(JTDI)	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, HDMI_CEC, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SPI6_NSS, UART4_RTS, CAN3_TX, UART7_TX, EVENTOUT	-
78	111	B14	139	161	B14	B4	139	161	B14	PC10	I/O	FT	-	DFSDM1_CKIN5, SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDMMC1_D2, DCMI_D8, LCD_R2, EVENTOUT	-
79	112	B13	140	162	B13	C4	140	162	B13	PC11	I/O	FT	-	DFSDM1_DATIN5, SPI3_MISO, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SDMMC1_D3, DCMI_D4, EVENTOUT	-
80	113	A12	141	163	A12	D4	141	163	A12	PC12	I/O	FT	-	TRACED3, SPI3_MOSI/I2S3_SD, USART3_CK, UART5_TX, SDMMC1_CK, DCMI_D9, EVENTOUT	-

Table 13. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx register boundary addresses(1) (continued)

Bus	Boundary address	Peripheral
	0x4000 8000- 0x4000 FFFF	Reserved
APB1	0x4000 7C00 - 0x4000 7FFF	UART8
	0x4000 7800 - 0x4000 7BFF	UART7
	0x4000 7400 - 0x4000 77FF	DAC
	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6C00 - 0x4000 6FFF	HDMI-CEC
	0x4000 6800 - 0x4000 6BFF	CAN2
	0x4000 6400 - 0x4000 67FF	CAN1
	0x4000 6000 - 0x4000 63FF	I2C4
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 5000 - 0x4000 53FF	UART5
	0x4000 4C00 - 0x4000 4FFF	UART4
	0x4000 4800 - 0x4000 4BFF	USART3
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	SPDIFRX
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	CAN3
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 2400 - 0x4000 27FF	LPTIM1
	0x4000 2000 - 0x4000 23FF	TIM14
	0x4000 1C00 - 0x4000 1FFF	TIM13
	0x4000 1800 - 0x4000 1BFF	TIM12
	0x4000 1400 - 0x4000 17FF	TIM7
	0x4000 1000 - 0x4000 13FF	TIM6
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2

1. The gray color is used for reserved Flash memory addresses.

5.3 Operating conditions

5.3.1 General operating conditions

Table 17. General operating conditions

Symbol	Parameter	Conditions[1]		Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Power Scale 3 (VOS[1:0] bits in PWR_CR register = 0x01), Regulator ON, over-drive OFF		0	-	144	MHz
		Power Scale 2 (VOS[1:0] bits in PWR_CR register = 0x10), Regulator ON	Over-drive OFF	0	-	168	
			Over-drive ON		-	180	
		Power Scale 1 (VOS[1:0] bits in PWR_CR register= 0x11), Regulator ON	Over-drive OFF	0	-	180	
			Over-drive ON		-	216[2]	
f_{PCLK1}	Internal APB1 clock frequency	Over-drive OFF		0	-	45	
		Over-drive ON		0	-	54	
f_{PCLK2}	Internal APB2 clock frequency	Over-drive OFF		0	-	90	
		Over-drive ON		0	-	108	
V_{DD}	Standard operating voltage	-		1.7[3]	-	3.6	V
V_{DDA}[4][5]	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as V_{DD}[6]		1.7[3]	-	2.4	
	Analog operating voltage (ADC limited to 2.4 M samples)			2.4	-	3.6	
V_{DDUSB}	USB supply voltage (supply voltage for PA11,PA12, PB14 and PB15 pins)	USB not used		1.7	3.3	3.6	
		USB used		3.0	-	3.6	
V_{BAT}	Backup operating voltage	-		1.65	-	3.6	
$V_{DDSDMMC}$	SDMMC2 supply voltage (supply voltage for PG[12:9] and PD6 pins)	It can be different from VDD		1.7	-	3.6	
V_{DDDSI}	DSI system operating	-		1.7	-	3.6	

5.3.16 Memory characteristics

Flash memory

The characteristics are given at TA = –40 to 105 °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

Table 55. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode, V_{DD} = 1.7 V	-	14	-	mA
		Write / Erase 16-bit mode, V_{DD} = 2.1 V	-	17	-	
		Write / Erase 32-bit mode, V_{DD} = 3.3 V	-	24	-	

Table 56. Flash memory programming (single bank configuration nDBANK=1)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100(2)	µs
$t_{ERASE32KB}$	Sector (32 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	250	600	
		Program/erase parallelism (PSIZE) = x 32	-	200	500	
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1100	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	800	1400	
		Program/erase parallelism (PSIZE) = x 32	-	500	1100	
$t_{ERASE256KB}$	Sector (256 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2.1	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.5	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t_{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	16	32	s
		Program/erase parallelism (PSIZE) = x 16	-	11	22	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	

Table 57. Flash memory programming (dual bank configuration nDBANK=0) (continued)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{BE}	Bank erase time	Program/erase parallelism (PSIZE) = x 8	-	16	32	s
		Program/erase parallelism (PSIZE) = x 16	-	11	22	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	
V_{prog}	Programming voltage	32-bit program operation	2.7	-	3	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.7	-	3.6	V

1. Guaranteed by characterization results.
2. The maximum programming time is measured after 100K erase operations.

Table 58. Flash memory programming with V_{PP}

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Double word programming	T_A = 0 to +40 °C V_{DD} = 3.3 V V_{PP} = 8.5 V	-	16	100(2)	µs
$t_{ERASE32KB}$	Sector (32 KB) erase time		-	180	-	ms
$t_{ERASE128KB}$	Sector (128 KB) erase time		-	450	-	
$t_{ERASE256KB}$	Sector (256 KB) erase time		-	900	-	
t_{ME}	Mass erase time		-	6.9	-	s
V_{prog}	Programming voltage	-	2.7	-	3.6	V
V_{PP}	V_{PP} voltage range	-	7	-	9	V
I_{PP}	Minimum current sunk on the V_{PP} pin	-	10	-	-	mA
t_{VPP}(3)	Cumulative time during which V_{PP} is applied	-	-	-	1	hour

1. Guaranteed by design.
2. The maximum programming time is measured after 100K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Table 59. Flash memory endurance and data retention

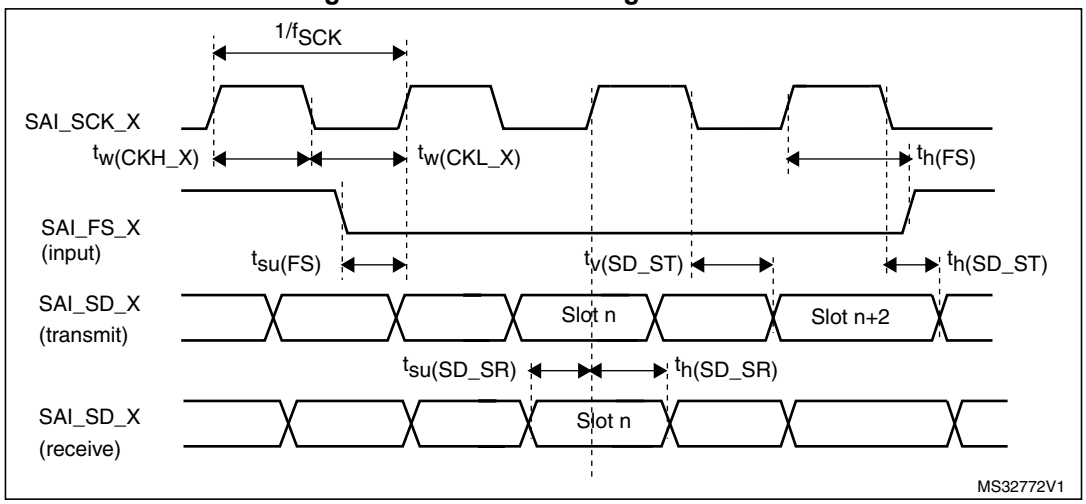
Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

Table 82. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
I_{DDA}(4)	DAC DC V_{DDA} current consumption in quiescent mode(3)	-	280	380	µA	With no load, middle code (0x800) on the inputs
		-	475	625	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
DNL(4)	Differential non linearity Difference between two consecutive code-1LSB)	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration.
		-	-	±2	LSB	Given for the DAC in 12-bit configuration.
INL(4)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±1	LSB	Given for the DAC in 10-bit configuration.
		-	-	±4	LSB	Given for the DAC in 12-bit configuration.
Offset(4)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{REF+}/2)	-	-	±10	mV	Given for the DAC in 12-bit configuration
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(4)	Gain error	-	-	±0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}$(4)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±4LSB	-	3	6	µs	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ
THD(4)	Total Harmonic Distortion Buffer ON	-	-	-	dB	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ
Update rate(2)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ
t_{WAKEUP}(4)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ input code between lowest and highest possible ones.
PSRR+ (2)	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 2.18.2: Internal reset OFF*).
2. Guaranteed by design.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed by characterization results.

Figure 54. SAI slave timing waveforms



USB OTG full speed (FS) characteristics

This interface is present in both the USB OTG HS and USB OTG FS controllers.

Table 90. USB OTG full speed startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB OTG full speed transceiver startup time	1	µs

1. Guaranteed by design.

Table 91. USB OTG full speed DC electrical characteristics

Symbol		Parameter	Conditions	Min. (1)	Typ.	Max. (1)	Unit
Input levels	V_{DDUSB}	USB OTG full speed transceiver operating voltage	-	3.0(2)	-	3.6	V
	V_{DI}(3)	Differential input sensitivity	I(USB_FS_DP/DM, USB_HS_DP/DM)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold	-	1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	

Table 103. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK} - 1$	$8T_{HCLK} + 1$	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{HCLK} - 1.5$	$6T_{HCLK} + 0.5$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK} - 1$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK} + 2$	-	

1. Guaranteed by characterization results.

Figure 63. Asynchronous multiplexed PSRAM/NOR read waveforms

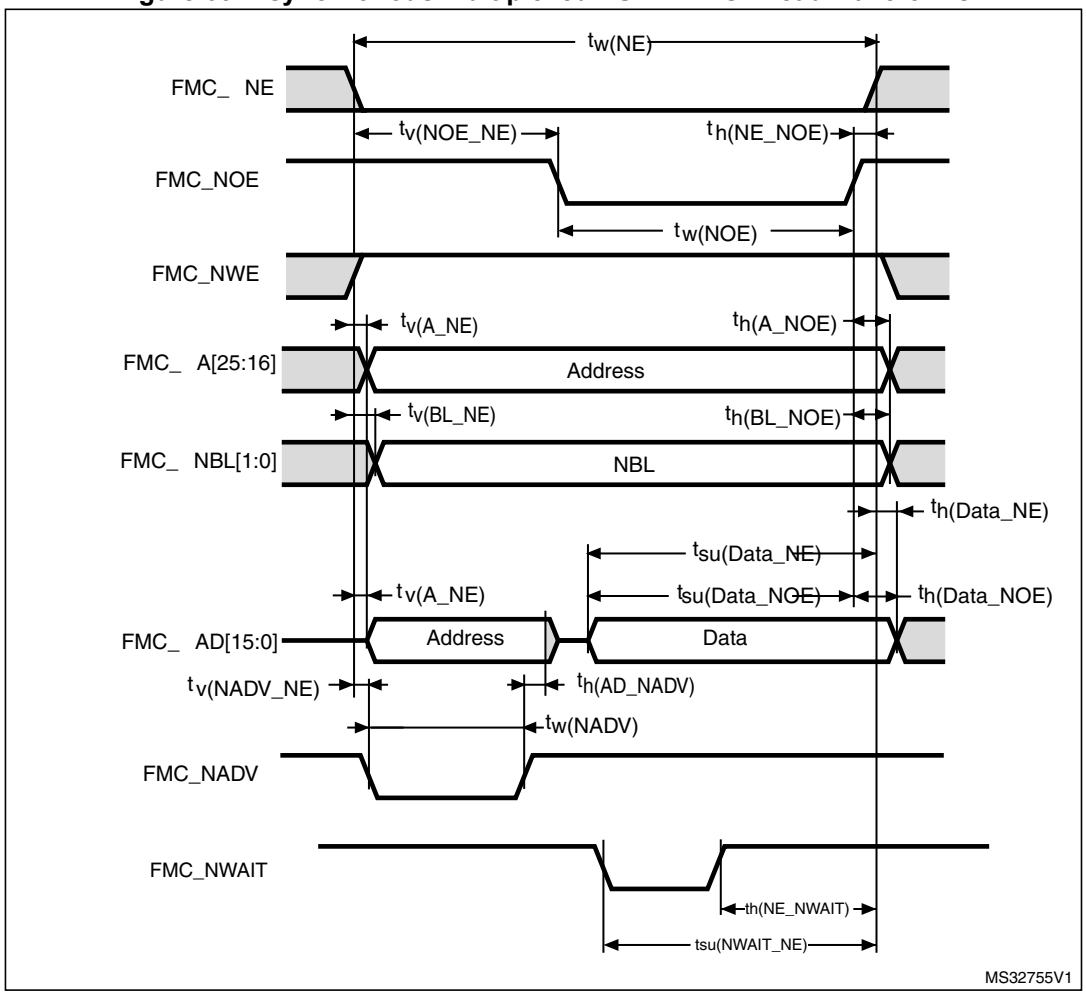


Figure 67. Synchronous non-multiplexed NOR/PSRAM read timings

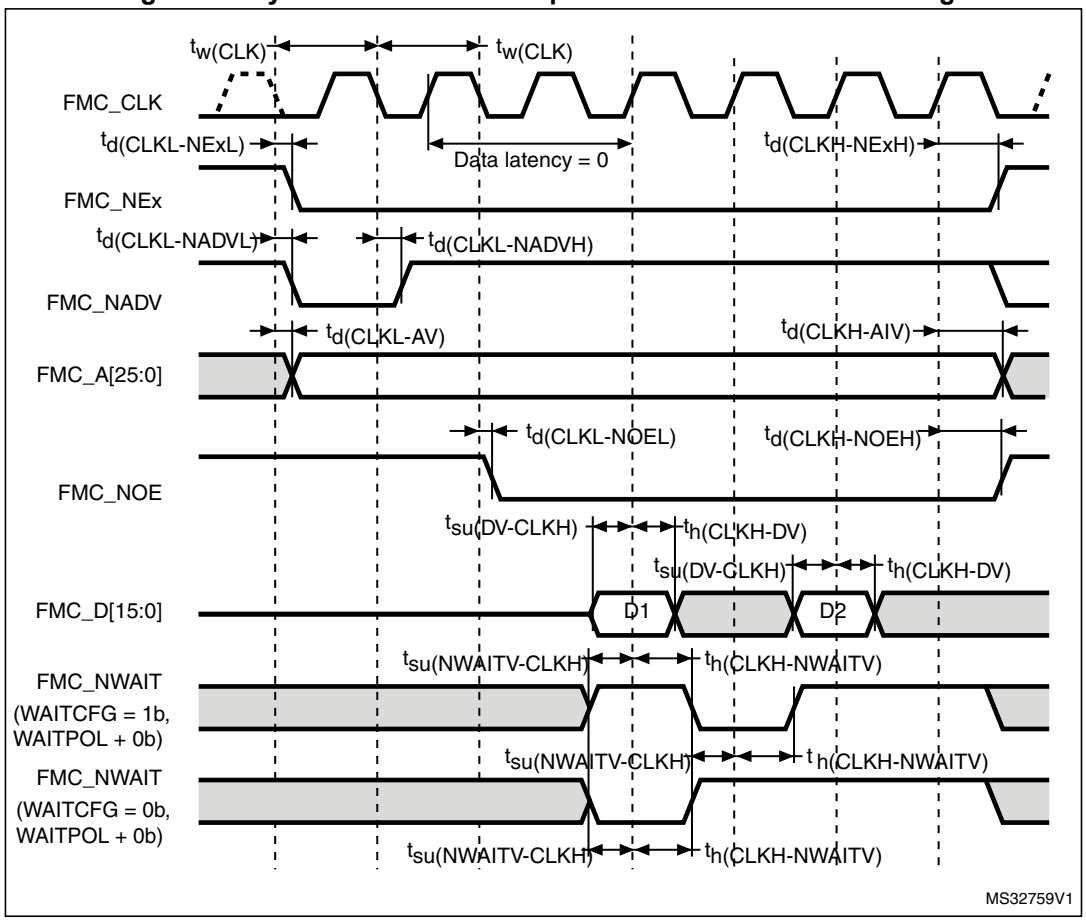


Table 110. Synchronous non-multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK} - 0.5$	-	ns
$t_{(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{HCLK} + 0.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{HCLK} + 0.5$	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	1.5	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	3.5	-	
$t_{(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

Table 122. DFSDM measured timing 1.71-3.6V (continued)

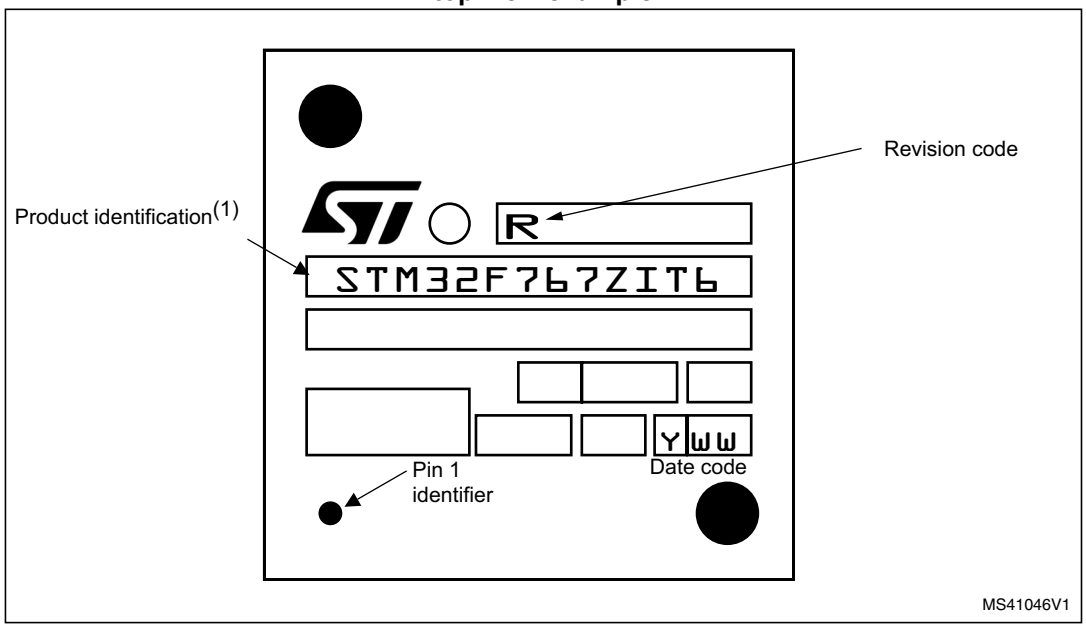
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < V_{DD} < 3.6 V	TCKIN/2 - 0.5	$T_{CKIN}/2$	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < V_{DD} < 3.6 V	2	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < V_{DD} < 3.6 V	3	-	-	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0]=2,3), Internal clock mode (SPICKSEL[1:0]≠0), 1.71 < V_{DD} < 3.6 V	(CKOUTDIV+1) * $T_{DFSDMCLK}$	-	(2*CKOUTDIV) * $T_{DFSDMCLK}$	

LQFP144 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 88. LQFP144, 20 x 20mm, 144-pin low-profile quad flat package top view example



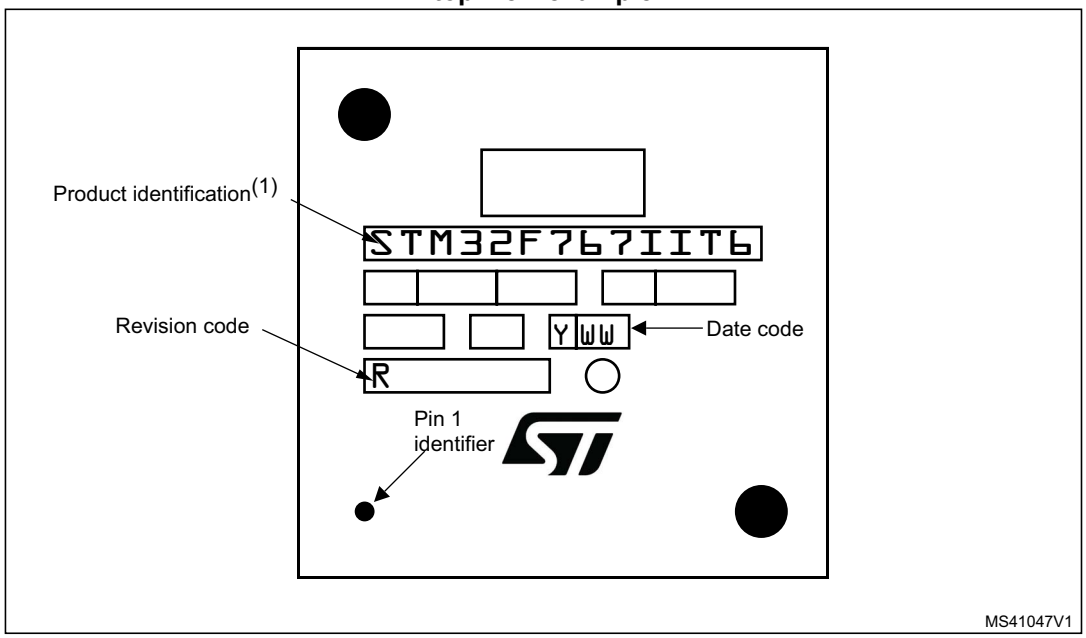
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

LQFP176 device marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 91. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6.8 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max x Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 135. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP100 - 14 × 14 mm / 0.5 mm pitch	43	°C/W
	Thermal resistance junction-ambient WLCSP180 - 0.4 mm pitch	30	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	40	
	Thermal resistance junction-ambient LQFP176 - 24 × 24 mm / 0.5 mm pitch	38	
	Thermal resistance junction-ambient LQFP208 - 28 × 28 mm / 0.5 mm pitch	19	
	Thermal resistance junction-ambient UFBGA176 - 10× 10 mm / 0.5 mm pitch	39	
	Thermal resistance junction-ambient TFBGA216 - 13 × 13 mm / 0.8 mm pitch	29	

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.