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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 56800E |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SCI, SPI |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 32KB (16K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 16 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 8x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LQFP |
| Supplier Device Package | 44-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f8025vld |

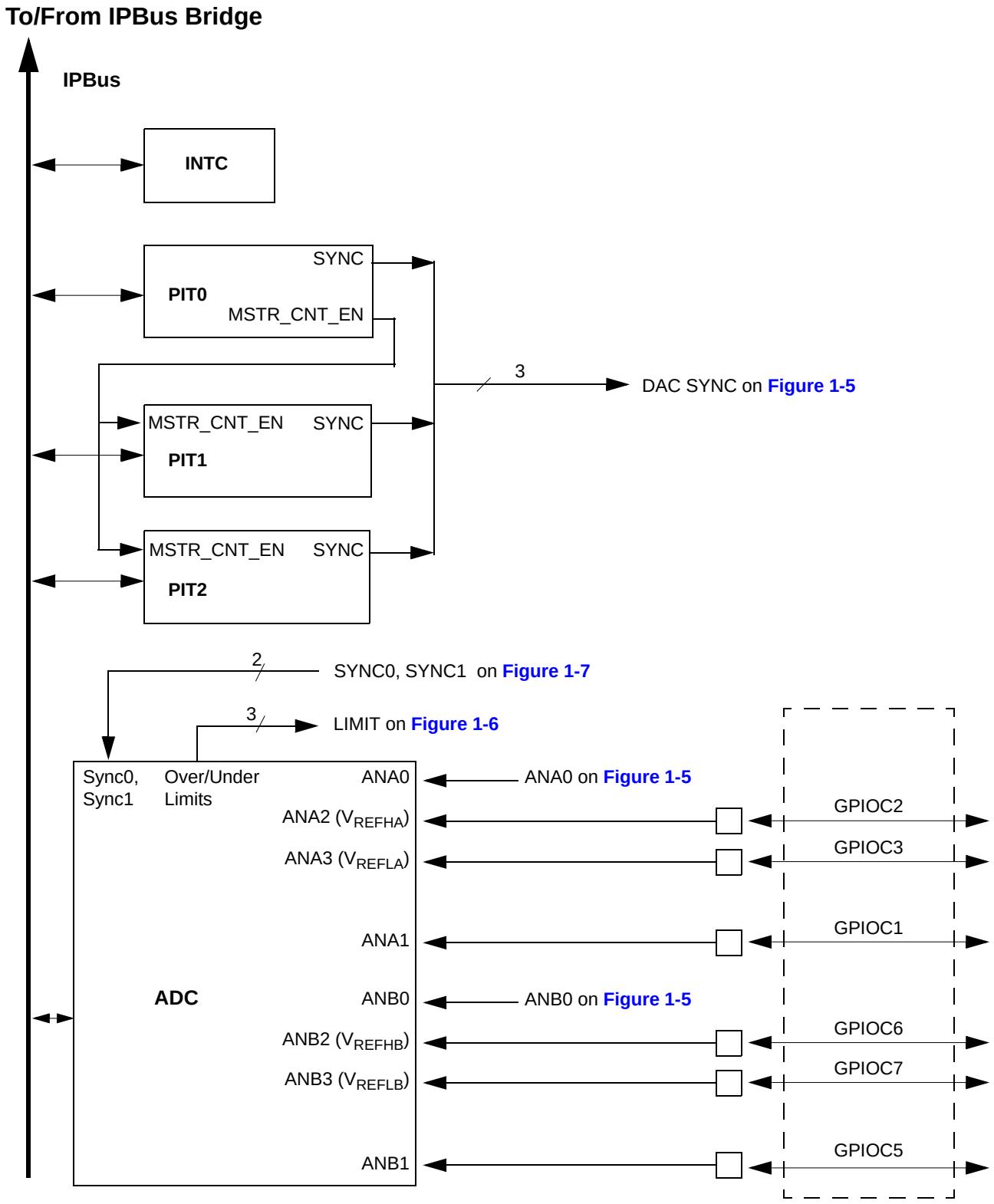


**Figure 1-3 56F8035/56F8025 I/O Pin-Out Muxing (Part 1/5)**

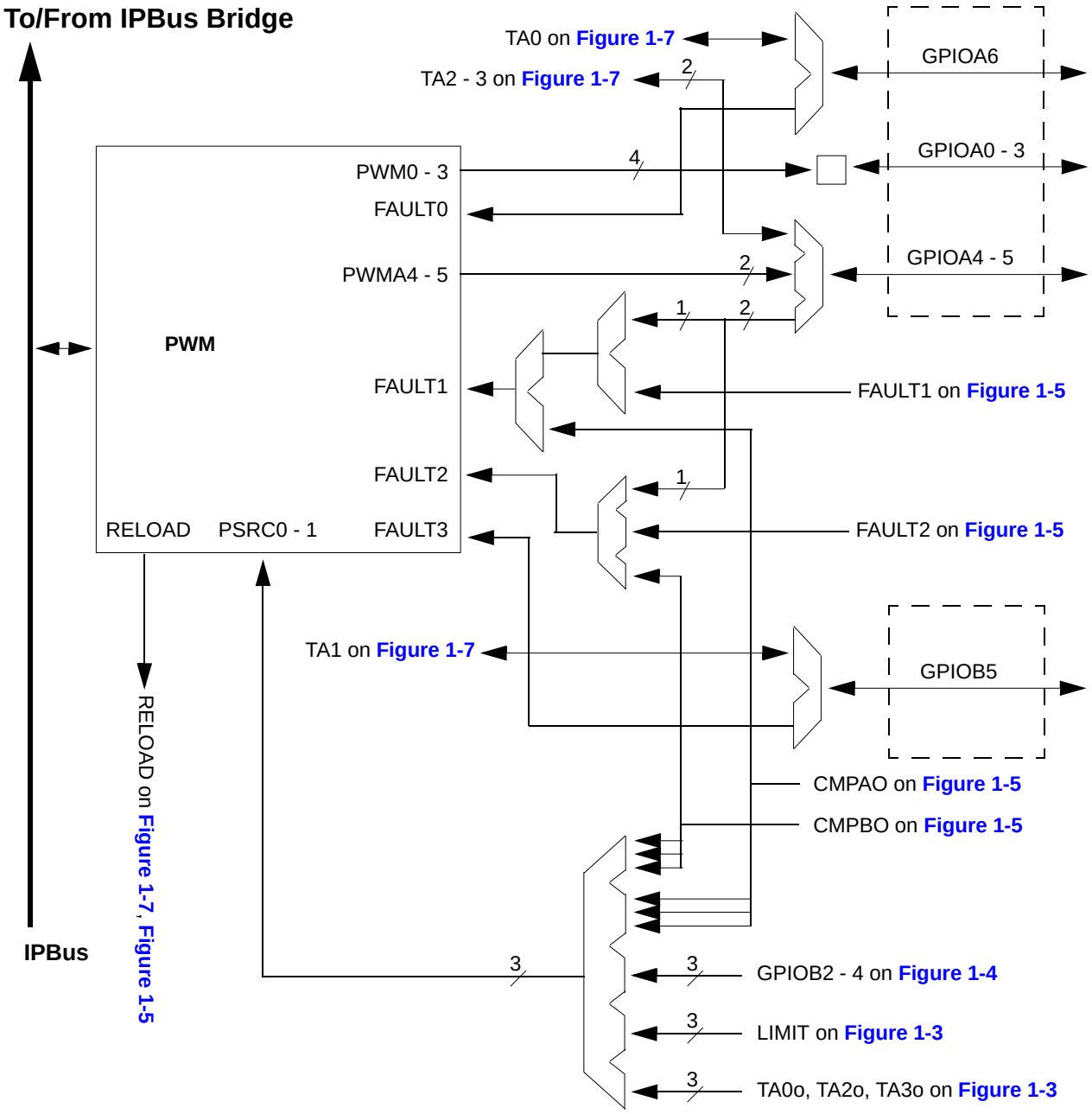


**Figure 1-6 56F8035/56F8025 I/O Pin-Out Muxing (Part 4/5)**

## Table 2-3 56F8035/56F8025 Signal and Package Information for the 44-Pin LQFP

| Signal Name | LQFP Pin No. | Type | State During Reset | Signal Description |
|---|---|---|---|---|
| **GPIOA10**<br><br>**(CMPAI2)** | 25 | Input/ Output<br><br>Input | Input, internal pull-up enabled | **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.<br><br>**Comparator A, Input 2** — This is an analog input to Comparator A.<br><br>After reset, the default state is GPIOA10. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**. |
| **GPIOA11**<br><br>**(CMPBI2)** | 6 | Input/ Output<br><br>Input | Input, internal pull-up enabled | **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.<br><br>**Comparator B, Input 2** — This is an analog input to Comparator B.<br><br>After reset, the default state is GPIOA11. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**. |
| **GPIOB0**<br><br>**(SCLK0)**<br><br>**(SCL[5])** | 30 | Input/ Output<br><br>Input/ Output<br><br>Input/ Output | Input, internal pull-up enabled | **Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.<br><br>**QSPI0 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. A Schmitt trigger input is used for noise immunity.<br><br>**Serial Clock** — This pin serves as the $I^2C$ serial clock.<br><br>After reset, the default state is GPIOB0. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**. |
| [5]The SCL signal is also brought out on the GPIOB7 pin. | | | | |
| **GPIOB1**<br><br>**($\overline{SS0}$)**<br><br>**(SDA[6])** | 2 | Input/ Output<br><br>Input/ Output<br><br>Input | Input, internal pull-up enabled | **Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.<br><br>**QSPI0 Slave Select** — $\overline{SS}$ is used in slave mode to indicate to the QSPI0 module that the current transfer is to be received.<br><br>**Serial Data** — This pin serves as the $I^2C$ serial data line.<br><br>After reset, the default state is GPIOB1. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**. |
| [6]The SDA signal is also brought out on the GPIOB6 pin. | | | | |

**Return to Table 2-2**

## Table 2-3 56F8035/56F8025 Signal and Package Information for the 44-Pin LQFP

| Signal Name | LQFP Pin No. | Type | State During Reset | Signal Description |
|---|---|---|---|---|
| **TDO**<br><br>**(GPIOD1)** | 44 | Output<br><br>Input/ Output | Output tri-stated, internal pull-up enabled | **Test Data Output** — This tri-stateable output pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and changes on the falling edge of TCK.<br><br>**Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin.<br><br>After reset, the default state is TDO. |
| **TCK**<br><br>**(GPIOD2)** | 19 | Input<br><br>Input/ Output | Input, internal pull-up enabled | **Test Clock Input** — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pull-up resistor. A Schmitt trigger input is used for noise immunity.<br><br>**Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin.<br><br>After reset, the default state is TCK. |
| **TMS**<br><br>**(GPIOD3)** | 43 | Input<br><br>Input/ Output | Input, internal pull-up enabled | **Test Mode Select Input** — This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.<br><br>**Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin.<br><br>After reset, the default state is TMS.<br><br>**Note:** Always tie the TMS pin to $V_{DD}$ through a 2.2K resistor. |

**Return to Table 2-2**

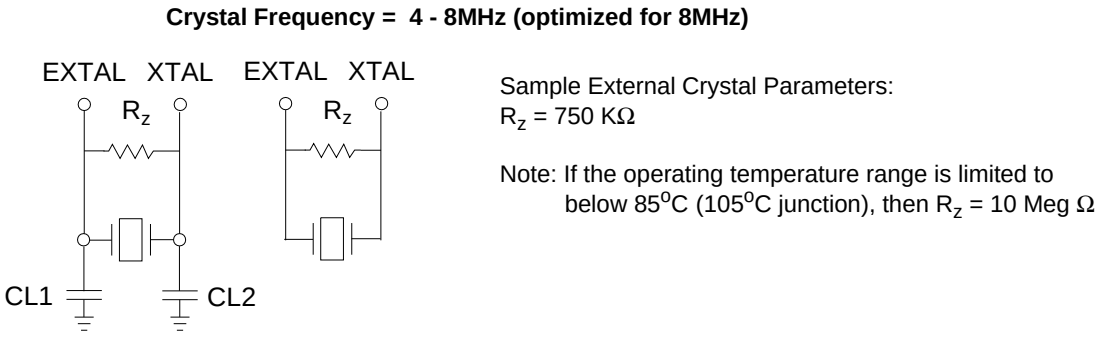


**Figure 3-1 External Crystal Oscillator Circuit**

## 3.6 Ceramic Resonator

The internal crystal oscillator circuit is also designed to interface with a ceramic resonator in the frequency range of 4-8MHz. **Figure 3-2** shows the typical 2- and 3-terminal ceramic resonators and their circuits. Follow the resonator supplier's recommendations when selecting a resonator, since their parameters determine the component values required to provide maximum stability and reliable start up. The load capacitance values used in the resonator circuit design should include all stray layout capacitances. The resonator and associated components should be mounted as near as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time.

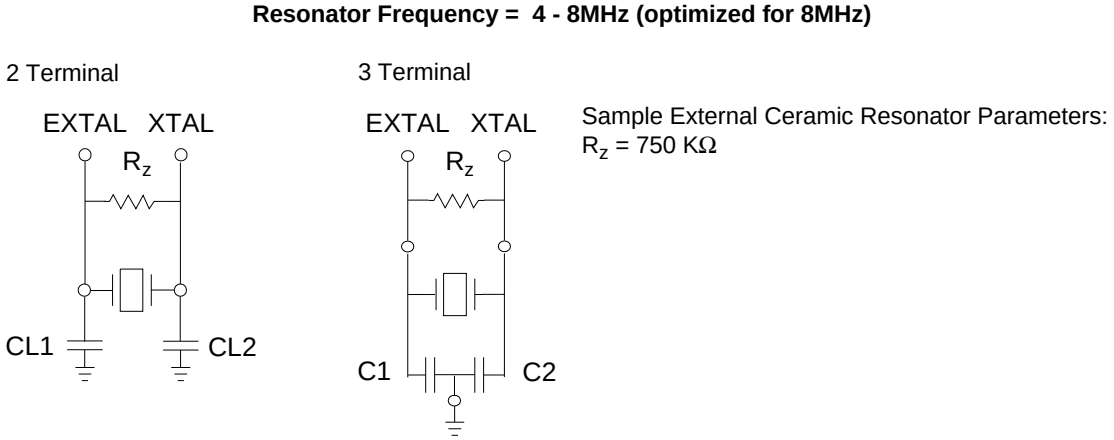


**Figure 3-2 External Ceramic Resonator Circuit**

## 3.7 External Clock Input - Crystal Oscillator Option

The recommended method of connecting an external clock is illustrated in **Figure 3-3.** The external clock source is connected to XTAL and the EXTAL pin is grounded. The external clock input must be generated using a relatively low impedance driver.

## Table 4-5 Data Memory Map[1] for 56F8035 (Continued)

| Begin/End Address | Memory Allocation |
|---|---|
| X:$00 FFFF<br>X:$00 F000 | On-Chip Peripherals<br>4096 locations allocated |
| X:$00 EFFF<br>X:$00 8800 | RESERVED |
| X:$00 87FF<br>X:$00 8000 | RESERVED |
| X:$00 7FFF<br>X:$00 1000 | RESERVED |
| X:$00 0FFF<br>X:$00 0000 | On-Chip Data RAM<br>8KB[2] |

1. All addresses are 16-bit Word addresses.
2. This RAM is shared with Program space starting at P: $00 8000; see **Figure 4-1**.

## Table 4-6 Data Memory Map[1] for 56F8025

| Begin/End Address | Memory Allocation |
|---|---|
| X:$FF FFFF<br>X:$FF FF00 | EOnCE<br>256 locations allocated |
| X:$FF FEFF<br>X:$01 0000 | RESERVED |
| X:$00 FFFF<br>X:$00 F000 | On-Chip Peripherals<br>4096 locations allocated |
| X:$00 EFFF<br>X:$00 8800 | RESERVED |
| X:$00 87FF<br>X:$00 8000 | RESERVED |
| X:$00 7FFF<br>X:$00 0800 | RESERVED |
| X:$00 07FF<br>X:$00 0000 | On-Chip Data RAM[2]<br>4KB |

1. All addresses are 16-bit Word addresses.
2. This RAM is shared with Program space starting at P: $00 8000; see **Figure 4-2**.

## Table 4-8 Data Memory Peripheral Base Address Map Summary (Continued)

| Peripheral | Prefix | Base Address | Table Number |
|---|---|---|---|
| ADC | ADC | X:$00 F080 | 4-10 |
| PWM | PWM | X:$00 F0C0 | 4-11 |
| ITCN | ITCN | X:$00 F0E0 | 4-12 |
| SIM | SIM | X:$00 F100 | 4-13 |
| COP | COP | X:$00 F120 | 4-14 |
| CLK, PLL, OSC | OCCS | X:$00 F130 | 4-15 |
| Power Supervisor | PS | X:$00 F140 | 4-16 |
| GPIO Port A | GPIOA | X:$00 F150 | 4-17 |
| GPIO Port B | GPIOB | X:$00 F160 | 4-18 |
| GPIO Port C | GPIOC | X:$00 F170 | 4-19 |
| GPIO Port D | GPIOD | X:$00 F180 | 4-20 |
| PIT 0 | PIT0 | X:$00 F190 | 4-21 |
| PIT 1 | PIT1 | X:$00 F1A0 | 4-22 |
| PIT 2 | PIT2 | X:$00 F1B0 | 4-23 |
| DAC 0 | DAC0 | X:$00 F1C0 | 4-24 |
| DAC 1 | DAC1 | X:$00 F1D0 | 4-25 |
| Comparator A | CMPA | X:$00 F1E0 | 4-26 |
| Comparator B | CMPB | X:$00 F1F0 | 4-27 |
| QSCI 0 | SCI0 | X:$00 F200 | 4-28 |
| QSPI 0 | SPI0 | X:$00 F220 | 4-29 |
| $I^2C$ | I2C | X:$00 F280 | 4-30 |
| FM | FM | X:$00 F400 | 4-31 |

## Table 4-9 Quad Timer A Registers Address Map (TMRA_BASE = $00 F000)

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| TMRA0_COMP1 | $0 | Compare Register 1 |
| TMRA0_COMP2 | $1 | Compare Register 2 |
| TMRA0_CAPT | $2 | Capture Register |
| TMRA0_LOAD | $3 | Load Register |
| TMRA0_HOLD | $4 | Hold Register |
| TMRA0_CNTR | $5 | Counter Register |
| TMRA0_CTRL | $6 | Control Register |
| TMRA0_SCTRL | $7 | Status and Control Register |
| TMRA0_CMPLD1 | $8 | Comparator Load Register 1 |
| TMRA0_CMPLD2 | $9 | Comparator Load Register 2 |
| TMRA0_CSCTRL | $A | Comparator Status and Control Register |
| TMRA0_FILT | $B | Input Filter Register |
| | | Reserved |

**Table 4-13 SIM Registers Address Map (Continued)**
**(SIM_BASE = $00 F100)**

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| SIM_IPS2 | $1A | Internal Peripheral Source Select Register 2 for TMRA |
| | | Reserved |

**Table 4-14 Computer Operating Properly Registers Address Map**
**(COP_BASE = $00 F120)**

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| COP_CTRL | $0 | Control Register |
| COP_TOUT | $1 | Time-Out Register |
| COP_CNTR | $2 | Counter Register |

**Table 4-15 Clock Generation Module Registers Address Map**
**(OCCS_BASE = $00 F130)**

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| OCCS_CTRL | $0 | Control Register |
| OCCS_DIVBY | $1 | Divide-By Register |
| OCCS_STAT | $2 | Status Register |
| | | Reserved |
| OCCS_OCTRL | $5 | Oscillator Control Register |
| OCCS_CLKCHK | $6 | Clock Check Register |
| OCCS_PROT | $7 | Protection Register |

**Table 4-16 Power Supervisor Registers Address Map**
**(PS_BASE = $00 F140)**

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| PS_CTRL | $0 | Control Register |
| PS_STAT | $1 | Status Register |
| | | Reserved |

## Table 4-20 GPIOD Registers Address Map (GPIOD_BASE = $00 F180)

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| GPIOD_PUPEN | $0 | Pull-up Enable Register |
| GPIOD_DATA | $1 | Data Register |
| GPIOD_DDIR | $2 | Data Direction Register |
| GPIOD_PEREN | $3 | Peripheral Enable Register |
| GPIOD_IASSRT | $4 | Interrupt Assert Register |
| GPIOD_IEN | $5 | Interrupt Enable Register |
| GPIOD_IEPOL | $6 | Interrupt Edge Polarity Register |
| GPIOD_IPEND | $7 | Interrupt Pending Register |
| GPIOD_IEDGE | $8 | Interrupt Edge-Sensitive Register |
| GPIOD_PPOUTM | $9 | Push-Pull Output Mode Control Register |
| GPIOD_RDATA | $A | Raw Data Input Register |
| GPIOD_DRIVE | $B | Output Drive Strength Control Register |

## Table 4-21 Programmable Interval Timer 0 Registers Address Map (PIT0_BASE = $00 F190)

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| PIT0_CTRL | $0 | Control Register |
| PIT0_MOD | $1 | Modulo Register |
| PIT0_CNTR | $2 | Counter Register |

## Table 4-22 Programmable Interval Timer 1 Registers Address Map (PIT1_BASE = $00 F1A0)

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| PIT1_CTRL | $0 | Control Register |
| PIT1_MOD | $1 | Modulo Register |
| PIT1_CNTR | $2 | Counter Register |

## Table 4-23 Programmable Interval Timer 2 Registers Address Map (PIT2_BASE = $00 F1B0)

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| PIT2_CTRL | $0 | Control Register |

## 5.6.2 Interrupt Priority Register 1 (IPR1)

| Base + $1 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read | GPIOD IPL | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FM_CBE IPL | | FM_CC IPL | | FM_ERR IPL | |
| Write | | | | | | | | | | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 5-4 Interrupt Priority Register 1 (IPR1)**

### 5.6.2.1 GPIOD Interrupt Priority Level (GPIOD IPL)—Bits 15–14

This field is used to set the interrupt priority level for the GPIOD IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

### 5.6.2.2 Reserved—Bits 13–6

This bit field is reserved. Each bit must be set to 0.

### 5.6.2.3 FM Command, Data, Address Buffers Empty Interrupt Priority Level (FM_CBE IPL)—Bits 5–4

This field is used to set the interrupt priority level for the FM Command, Data Address Buffers Empty IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

### 5.6.2.4 FM Command Complete Interrupt Priority Level (FM_CC IPL)—Bits 3–2

This field is used to set the interrupt priority level for the FM Command Complete IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

## 5.6.8 Vector Base Address Register (VBA)

| Base + $7 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read | 0 | 0 | VECTOR_BASE_ADDRESS | | | | | | | | | | | | | |
| Write | | | | | | | | | | | | | | | | |
| RESET[1] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

1. The 56F8035 resets to a value of 0 x 0000. This corresponds to reset addresses of 0 x 000000.
The 56F8025 resets to a value of 0 x 0080. This corresponds to reset addresses of 0 x 004000.

**Figure 5-10 Vector Base Address Register (VBA)**

### 5.6.8.1 Reserved—Bits 15–14

This bit field is reserved. Each bit must be set to 0.

### 5.6.8.2 Vector Address Bus (VAB) Bits 13–0

The value in this register is used as the upper 14 bits of the interrupt vector VAB[20:0]. The lower 7 bits are determined based on the highest priority interrupt and are then appended onto VBA before presenting the full VAB to the Core.

## 5.6.9 Fast Interrupt Match 0 Register (FIM0)

| Base + $8 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FAST INTERRUPT 0 | | | | | |
| Write | | | | | | | | | | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 5-11 Fast Interrupt Match 0 Register (FIM0)**

### 5.6.9.1 Reserved—Bits 15–6

This bit field is reserved. Each bit must be set to 0.

### 5.6.9.2 Fast Interrupt 0 Vector Number (FAST INTERRUPT 0)—Bits 5–0

These values determine which IRQ will be Fast Interrupt 0. Fast Interrupts vector directly to a service routine based on values in the Fast Interrupt Vector Address registers without having to go to a jump table first. IRQs used as Fast Interrupts *must* be set to priority level 2. Unexpected results will occur if a Fast Interrupt vector is set to any other priority. A Fast Interrupt automatically becomes the highest-priority level 2 interrupt regardless of its location in the interrupt table prior to being declared as Fast Interrupt. Fast Interrupt 0 has priority over Fast Interrupt 1. To determine the vector number of each IRQ, refer to the vector table.

### 6.3.6 SIM Power Control Register (SIM_PWR)

This register controls the Standby mode of the large on-chip regulator. The large on-chip regulator derives the core digital logic power supply from the IO power supply. At a system bus frequency of 200kHz, the large regulator may be put in a reduced-power standby mode without interfering with device operation to reduce device power consumption. Refer to the overview of power-down modes and the overview of clock generation for more information on the use of large regulator standby.

| Base + $8 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LRSTDBY | |
| Write | | | | | | | | | | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-7 SIM Power Control Register (SIM_PWR)**

#### 6.3.6.1 Reserved—Bits 15–2

This bit field is reserved. Each bit must be set to 0.

#### 6.3.6.2 Large Regulator Standby Mode (LRSTDBY)—Bits 1–0

- 00 = Large regulator is in Normal mode
- 01 = Large regulator is in Standby (reduced-power) mode
- 10 = Large regulator is in Normal mode and the LRSTDBY field is write-protected until the next reset
- 11 = Large regulator is in Standby mode and the LRSTDBY field is write-protected until the next reset

### 6.3.7 Clock Output Select Register (SIM_CLKOUT)

The Clock Output Select register can be used to multiplex out selected clock sources generated inside the clock generation and SIM modules onto the muxed clock output pins. All functionality is for test purposes only. Glitches may be produced when the clock is enabled or switched. The delay from the clock source to the output is unspecified. The observability of the clock output signals at output pads is subject to the frequency limitations of the associated IO cell.

GPIOA[3:0] can function as GPIO, PWM, or as clock output pins. If GPIOA[3:0] are programmed to operate as peripheral outputs, then the choice is between PWM and clock outputs. The default state is for the peripheral function of GPIOA[3:0] to be programmed as PWM (selected by bits [9:6] of the Clock Output Select register).

See **Figure 6-8** for details.

| Base + $A | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read | 0 | 0 | 0 | 0 | 0 | 0 | $\overline{\text{PWM3}}$ | $\overline{\text{PWM2}}$ | $\overline{\text{PWM1}}$ | $\overline{\text{PWM0}}$ | 1 | 0 | 0 | 0 | 0 | 0 |
| Write | | | | | | | | | | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-8 CLKO Select Register (SIM_CLKOUT)**

- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

#### 6.3.11.5 Reserved—Bit 11

This bit field is reserved. It must be set to 0.

#### 6.3.11.6 Analog-to-Digital Converter Clock Stop Disable (ADC_SD)—Bit 10

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

#### 6.3.11.7 Reserved—Bits 9–7

This bit field is reserved. Each bit must be set to 0.

#### 6.3.11.8 Inter-Integrated Circuit Clock Stop Disable (I2C_SD)—Bit 6

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

#### 6.3.11.9 Reserved—Bit 5

This bit field is reserved. It must be set to 0.

#### 6.3.11.10 QSCI0 Clock Stop Disable (QSCI0_SD)—Bit 4

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

#### 6.3.11.11 Reserved—Bit 3

This bit field is reserved. It must be set to 0.

#### 6.3.11.12 QSPI0 Clock Stop Disable (QSPI0_SD)—Bit 2

Each bit controls clocks to the indicated peripheral.

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

#### 6.3.11.13 Reserved—Bit 1

This bit field is reserved. It must be set to 0.

#### 6.3.11.14 PWM Clock Stop Disable (PWM_SD)—Bit 0

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

- 0 = XTAL - External Crystal Oscillator Output (default)
- 1 = CLKIN - External Clock Input

#### 6.3.20.3 Reserved—Bits 11–0

This bit field is reserved. Each bit must be set to 0.

### 6.3.21 Internal Peripheral Source Select Register 0 for Pulse Width Modulator (SIM_IPS0)

The internal integration of peripherals provides input signal source selection for peripherals where an input signal to a peripheral can be fed from one of several sources. These registers are organized by peripheral type and provide a selection list for every peripheral input signal that has more than one alternative source to indicate which source is selected.

If one of the alternative sources is GPIO, the setting in these registers must be made consistently with the settings in the GPS*n* and GPIO*x*_PEREN registers. Specifically, when an IPS*n* field is configured to select an I/O pin as the source, then GPS*n* register settings must configure only one I/O pin to feed this peripheral input function. Also, the GPIO*x*_PEREN bit for that I/O pin must be set to 1 to enable peripheral control of the I/O.

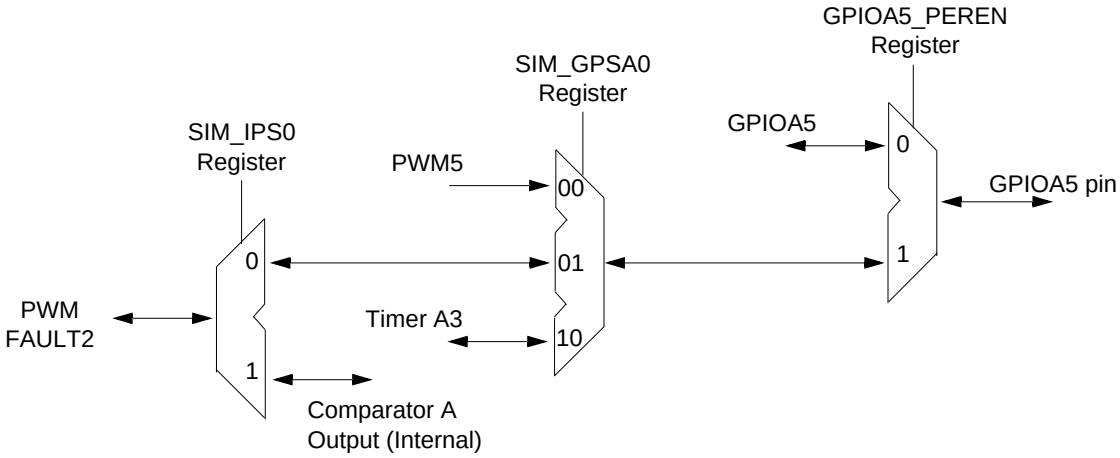


**Figure 6-24 Overall Control of Signal Source using SIM_IPS*n* Control**

IPS*n* settings should not be altered while an affected peripheral is in an enabled (operational) configuration. See the **56F802x and 56F803x Peripheral Reference Manual** for details.

master clock by two and gates it with appropriate power mode and clock gating controls. A 3X system high-speed peripheral clock input from OCCS operates at three times the system clock at a maximum of 96MHz and can be an optional clock for PWM, Timer A, Timer B, and $I^2C$ modules. These clocks are generated by gating the 3X system high-speed peripheral clock with appropriate power mode and clock gating controls.

The OCCS configuration controls the operating frequency of the SIM's master clocks. In the OCCS, either an external clock (CLKIN), a crystal oscillator, or the relaxation oscillator can be selected as the master clock source (MSTR_OSC). An external clock can be operated at any frequency up to 64MHz. The crystal oscillator can be operated only at a maximum of 8MHz. The relaxation oscillator can be operated at full speed (8MHz), standby speed (200kHz using ROSB), or powered down (using ROPD). An 8MHz MSTR_OSC can be multiplied to 196MHz using the PLL and postscaled to provide a variety of high-speed clock rates. Either the postscaled PLL output or MSTR_OSC signal can be selected to produce the master clocks to the SIM. When the PLL is selected, both the 3X system clock and the 2X system clock are enabled. If the PLL is not selected, the 3X system clock is disabled and the master clock is MSTR_OSC.

In combination with the OCCS module, the SIM provides power modes (see **Section 6.5**), clock enables, and clock rate controls to provide flexible control of clocking and power utilization. The clock rate controls enable the high-speed clocking option for the two quad timers (TMRA and TMRB) and PWM, but requires the PLL to be on and selected. Refer to the **56F802x and 56F803x Peripheral Reference Manual** for further details. The peripheral clock enable controls can be used to disable an individual peripheral clock when it is not used.

## Table 8-2 GPIO External Signals Map

| GPIO Function | Peripheral Function | LQFP Package Pin | Notes |
|---|---|---|---|
| GPIOA0 | PWM0 | 40 | Defaults to A0 |
| GPIOA1 | PWM1 | 39 | Defaults to A1 |
| GPIOA2 | PWM2 | 32 | Defaults to A2 |
| GPIOA3 | PWM3 | 33 | Defaults to A3 |
| GPIOA4 | PWM4 / TA2 / FAULT1 | 31 | SIM register SIM_GPS is used to select between PWM4, TA2, and FAULT1.<br>Defaults to A4 |
| GPIOA5 | PWM5 / TA3 / FAULT2 | 27 | SIM register SIM_GPS is used to select between PWM5, TA3, and FAULT2.<br>Defaults to A5 |
| GPIOA6 | FAULT0 / TA0 | 24 | SIM register SIM_GPS is used to select between FAULT0 and TA0.<br>Defaults to A6 |
| GPIOA7 | $\overline{\text{RESET}}$ | 21 | Defaults to $\overline{\text{RESET}}$ |
| GPIOA8 | FAULT1 / TA2 / CMPAI1 | 26 | SIM register SIM_GPS is used to select between FAULT1, TA2, and CMPAI1.<br>Defaults to A8 |
| GPIOA9 | FAULT2 / TA3 / CMPBI1 | 5 | SIM register SIM_GPS is used to select between FAULT2, TA3, and CMPBI1.<br>Defaults to A9 |
| GPIOA10 | CMPAI2 | 25 | Defaults to A10 |
| GPIOA11 | CMPBI2 | 6 | Defaults to A11 |
| GPIOB0 | SCLK0 / SCL | 30 | SIM register SIM_GPS is used to select between SCLK and SCL.<br>Defaults to B0 |
| GPIOB1 | $\overline{\text{SS0}}$ / SDA | 2 | SIM register SIM_GPS is used to select between $\overline{\text{SS0}}$ and SDA.<br>Defaults to B1 |
| GPIOB2 | MISO0 / TA2 / PSRC0 | 23 | SIM register SIM_GPS is used to select between MISO0, TA2, and PSRC0.<br>Defaults to B2 |

| Add. Offset | Register Acronym | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $0 | GPIOA_PUPEN | R | 0 | 0 | 0 | 0 | PU[15:0] | | | | | | | | | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| $1 | GPIOA_DATA | R | .0 | .0 | .0 | .0 | D[15:0] | | | | | | | | | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $2 | GPIOA_DDIR | R | .0. | .0. | .0. | .0. | DD[15:0] | | | | | | | | | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $3 | GPIOA_PEREN | R | 0 | 0 | 0 | 0 | PE[15:0] | | | | | | | | | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $4 | GPIOA_IASSRT | R | 0 | 0 | 0 | 0 | IA[15:0] | | | | | | | | | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $5 | GPIOA_IEN | R | 0 | 0 | 0 | 0 | IEN[15:0] | | | | | | | | | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $6 | GPIOA_IEPOL | R | 0 | 0 | 0 | 0 | IEPOL[15:0] | | | | | | | | | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $7 | GPIOA_IPEND | R | 0 | 0 | 0 | 0 | IPR[15:0] | | | | | | | | | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $8 | GPIOA_IEDGE | R | 0 | 0 | 0 | 0 | IES[15:0] | | | | | | | | | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $9 | GPIOA_PPOUTM | R | 0 | 0 | 0 | 0 | OEN[15:0] | | | | | | | | | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| $A | GPIOA_RDATA | R | 0 | 0 | 0 | 0 | RAW DATA[15:0] | | | | | | | | | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| $B | GPIOA_DRIVE | R | 0 | 0 | 0 | 0 | DRIVE[15:0] | | | | | | | | | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| R | 0 | Read as 0 |
| W | | Reserved |
| RS | | Reset |

**Figure 8-1 GPIOA Register Map Summary**

| Add. Offset | Register Acronym | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $0 | GPIOB_PUPEN | R | 0 | 0 | 0 | 0 | PU[15:0] | | 0 | 0 | PU | | | 0 | PU | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| $1 | GPIOB_DATA | R | 0 | 0 | 0 | 0 | D[15:0] | | 0 | 0 | D | | | 0 | D | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $2 | GPIOB_DDIR | R | 0 | 0 | 0 | 0 | DD[15:0] | | 0 | 0 | DD | | | 0 | DD | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $3 | GPIOB_PEREN | R | 0 | 0 | 0 | 0 | PE[15:0] | | 0 | 0 | PE | | | 0 | PE | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $4 | GPIOB_IASSRT | R | 0 | 0 | 0 | 0 | IA[15:0] | | 0 | 0 | IA | | | 0 | IA | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $5 | GPIOB_IEN | R | 0 | 0 | 0 | 0 | IEN[15:0] | | 0 | 0 | IEN | | | 0 | IEN | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $6 | GPIOB_IEPOL | R | 0 | 0 | 0 | 0 | IEPOL[15:0] | | 0 | 0 | IEPOL | | | 0 | IEPOL | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $7 | GPIOB_IPEND | R | 0 | 0 | 0 | 0 | IPR[15:0] | | 0 | 0 | IPR | | | 0 | IPR | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $8 | GPIOB_IEDGE | R | 0 | 0 | 0 | 0 | IES[15:0] | | 0 | 0 | IES | | | 0 | IES | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $9 | GPIOB_PPOUTM | R | 0 | 0 | 0 | 0 | OEN[15:0] | | 0 | 0 | OEN | | | 0 | OEN | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| $A | GPIOB_RDATA | R | 0 | 0 | 0 | 0 | RAW DATA[15:0] | | 0 | 0 | RAW DATA | | | 0 | RAW DATA | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| $B | GPIOB_DRIVE | R | 0 | 0 | 0 | 0 | DRIVE[15:0] | | 0 | 0 | DRIVE | | | 0 | DRIVE | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| R | 0 | Read as 0 |
| W | | Reserved |
| RS | | Reset |

**Figure 8-2 GPIOB Register Map Summary**

## 10.2 DC Electrical Characteristics

**Table 10-5 DC Electrical Characteristics**
At Recommended Operating Conditions

| Characteristic | Symbol | Notes | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Output Voltage High | $V_{OH}$ | Pin Group 1 | 2.4 | — | — | V | $I_{OH} = I_{OHmax}$ |
| Output Voltage Low | $V_{OL}$ | Pin Groups 1, 2 | — | — | 0.4 | V | $I_{OL} = I_{OLmax}$ |
| Digital Input Current High (a)<br>pull-up enabled or disabled | $I_{IH}$ | Pin Groups 1, 2 | — | 0 | +/- 2.5 | µA | $V_{IN}$ = 2.4V to 5.5V |
| Comparator Input Current High | $I_{IHC}$ | Pin Group 3 | — | 0 | +/- 2 | µA | $V_{IN} = V_{DDA}$ |
| Oscillator Input Current High | $I_{IHOSC}$ | Pin Group 3 | — | 0 | +/- 2 | µA | $V_{IN} = V_{DDA}$ |
| Digital Input Current Low[1]<br>pull-up enabled<br>pull-up disabled | $I_{IL}$ | Pin Groups 1, 2 | <br>-15<br>— | <br>-30<br>0 | <br>-60<br>+/- 2.5 | µA | $V_{IN}$ = 0V |
| Comparator Input Current Low | $I_{ILC}$ | Pin Group 3 | — | 0 | +/- 2 | µA | $V_{IN}$ = 0V |
| Oscillator Input Current Low | $I_{ILOSC}$ | Pin Group 3 | — | 0 | +/- 2 | µA | $V_{IN}$ = 0V |
| DAC Output Voltage Range | $V_{DAC}$ | Internal | Typically $V_{SSA}$ + 40mV | — | Typically $V_{DDA}$ - 40mV | V | — |
| Output Current [1]<br>High Impedance State | $I_{OZ}$ | Pin Groups 1, 2 | — | 0 | +/- 2.5 | µA | — |
| Schmitt Trigger Input Hysteresis | $V_{HYS}$ | Pin Groups 1, 2 | — | 0.35 | — | V | — |
| Input Capacitance | $C_{IN}$ | | — | 10 | — | pF | — |
| Output Capacitance | $C_{OUT}$ | | — | 10 | — | pF | — |

1. See **Figure 10-1**

**Default Mode**

Pin Group 1: GPIO, TDI, TDO, TMS, TCK

Pin Group 2: $\overline{\text{RESET}}$, GPIOA7

Pin Group 3: ADC and Comparator Analog Inputs

Pin Group 4: XTAL, EXTAL

# 10.8 Reset, Stop, Wait, Mode Select, and Interrupt Timing

.

**Table 10-13 Reset, Stop, Wait, Mode Select, and Interrupt Timing[1,2]**

| Characteristic | Symbol | Typical Min | Typical Max | Unit | See Figure |
|---|---|---|---|---|---|
| Minimum $\overline{\text{RESET}}$ Assertion Duration | $t_{RA}$ | 4T | — | ns | — |
| Minimum GPIO pin Assertion for Interrupt | $t_{IW}$ | 2T | — | ns | 10-6 |
| $\overline{\text{RESET}}$ deassertion to First Address Fetch[3] | $t_{RDA}$ | $96T_{OSC}$ + 64T | $97T_{OSC}$ + 65T | ns | — |
| Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop) | $t_{IF}$ | — | 6T | ns | — |

1. In the formulas, T = system clock cycle and $T_{osc}$ = oscillator clock cycle. For an operating frequency of 32MHz, T = 31.25ns. At 8MHz (used during Reset and Stop modes), T = 125ns.
2. Parameters listed are guaranteed by design.
3. During Power-On Reset, it is possible to use the 56F8035/56F8025 internal reset stretching circuitry to extend this period to 2^21T.

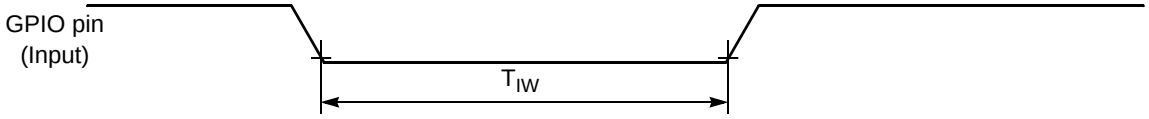


**Figure 10-6 GPIO Interrupt Timing (Negative Edge-Sensitive)**