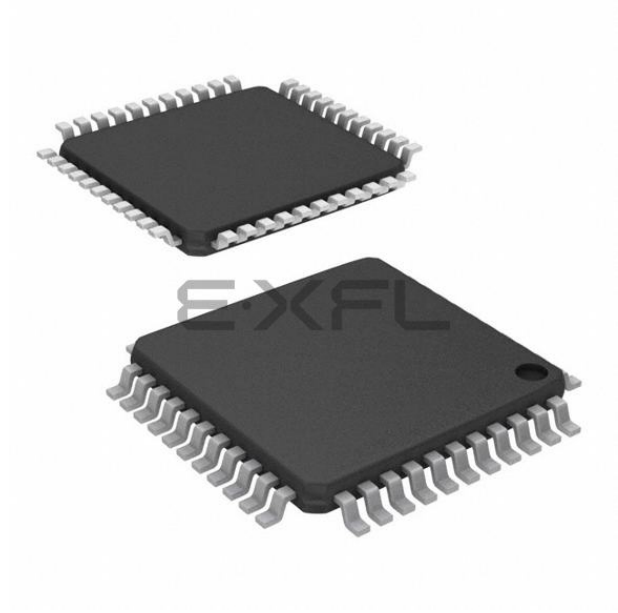

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8025vldr

Document Revision History

Version History	Description of Change
Rev. 0	Initial public release.
Rev. 1	• In Table 5-3, changed the ITCN_BASE address from $00 F060 (incorrect value) to $00 F0E0 (the correct value). • In Table 10-4, added an entry for flash data retention with less than 100 program/erase cycles (minimum 20 years). • In Table 10-6, changed the device clock speed in STOP mode from 8MHz to 4MHz. • In Table 10-12, changed the typical relaxation oscillator output frequency in Standby mode from 400kHz to 200kHz. • Changed input propagation delay values in Table 10-20 as follows: Old values: 1 µs typical, 2 µs maximum New values: 35 ns typical, 45 ns maximum
Rev. 2	• In Table 10-19, changed the maximum ADC internal clock frequency from 8MHz to 5.33MHz. • Replaced the case outline schematics in Figure 11-2, Figure 11-3, and Figure 11-4.
Rev. 3	Added the following note to the description of the TMS signal in Table 2-3: **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.
Rev. 4	• Changed the VBA register reset value and updated the footnote in **Section 5.6.8**. • Changed the STANDBY > STOP I_{DD} values in **Table 10-6** as follows: Typical: was 290µA, is 540µA Maximum: was 390µA, is 650µA • Changed the POWERDOWN I_{DD} values in **Table 10-6** as follows: Typical: was 190µA, is 440µA Maximum: was 250µA, is 550µA • Changed footnote 1 in **Table 10-12** (was “Output frequency after application of 8MHz trim value, at 125°C.”, is “Output frequency after application of factory trim”). • Deleted the text “at 125°C” from **Figure 10-5**. • Changed the maximum input offset voltage in **Table 10-20** (was +/- 20 mV, is ±35 mV).
Rev. 5	• In **Table 2-3**, change V_{CAP} value from 4.7µF to 2.2µF. • Revised **Section 7, Security Features**. • Fixed miscellaneous typos.

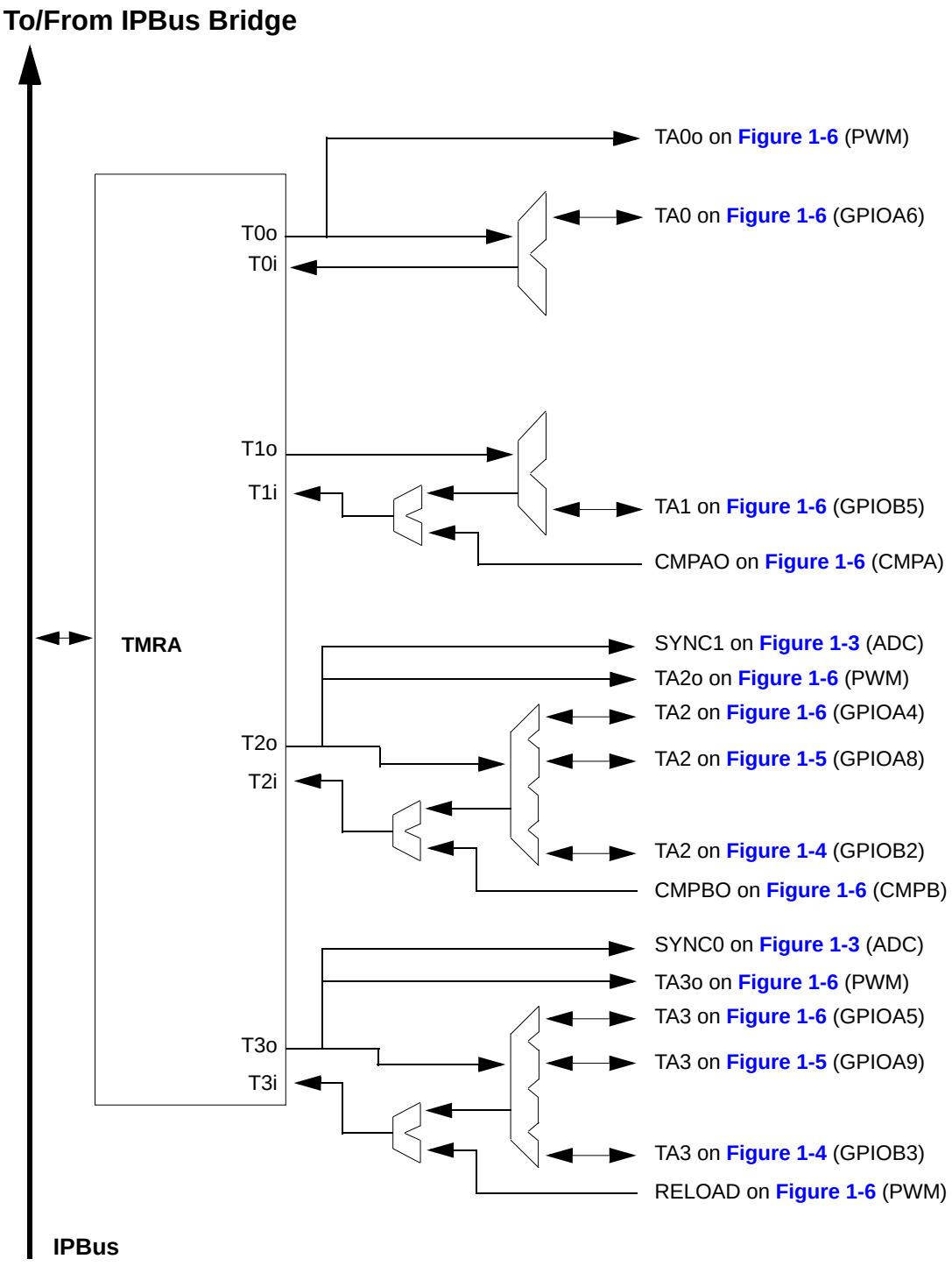


Figure 1-7 56F8035/56F8025 I/O Pin-Out Muxing (Part 5/5)

1.5 Product Documentation

The documents listed in **Table 1-2** are required for a complete description and proper design with the 56F8035/56F8025. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at:
http://www.freescale.com

Table 1-2 56F8035/56F8025 Chip Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, 16-bit Digital Signal Controller core processor, and the instruction set	DSP56800ERM
56F802x and 56F803x Peripheral Reference Manual	Detailed description of peripherals of the 56F802x and 56F803x family of devices	MC56F80xxRM
56F802x and 56F803x Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the 56F802x and 56F803x family of devices	56F80xxBLUG
56F8035/56F8025 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	MC56F8035/56F8025
56F8035/56F8025 Errata	Details any chip issues that might be present	MC56F8035/56F8025E

1.6 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
“asserted”	A high true (active high) signal is high or a low true (active low) signal is low.
“deasserted”	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:	Signal/Symbol	Logic State	Signal State	Voltage[1]
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

2.1 Introduction

The input and output signals of the 56F8035/56F8025 are organized into functional groups, as detailed in **Table 2-1**. **Table 2-2** summarizes all device pins. In **Table 2-2**, each table row describes the signal or signals present on a pin, sorted by pin number.

Table 2-1 Functional Group Pin Allocations

Functional Group	Number of Pins
Power Inputs (V_{DD}, V_{DDA})	3
Ground (V_{SS}, V_{SSA})	4
Supply Capacitors	2
Reset[1]	1
Pulse Width Modulator (PWM) Ports[1]	12
Serial Peripheral Interface (SPI) Ports[1]	4
Timer Module A (TMRA) Ports[1]	4
Analog-to-Digital Converter (ADC) Ports[1]	8
Serial Communications Interface 0 (SCI0) Ports[1]	2
Inter-Integrated Circuit Interface (I^2C) Ports[1]	2
Oscillator Signals[1]	2
JTAG/Enhanced On-Chip Emulation (EOnCE)[1]	4

1. Pins may be shared with other peripherals; see **Table 2-2**.

Table 2-2 56F8035/56F8025 Pins (Continued)

			Peripherals:										
Pin #	**Pin Name**	**Signal Name**	**GPIO**	**I2C**	**QSCI**	**QSPI**	**ADC**	**PWM**	**Quad Timer**	**Comp**	**Power & Ground**	**JTAG**	**Misc**
28	**VSS_IO**	V_{SS}									**V_{SS}**		
29	**VDD_IO**	V_{DD}									V_{DD}		
30	**GPIOB0**	GPIOB0, SCLK0, SCL	**B0**	SCL		SCLK0							
31	**GPIOA4**	GPIOA4, PWM4, TA2, FAULT1	**A4**					PWM4 FAULT1	TA2				
32	**GPIOA2**	GPIOA2, PWM2	**A2**					PWM2					
33	**GPIOA3**	GPIOA3, PWM3	**A3**					PWM3					
34	**VCAP**	V_{CAP}									**V_{CAP}**		
35	**VDD_IO**	V_{DD}									**V_{DD}**		
36	**VSS_IO**	V_{SS}									**V_{SS}**		
37	**GPIOD5**	GPIOD5, XTAL, CLKIN	**D5**										XTAL CLKIN
38	**GPIOD4**	GPIOD4, EXTAL	**D4**										EXTAL
39	**GPIOA1**	GPIOA1, PWM1	**A1**					PWM1					
40	**GPIOA0**	GPIOA0, PWM0	**A0**					PWM0					
41	**TDI**	TDI, GPIOD0	D0									**TD1**	
42	**GPIOB11**	GPIOB11, CMPBO	**B11**							CMPBO			
43	**TMS**	TMS, GPIOD3	D3									**TMS**	
44	**TDO**	TDO, GPIOD1	D1									**TDO**	

Table 2-3 56F8035/56F8025 Signal and Package Information for the 44-Pin LQFP

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOA6	24	Input/ Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(FAULT0)		Input		**Fault0** — This fault input pin is used for disabling selected PWM outputs in cases where fault conditions originate off-chip.
(TA0)				**TA0** — Timer A, Channel 0. After reset, the default state is GPIOA6. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
GPIOA8	26	Input/ Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(FAULT1)		Input		**Fault1** — This fault input pin is used for disabling selected PWM outputs in cases where fault conditions originate off-chip.
(TA2)		Input/ Output		**TA2** — Timer A, Channel 2.
(CMPAI1)		Input		**Comparator A, Input 1** — This is an analog input to Comparator A. After reset, the default state is GPIOA8. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
GPIOA9	5	Input/ Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(FAULT2)		Input		**Fault2** — This fault input pin is used for disabling selected PWM outputs in cases where fault conditions originate off-chip.
(TA3)		Input/ Output		**TA2** — Timer A, Channel 3.
(CMPBI1)		Input		**Comparator B, Input 1** — This is an analog input to Comparator B. After reset, the default state is GPIOA9. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.

Return to Table 2-2

Table 4-1 Chip Memory Configurations

On-Chip Memory	56F8035	56F8025	Use Restrictions
Program Flash (PFLASH)	32K x 16 or 64KB	16K x 16 or 32KB	Erase/Program via Flash interface unit and word writes to CDBW
Unified RAM (RAM)	4K x 16 or 8KB	2K x 16 or 4KB	Usable by both the Program and Data memory spaces

4.2 Interrupt Vector Table

Table 4-2 provides the 56F8035/56F8025's reset and interrupt priority structure, including on-chip peripherals. The table is organized with higher-priority vectors at the top and lower-priority interrupts lower in the table. As indicated, the priority of an interrupt can be assigned to different levels, allowing some control over interrupt priorities. All level 3 interrupts will be serviced before level 2, and so on. For a selected priority level, the lowest vector number has the highest priority.

The location of the vector table is determined by the Vector Base Address (VBA). Please see Section 5.6.8 for the reset value of the VBA.

By default, the chip reset address and COP reset address will correspond to vector 0 and 1 of the interrupt vector table. In these instances, the first two locations in the vector table must contain branch or JMP instructions. All other entries must contain JSR instructions.

Table 4-2 Interrupt Vector Table Contents[1]

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
core			P:$00	Reserved for Reset Overlay[2]
core			P:$02	Reserved for COP Reset Overlay
core	2	3	P:$04	Illegal Instruction
core	3	3	P:$06	SW Interrupt 3
core	4	3	P:$08	HW Stack Overflow
core	5	3	P:$0A	Misaligned Long Word Access
core	6	1-3	P:$0C	EOnCE Step Counter
core	7	1-3	P:$0E	EOnCE Breakpoint Unit
core	8	1-3	P:$10	EOnCE Trace Buffer
core	9	1-3	P:$12	EOnCE Transmit Register Empty
core	10	1-3	P:$14	EOnCE Receive Register Full
core	11	2	P:$16	SW Interrupt 2
core	12	1	P:$18	SW Interrupt 1
core	13	0	P:$1A	SW Interrupt 0
	14			Reserved
LVI	15	1-3	P:$1E	Low-Voltage Detector (Power Sense)
PLL	16	1-3	P:$20	Phase-Locked Loop

Table 4-7 EOnCE Memory Map (Continued)

Address	Register Acronym	Register Name
X:$FF FFFB - X:$FF FFA1		Reserved
X:$FF FFA0	OCR	Control Register
X:$FF FF9F		Instruction Step Counter
X:$FF FF9E	OSCNTR (24 bits)	Instruction Step Counter
X:$FF FF9D	OSR	Status Register
X:$FF FF9C	OBASE	Peripheral Base Address Register
X:$FF FF9B	OTBCR	Trace Buffer Control Register
X:$FF FF9A	OTBPR	Trace Buffer Pointer Register
X:$FF FF99		Trace Buffer Register Stages
X:$FF FF98	OTB (21 - 24 bits/stage)	Trace Buffer Register Stages
X:$FF FF97		Breakpoint Unit Control Register
X:$FF FF96	OBCR (24 bits)	Breakpoint Unit Control Register
X:$FF FF95		Breakpoint Unit Address Register 1
X:$FF FF94	OBAR1 (24 bits)	Breakpoint Unit Address Register 1
X:$FF FF93		Breakpoint Unit Address Register 2
X:$FF FF92	OBAR2 (32 bits)	Breakpoint Unit Address Register 2
X:$FF FF91		Breakpoint Unit Mask Register 2
X:$FF FF90	OBMSK (32 bits)	Breakpoint Unit Mask Register 2
X:$FF FF8F		Reserved
X:$FF FF8E	OBCNTR	EOnCE Breakpoint Unit Counter
X:$FF FF8D		Reserved
X:$FF FF8C		Reserved
X:$FF FF8B		Reserved
X:$FF FF8A	OESCR	External Signal Control Register
X:$FF FF89 - X:$FF FF00		Reserved

4.6 Peripheral Memory-Mapped Registers

On-chip peripheral registers are part of the data memory map on the 56800E series. These locations may be accessed with the same addressing modes used for ordinary Data memory, except all peripheral registers should be read or written using word accesses only.

Table 4-8 summarizes base addresses for the set of peripherals on the 56F8035/56F8025 device. Peripherals are listed in order of the base address.

The following tables list all of the peripheral registers required to control or access the peripherals.

Table 4-8 Data Memory Peripheral Base Address Map Summary

Peripheral	Prefix	Base Address	Table Number
Timer A	TMRA	X:$00 F000	4-9

Table 4-23 Programmable Interval Timer 2 Registers Address Map (Continued) (PIT2_BASE = $00 F1B0)

Register Acronym	Address Offset	Register Description
PIT2_MOD	$1	Modulo Register
PIT2_CNTR	$2	Counter Register

Table 4-24 Digital-to-Analog Converter 0 Registers Address Map (DAC0_BASE = $00 F1C0)

Register Acronym	Address Offset	Register Description
DAC0_CTRL	$0	Control Register
DAC0_DATA	$1	Data Register
DAC0_STEP	$2	Step Register
DAC0_MINVAL	$3	Minimum Value Register
DAC0_MAXVAL	$4	Maximum Value Register

Table 4-25 Digital-to-Analog Converter 0 Registers Address Map (DAC1_BASE = $00 F1D0)

Register Acronym	Address Offset	Register Description
DAC1_CTRL	$0	Control Register
DAC1_DATA	$1	Data Register
DAC1_STEP	$2	Step Register
DAC1_MINVAL	$3	Minimum Value Register
DAC1_MAXVAL	$4	Maximum Value Register

Table 4-26 Comparator A Registers Address Map (CMPA_BASE = $00 F1E0)

Register Acronym	Address Offset	Register Description
CMPA_CTRL	$0	Control Register
CMPA_STAT	$1	Status Register
CMPA_FILT	$2	Filter Register

Table 4-27 Comparator B Registers Address Map (CMPB_BASE = $00 F1F0)

Register Acronym	Address Offset	Register Description
CMPB_CTRL	$0	Control Register
CMPB_STAT	$1	Status Register

5.6.1.5 EOnCE Transmit Register Empty Interrupt Priority Level (TX_REG IPL)— Bits 7–6

This field is used to set the interrupt priority level for the EOnCE Transmit Register Empty IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.6 EOnCE Trace Buffer Interrupt Priority Level (TRBUF IPL)— Bits 5–4

This field is used to set the interrupt priority level for the EOnCE Trace Buffer IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.7 EOnCE Breakpoint Unit Interrupt Priority Level (BKPT_U IPL)— Bits 3–2

This field is used to set the interrupt priority level for the EOnCE Breakpoint Unit IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.8 EOnCE Step Counter Interrupt Priority Level (STPCNT IPL)— Bits 1–0

This field is used to set the interrupt priority level for the EOnCE Step Counter IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

Table 5-4 Interrupt Priority Encoding

IPIC_VALUE[1:0]	Current Interrupt Priority Level	Required Nested Exception Priority
00	No interrupt or SWILP	Priorities 0, 1, 2, 3
01	Priority 0	Priorities 1, 2, 3
10	Priority 1	Priorities 2, 3
11	Priority 2 or 3	Priority 3

5.6.19.3 Vector Number - Vector Address Bus (VAB)—Bits 12–6

This *read-only* field shows bits [7:1] of the Vector Address Bus used at the time the last IRQ was taken. In the case of a Fast Interrupt, it shows the lower address bits of the jump address. This field is only updated when the 56800E core jumps to a new interrupt service routine.

Note: Nested interrupts may cause this field to be updated before the original interrupt service routine can read it.

5.6.19.4 Interrupt Disable (INT_DIS)—Bit 5

This bit allows all interrupts to be disabled.

- 0 = Normal operation (default)
- 1 = All interrupts disabled

5.6.19.5 Reserved—Bits 4-2

This bit field is reserved. Each bit must be set to 1.

5.6.19.6 Reserved—Bits 1–0

This bit field is reserved. Each bit must be set to 0.

5.7 Resets

5.7.1 General

Table 5-5 Reset Summary

Reset	Priority	Source	Characteristics
Core Reset		$\overline{\text{RST}}$	Core reset from the SIM

6.3.12 Stop Disable Register 1 (SD1)

See **Section 6.3.11** for general information about Stop Disable Registers.

Base + $F	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	PIT2_SD	PIT1_SD	PIT0_SD	0	0	0	0	0	0	0	0	TA3_SD	TA2_SD	TA1_SD	TA0_SD
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-13 Stop Disable Register 1 (SD1)

6.3.12.1 Reserved—Bit 15

This bit field is reserved. It must be set to 0.

6.3.12.2 Programmable Interval Timer 2 Clock Stop Disable (PIT2_SD)—Bit 14

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE1 register

6.3.12.3 Programmable Interval Timer 1 Clock Stop Disable (PIT1_SD)—Bit 13

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE1 register

6.3.12.4 Programmable Interval Timer 0 Clock Stop Disable (PIT0_SD)—Bit 12

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE1 register

6.3.12.5 Reserved—Bits 11–4

This bit field is reserved. Each bit must be set to 0.

6.3.12.6 Quad Timer A, Channel 3 Clock Stop Disable (TA3_SD)—Bit 3

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE1 register

6.3.12.7 Quad Timer A, Channel 2 Clock Stop Disable (TA2_SD)—Bit 2

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE1 register

Table 8-2 GPIO External Signals Map (Continued)

GPIO Function	Peripheral Function	LQFP Package Pin	Notes
GPIOD0	TDI	41	Defaults to TDI
GPIOD1	TDO	44	Defaults to TDO
GPIOD2	TCK	19	Defaults to TCK
GPIOD3	TMS	43	Defaults to TMS
GPIOD4	EXTAL	38	Defaults to D4
GPIOD5	XTAL / CLKIN	37	SIM register SIM_GPSCD is used to select between XTAL and CLKIN. Defaults to D5

8.3 Reset Values

Tables **8-1** and **8-2** detail registers for the 56F8035/56F8025; Figures **8-1** through **8-4** summarize register maps and reset values.

Add. Offset	Register Acronym		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	GPIOD_PUPEN	R											PU[15:0]					
		W																
		RS	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$1	GPIOD_DATA	R											D[15:0]					
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$2	GPIOD_DDIR	R											DD[15:0]					
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$3	GPIOD_PEREN	R											PE[15:0]					
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
$4	GPIOD_IASSRT	R											IA[15:0]					
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$5	GPIOD_IEN	R											IEN[15:0]					
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$6	GPIOD_IEPOL	R											IEPOL[15:0]					
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$7	GPIOD_IPEND	R											IPR[15:0]					
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$8	GPIOD_IEDGE	R											IES[15:0]					
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$9	GPIOD_PPOUTM	R											OEN[15:0]					
		W																
		RS	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$A	GPIOD_RDATA	R											RAW DATA[15:0]					
		W																
		RS	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X
$B	GPIOD_DRIVE	R											DRIVE[15:0]					
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R	0	Read as 0
W		Reserved
RS		Reset

Figure 8-4 GPIOD Register Map Summary

10.4 Flash Memory Characteristics

Table 10-9 Flash Timing Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Program time[1]	Tprog	20	—	40	µs
Erase time [2]	Terase	20	—	—	ms
Mass erase time	Tme	100	—	—	ms

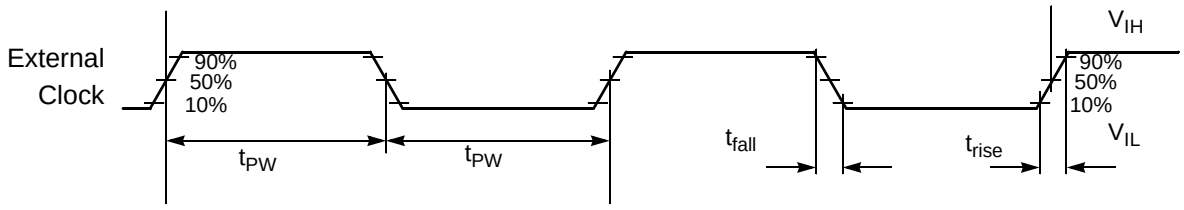
1. There is additional overhead which is part of the programming sequence. See the **56F802x and 56F803x Peripheral Reference Manual** for details.
2. Specifies page erase time. There are 512 bytes per page in the Program Flash memory.

10.5 External Clock Operation Timing

Table 10-10 External Clock Operation Timing Requirements[1]

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[2]	f_{osc}	4	8	8	MHz
Clock Pulse Width[3]	t_{PW}	6.25	—	—	ns
External Clock Input Rise Time[4]	t_{rise}	—	—	3	ns
External Clock Input Fall Time[5]	t_{fall}	—	—	3	ns

1. Parameters listed are guaranteed by design.
2. See **Figure 10-4** for details on using the recommended connection of an external clock driver.
3. The chip may not function if the high or low pulse width is smaller than 6.25ns.
4. External clock input rise time is measured from 10% to 90%.
5. External clock input fall time is measured from 90% to 10%.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 10-4 External Clock Timing

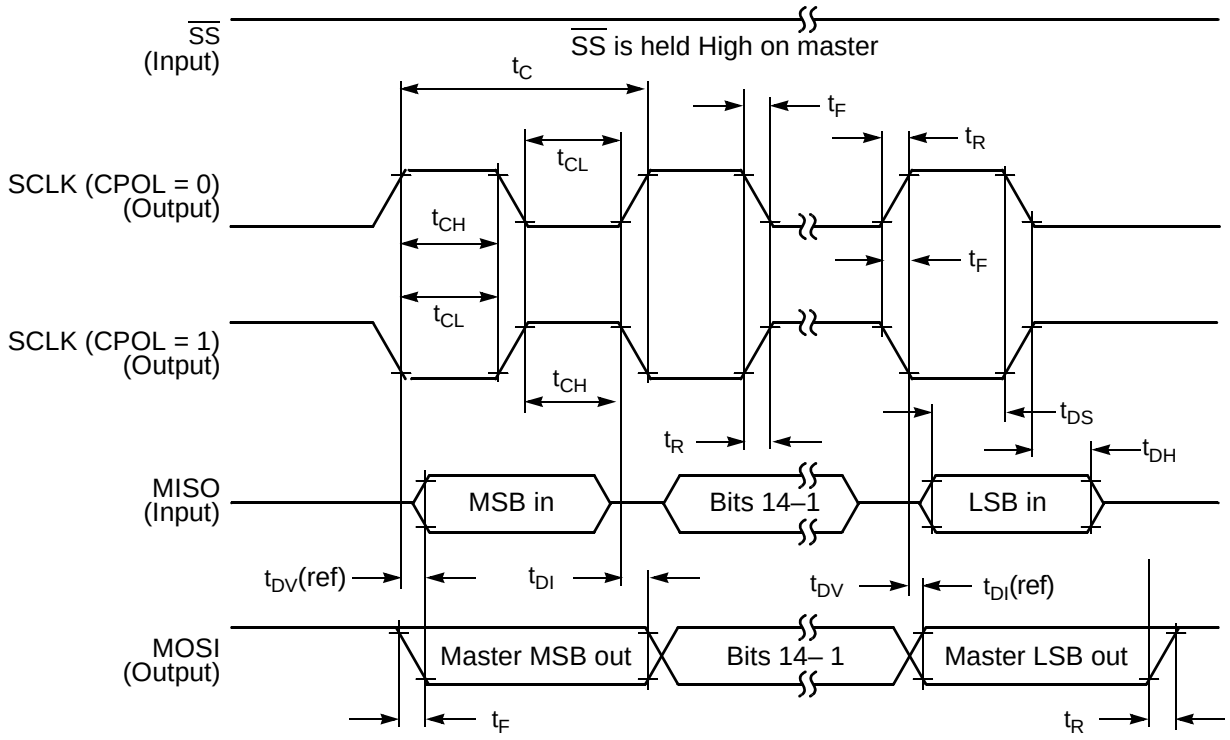


Figure 10-8 SPI Master Timing (CPHA = 1)

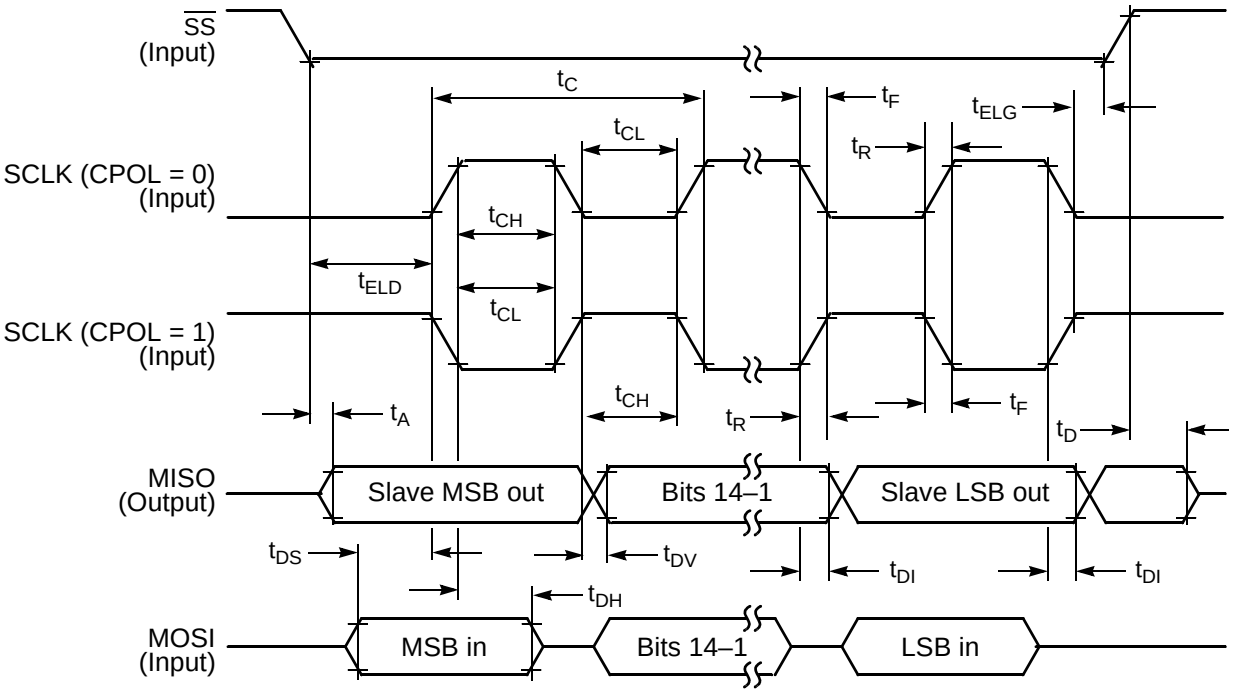


Figure 10-9 SPI Slave Timing (CPHA = 0)

10.13 JTAG Timing

Table 10-18 JTAG Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation[1]	f_{OP}	DC	SYS_CLK/8	MHz	10-15
TCK clock pulse width	t_{PW}	50	—	ns	10-15
TMS, TDI data set-up time	t_{DS}	5	—	ns	10-16
TMS, TDI data hold time	t_{DH}	5	—	ns	10-16
TCK low to TDO data valid	t_{DV}	—	30	ns	10-16
TCK low to TDO tri-state	t_{TS}	—	30	ns	10-16

1. TCK frequency of operation must be less than 1/8 the processor rate.

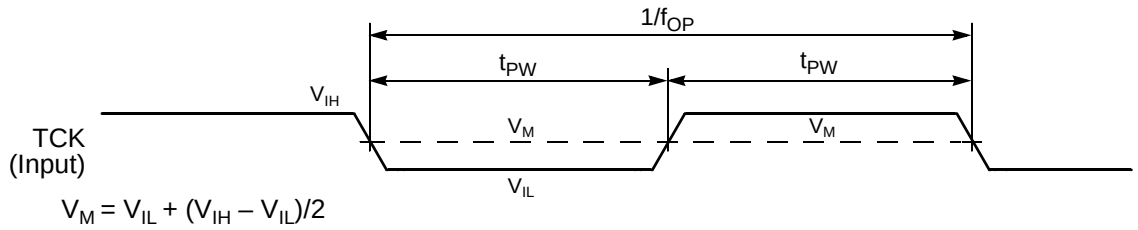


Figure 10-15 Test Clock Input Timing Diagram

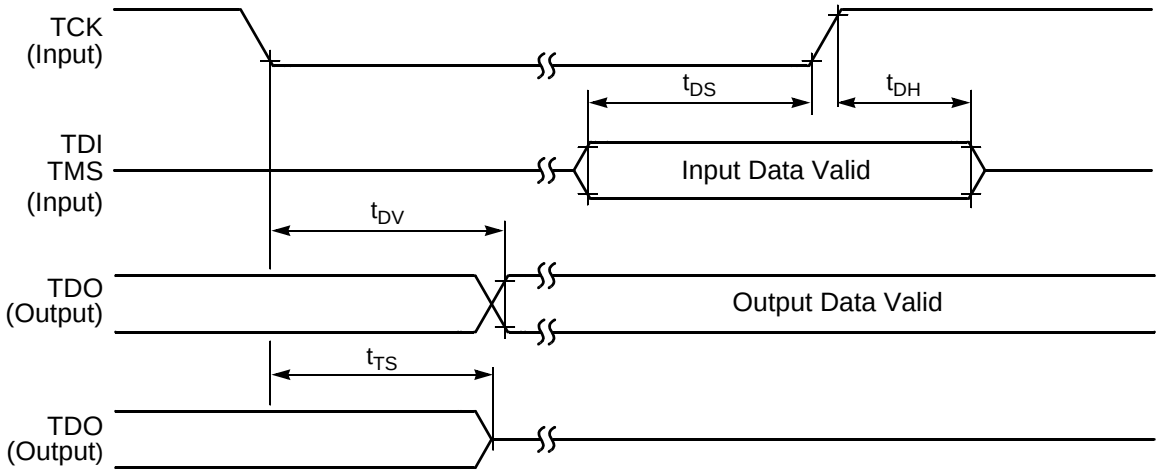


Figure 10-16 Test Access Port Timing Diagram

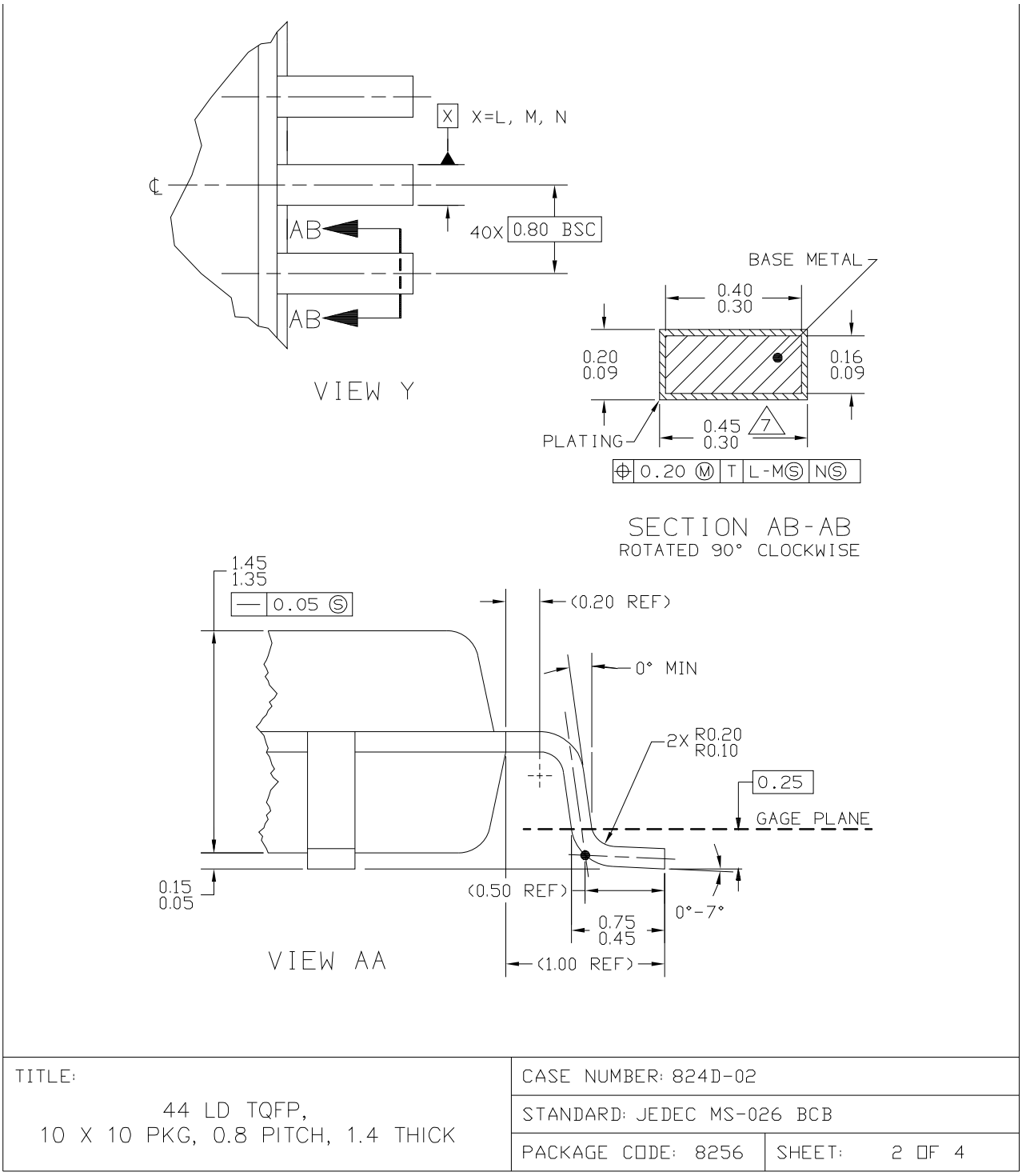


Figure 11-3 56F8035/56F8025 44-Pin LQFP Mechanical Information (2 of 3)

Please see **www.freescale.com** for the most current case outline.

- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF}, V_{DDA}, and V_{SSA} pins
- Using separate power planes for V_{DD} and V_{DDA} and separate ground planes for V_{SS} and V_{SSA} are recommended. Connect the separate analog and digital power and ground planes as close as possible to power supply outputs. If both analog circuit and digital circuit are powered by the same power supply, it is advisable to connect a small inductor or ferrite bead in serial with both V_{DDA} and V_{SSA} traces.
- It is highly desirable to physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. It is also desirable to place an analog ground trace around an analog signal trace to isolate it from digital traces.
- Because the Flash memory is programmed through the JTAG/EOnCE port, QSPI, QSCI, or I^2C, the designer should provide an interface to this port if in-circuit Flash programming is desired
- If desired, connect an external RC circuit to the $\overline{\text{RESET}}$ pin. The Resistor value should be in the range of 4.7k—10k; the Capacitor value should be in the range of 0.22µf - 4.7µf.
- Add a 3.3k external pull-up on the TMS pin of the JTAG port to keep EOnce in a restate during normal operation if JTAG converter is not present
- During reset and after reset but before I/O initialization, all I/O pins are at input state with internal pull-up enable. The typical value of internal pull-up is around 110K. These internal pull-ups can be disabled by software.
- To eliminate PCB trace impedance effect, each ADC input should have a 33pf-10 ohm RC filter
- Device GPIOs have only a down (substrate) diode on the GPIO circuit. Devices do not have a positive clamp diode because GPIOs use a floating gate structure to tolerate 5V input. The absolute maximum clamp current is -20mA at V_{in} less than 0V. The continuous clamp current is -2mA at V_{in} less than 0V. If positive voltage spikes are a concern, a positive clamp is recommended.

Part 13 Ordering Information

Table 13-1 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order devices.

Table 13-1 56F8035/56F8025 Ordering Information

Device	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Ambient Temperature Range	Order Number
MC56F8035	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	44	32	-40° to + 105° C	MC56F8035VLD*
MC56F8025	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	44	32	-40° to + 105° C	MC56F8025VLD*
MC56F8025	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	44	32	-40° to + 125° C	MC56F8025MLD*

* This package is RoHS compliant.