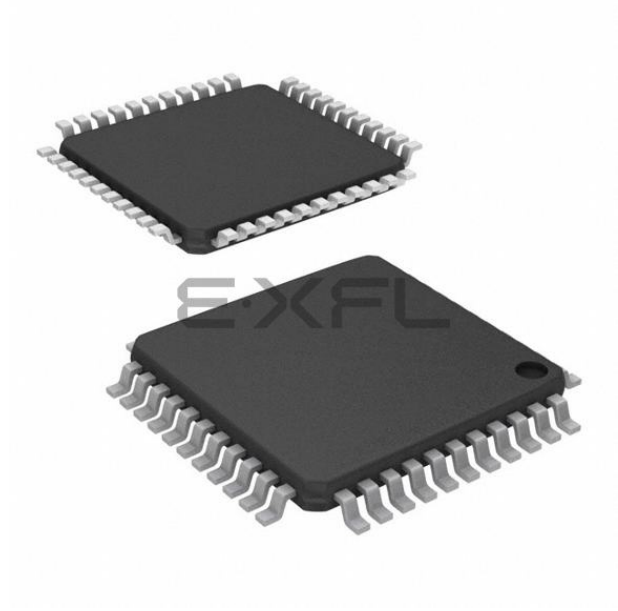

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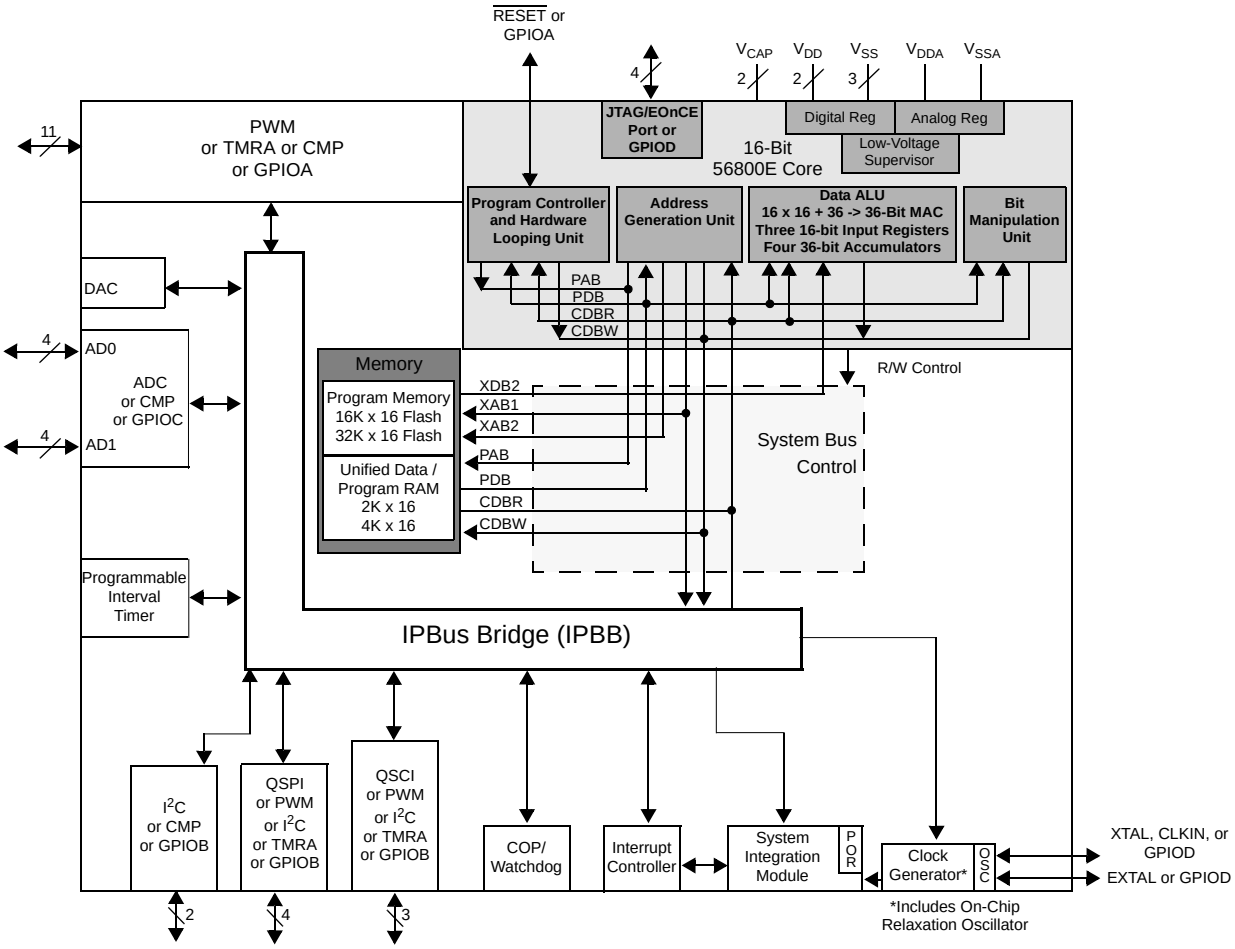
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8035vld

56F8035/56F8025 General Description

- Up to 32 MIPS at 32MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- 56F8035 offers 64KB (32K x 16) Program Flash
- 56F8025 offers 32KB (16K x 16) Program Flash
- 56F8035 offers 8KB (4K x 16) Unified Data/Program RAM
- 56F8025 offers 4KB (2K x 16) Unified Data/Program RAM
- One 6-channel PWM module
- Two 4-channel 12-bit Analog-to-Digital Converters (ADCs)
- Two Internal 12-bit Digital-to-Analog Converters (DACs)
- Two Analog Comparators
- Three Programmable Interval Timers (PITs)
- One Queued Serial Communication Interface (QSCI) with LIN slave functionality
- One Queued Serial Peripheral Interfaces (QSPI)
- One 16-bit Quad Timer
- One Inter-Integrated Circuit (I^2C) port
- Computer Operating Properly (COP)/Watchdog
- On-Chip Relaxation Oscillator
- Integrated Power-On Reset (POR) and Low-Voltage Interrupt (LVI) module
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging
- Up to 35 GPIO lines



56F8035/56F8025 Block Diagram

Table 2-3 56F8035/56F8025 Signal and Package Information for the 44-Pin LQFP

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOC3 **(ANA3)** **(V_{REFLA})**	13	Input/ Output Analog Input Analog Input	Input	**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. **ANA3** — Analog input to ADC A, Channel 3. **V_{REFLA}** — Analog reference voltage low (ADC A). After reset, the default state is GPIOC3.
GPIOC4 **(ANB0 & CMPBI3)**	7	Input/ Output Analog Input	Input	**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. **ANB0** — Analog input to ADC B, Channel 0. **Comparator B, Input 3** — This is an analog input to Comparator B. When used as an analog input, the signal goes to both the ANB0 and CMPBI3. After reset, the default state is GPIOC4.
GPIOC5 **(ANB1)**	8	Input/ Output Analog Input	Input	**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. **ANB1** — Analog input to ADC B, Channel 1. After reset, the default state is GPIOC5.
GPIOC6 **(ANB2)** **(V_{REFHB})**	9	Input/ Output Analog Input Input	Input	**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. **ANB2** — Analog input to ADC B, Channel 2. **V_{REFHB}** — Analog reference voltage high (ADC B). After reset, the default state is GPIOC6.

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Table 2-3 56F8035/56F8025 Signal and Package Information for the 44-Pin LQFP

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
TDO **(GPIOD1)**	44	Output Input/ Output	Output tri-stated, internal pull-up enabled	**Test Data Output** — This tri-stateable output pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and changes on the falling edge of TCK. **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TDO.
TCK **(GPIOD2)**	19	Input Input/ Output	Input, internal pull-up enabled	**Test Clock Input** — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pull-up resistor. A Schmitt trigger input is used for noise immunity. **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TCK.
TMS **(GPIOD3)**	43	Input Input/ Output	Input, internal pull-up enabled	**Test Mode Select Input** — This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TMS. **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.

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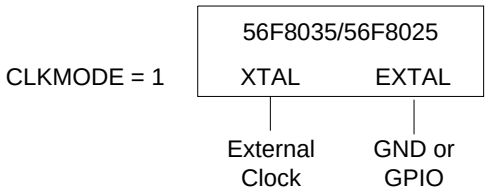


Figure 3-3 Connecting an External Clock Signal using XTAL

3.8 Alternate External Clock Input

The recommended method of connecting an external clock is illustrated in **Figure 3-3.** The external clock source is connected to GPIO6/RXD (primary) or GPIOB5/TA1/FAULT3/XTAL/EXTAL (secondary). The user has the option of using GPIO6/RXD/CLKIN or GPIOB5/TA1/FAULT3/CLKIN as external clock input.

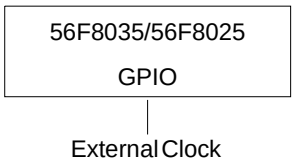


Figure 3-4 Connecting an External Clock Signal using GPIO

Part 4 Memory Maps

4.1 Introduction

The 56F8035/56F8025 device is a 16-bit motor-control chip based on the 56800E core. It uses a Harvard-style architecture with two independent memory spaces for Data and Program. On-chip RAM is shared by both spaces and Flash memory is used only in Program space.

This section provides memory maps for:

- Program Address Space, including the Interrupt Vector Table
- Data Address Space, including the EOnCE Memory and Peripheral Memory Maps

On-chip memory sizes for the device are summarized in **Table 4-1.** Flash memories' restrictions are identified in the "Use Restrictions" column of **Table 4-1.**

Table 4-9 Quad Timer A Registers Address Map (Continued) (TMRA_BASE = $00 F000)

Register Acronym	Address Offset	Register Description
TMRA0_ENBL	$F	Timer Channel Enable Register
TMRA1_COMP1	$10	Compare Register 1
TMRA1_COMP2	$11	Compare Register 2
TMRA1_CAPT	$12	Capture Register
TMRA1_LOAD	$13	Load Register
TMRA1_HOLD	$14	Hold Register
TMRA1_CNTR	$15	Counter Register
TMRA1_CTRL	$16	Control Register
TMRA1_SCTRL	$17	Status and Control Register
TMRA1_CMPLD1	$18	Comparator Load Register 1
TMRA1_CMPLD2	$19	Comparator Load Register 2
TMRA1_CSCTRL	$1A	Comparator Status and Control Register
TMRA1_FILT	$1B	Input Filter Register
		Reserved
TMRA2_COMP1	$20	Compare Register 1
TMRA2_COMP2	$21	Compare Register 2
TMRA2_CAPT	$22	Capture Register
TMRA2_LOAD	$23	Load Register
TMRA2_HOLD	$24	Hold Register
TMRA2_CNTR	$25	Counter Register
TMRA2_CTRL	$26	Control Register
TMRA2_SCTRL	$27	Status and Control Register
TMRA2_CMPLD1	$28	Comparator Load Register 1
TMRA2_CMPLD2	$29	Comparator Load Register 2
TMRA2_CSCTRL	$2A	Comparator Status and Control Register
TMRA2_FILT	$2B	Input Filter Register
		Reserved
TMRA3_COMP1	$30	Compare Register 1
TMRA3_COMP2	$31	Compare Register 2
TMRA3_CAPT	$32	Capture Register
TMRA3_LOAD	$33	Load Register
TMRA3_HOLD	$34	Hold Register
TMRA3_CNTR	$35	Counter Register
TMRA3_CTRL	$36	Control Register
TMRA3_SCTRL	$37	Status and Control Register
TMRA3_CMPLD1	$38	Comparator Load Register 1
TMRA3_CMPLD2	$39	Comparator Load Register 2

Table 4-10 Analog-to-Digital Converter Registers Address Map (Continued) (ADC_BASE = $00 F080)

Register Acronym	Address Offset	Register Description
ADC_LOLIM1	$1D	Low Limit Register 1
ADC_LOLIM2	$1E	Low Limit Register 2
ADC_LOLIM3	$1F	Low Limit Register 3
ADC_LOLIM4	$20	Low Limit Register 4
ADC_LOLIM5	$21	Low Limit Register 5
ADC_LOLIM6	$22	Low Limit Register 6
ADC_LOLIM7	$23	Low Limit Register 7
ADC_HILIM0	$24	High Limit Register 0
ADC_HILIM1	$25	High Limit Register 1
ADC_HILIM2	$26	High Limit Register 2
ADC_HILIM3	$27	High Limit Register 3
ADC_HILIM4	$28	High Limit Register 4
ADC_HILIM5	$29	High Limit Register 5
ADC_HILIM6	$2A	High Limit Register 6
ADC_HILIM7	$2B	High Limit Register 7
ADC_OFFST0	$2C	Offset Register 0
ADC_OFFST1	$2D	Offset Register 1
ADC_OFFST2	$2E	Offset Register 2
ADC_OFFST3	$2F	Offset Register 3
ADC_OFFST4	$30	Offset Register 4
ADC_OFFST5	$31	Offset Register 5
ADC_OFFST6	$32	Offset Register 6
ADC_OFFST7	$33	Offset Register 7
ADC_PWR	$34	Power Control Register
ADC_CAL	$35	Calibration Register
		Reserved

Table 4-11 Pulse Width Modulator Registers Address Map (PWM_BASE = $00 F0C0)

Register Acronym	Address Offset	Register Description
PWM_CTRL	$0	Control Register
PWM_FCTRL	$1	Fault Control Register
PWM_FLTACK	$2	Fault Status Acknowledge Register
PWM_OUT	$3	Output Control Register
PWM_CNTR	$4	Counter Register
PWM_CMOD	$5	Counter Modulo Register
PWM_VAL0	$6	Value Register 0

Table 4-12 Interrupt Control Registers Address Map (Continued) (ITCN_BASE = $00 F0E0)

Register Acronym	Address Offset	Register Description
ITCN_IRQP0	$E	IRQ Pending Register 0
ITCN_IRQP1	$F	IRQ Pending Register 1
ITCN_IRQP2	$10	IRQ Pending Register 2
ITCN_IRQP3	$11	IRQ Pending Register 3
		Reserved
ITCN_ICTRL	$16	Interrupt Control Register
		Reserved

Table 4-13 SIM Registers Address Map (SIM_BASE = $00 F100)

Register Acronym	Address Offset	Register Description
SIM_CTRL	$0	Control Register
SIM_RSTAT	$1	Reset Status Register
SIM_SWC0	$2	Software Control Register 0
SIM_SWC1	$3	Software Control Register 1
SIM_SWC2	$4	Software Control Register 2
SIM_SWC3	$5	Software Control Register 3
SIM_MSHID	$6	Most Significant Half JTAG ID
SIM_LSHID	$7	Least Significant Half JTAG ID
SIM_PWR	$8	Power Control Register
		Reserved
SIM_CLKOUT	$A	Clock Out Select Register
SIM_PCR	$B	Peripheral Clock Rate Register
SIM_PCE0	$C	Peripheral Clock Enable Register 0
SIM_PCE1	$D	Peripheral Clock Enable Register 1
SIM_SD0	$E	Peripheral STOP Disable Register 0
SIM_SD1	$F	Peripheral STOP Disable Register 1
SIM_IOSAHI	$10	I/O Short Address Location High Register
SIM_IOSALO	$11	I/O Short Address Location Low Register
SIM_PROT	$12	Protection Register
SIM_GPSA0	$13	GPIO Peripheral Select Register 0 for GPIOA
SIM_GPSA1	$14	GPIO Peripheral Select Register 1 for GPIOA
SIM_GPSB0	$15	GPIO Peripheral Select Register 0 for GPIOB
SIM_GPSB1	$16	GPIO Peripheral Select Register 1 for GPIOB
SIM_GPSCD	$17	GPIO Peripheral Select Register for GPIOC and GPIOD
SIM_IPS0	$18	Internal Peripheral Source Select Register 0 for PWM
SIM_IPS1	$19	Internal Peripheral Source Select Register 1 for DACs

Table 4-20 GPIOD Registers Address Map (GPIOD_BASE = $00 F180)

Register Acronym	Address Offset	Register Description
GPIOD_PUPEN	$0	Pull-up Enable Register
GPIOD_DATA	$1	Data Register
GPIOD_DDIR	$2	Data Direction Register
GPIOD_PEREN	$3	Peripheral Enable Register
GPIOD_IASSRT	$4	Interrupt Assert Register
GPIOD_IEN	$5	Interrupt Enable Register
GPIOD_IEPOL	$6	Interrupt Edge Polarity Register
GPIOD_IPEND	$7	Interrupt Pending Register
GPIOD_IEDGE	$8	Interrupt Edge-Sensitive Register
GPIOD_PPOUTM	$9	Push-Pull Output Mode Control Register
GPIOD_RDATA	$A	Raw Data Input Register
GPIOD_DRIVE	$B	Output Drive Strength Control Register

Table 4-21 Programmable Interval Timer 0 Registers Address Map (PIT0_BASE = $00 F190)

Register Acronym	Address Offset	Register Description
PIT0_CTRL	$0	Control Register
PIT0_MOD	$1	Modulo Register
PIT0_CNTR	$2	Counter Register

Table 4-22 Programmable Interval Timer 1 Registers Address Map (PIT1_BASE = $00 F1A0)

Register Acronym	Address Offset	Register Description
PIT1_CTRL	$0	Control Register
PIT1_MOD	$1	Modulo Register
PIT1_CNTR	$2	Counter Register

Table 4-23 Programmable Interval Timer 2 Registers Address Map (PIT2_BASE = $00 F1B0)

Register Acronym	Address Offset	Register Description
PIT2_CTRL	$0	Control Register

Add. Offset	Register Name		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	IPR0	R	PLL IPL		LVI IPL		0	0	RX_REG IPL		TX_REG IPL		TRBUF IPL		BKPT_U IPL		STPCNT IPL	
		W																
$1	IPR1	R	GPIOD IPL		0	0	0	0	0	0	0	0	FM_CBE IPL		FM_CC IPL		FM_ERR IPL	
		W																
$2	IPR2	R	QSCI0_XMIT IPL		0	0	0	0	QSPI0_XMIT IPL		QSPI0_RCV IPL		GPIOA IPL		GPIOB IPL		GPIOC IPL	
		W																
$3	IPR3	R	I2C_ERR IPL		0	0	0	0	0	0	0	0	QSCI0_RCV IPL		QSCI0_RERR IPL		QSCI0_TIDL IPL	
		W																
$4	IPR4	R	TMRA_3 IPL		TMRA_2 IPL		TMRA_1 IPL		TMRA_0 IPL		I2C_STAT IPL		I2C_TX IPL		I2C_RX IPL		I2C_GEN IPL	
		W																
$5	IPR5	R	PIT1 IPL		PIT0 IPL		COMPB IPL		COMPA IPL		TMRB_3 IPL		TMRB_2 IPL		TMRB_1 IPL		TMRB_0 IPL	
		W																
$6	IPR6		0	0	0	0	PWM_F IPL		PWM_RL IPL		ADC_ZC IPL		ADCB_CC IPL		ADCA_CC IPL		PIT2 IPL	
$7	VBA	R	0	0	VECTOR_BASE_ADDRESS													
		W																
$8	FIM0	R	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0					
		W																
$9	FIVAL0	R	FAST INTERRUPT 0 VECTOR ADDRESS LOW															
		W																
$A	FIVAH0	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0 VECTOR ADDRESS HIGH				
		W																
$B	FIM1	R	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1					
		W																
$C	FIVAL1	R	FAST INTERRUPT 1 VECTOR ADDRESS LOW															
		W																
$D	FIVAH1	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1 VECTOR ADDRESS HIGH				
		W																
$E	IRQP0	R	PENDING[16:2]															1
		W																
$F	IRQP1	R	PENDING[32:17]															
		W																
$10	IRQP2	R	PENDING[48:33]															
		W																
$11	IRQP3	R	PENDING[63:49]															
		W																
	Reserved																	
$16	ICTRL	R	INT	IPIC			VAB						INT_DIS	1	1	1	0	0
		W																
	Reserved																	

= Reserved

Figure 5-2 ITCN Register Map Summary

6.3.19.1 Reserved—Bits 15–9

This bit field is reserved. Each bit must be set to 0.

6.3.19.2 Configure GPIOB11 (GPS_B11)—Bit 8

This field selects the alternate function for GPIOB11.

- 0 = CMPBO - Comparator B Output (default)
- 1 = Reserved

6.3.19.3 Reserved—Bit 7

This bit field is reserved. It must be set to 0.

6.3.19.4 Configure GPIOB10 (GPS_B10)—Bit 6

This field selects the alternate function for GPIOB10.

- 0 = CMPAO - Comparator A Output (default)
- 1 = Reserved

6.3.19.5 Reserved—Bits 5–1

This bit field is reserved. Each bit must be set to 0.

6.3.19.6 Configure GPIOB7 (GPS_B7)—Bit 0

This field selects the alternate function for GPIOB7.

- 0 = TXD0 - QSCI0 Transmit Data (default)
- 1 = SCL - I^2C Serial Clock

6.3.20 SIM GPIO Peripheral Select Register for GPIOC and GPIOD (SIM_GPSCD)

See **Section 6.3.16** for general information about GPIO Peripheral Select Registers.

Base + $17	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	GPS_D5	0	0	0	0	0	0	0	0	0	0	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-23 GPIO Peripheral Select Register for GPIOC and GPIOD (SIM_GPSCD)

6.3.20.1 Reserved—Bits 15–13

This bit field is reserved. Each bit must be set to 0.

6.3.20.2 Configure GPIOD5 (GPS_D5)—Bit 12

This field selects the alternate function for GPIOD5.

Base + $18	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	IPS0_ FAULT2	0	IPS0_ FAULT1	0	0	IPS0_PSRC2			IPS0_PSRC1			IPS0_PSRC0		
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-25 Internal Peripheral Source Select Register for PWM (SIM_IPS0)

6.3.21.1 Reserved—Bits 15–14

This bit field is reserved. Each bit must be set to 0.

6.3.21.2 Select Peripheral Input Source for FAULT2 (IPS0_FAULT2)—Bit 13

This field selects the alternate input source signal to feed PWM input FAULT2.

- 0 = I/O Pin (External) - Use PWM FAULT2 Input Pin (default)
- 1 = CMPBO (Internal) - Use Comparator B Output

6.3.21.3 Reserved—Bit 12

This bit field is reserved. It must be set to 0.

6.3.21.4 Select Input Source for FAULT1 (IPS0_FAULT1)—Bit 11

This field selects the alternate input source signal to feed PWM input FAULT1.

- 0 = I/O pin (External) - Use PWM FAULT2 Input Pin (default)
- 1 = CMPAO (Internal) - Use Comparator A Output

6.3.21.5 Reserved—Bits 10–9

This bit field is reserved. Each bit must be set to 0.

6.3.21.6 Select Peripheral Input Source for PWM4/PWM5 Pair Source (IPS0_PSRC2)—Bits 8–6

This field selects the alternate input source signal to feed PWM input PSRC2 as the PWM4/PWM5 pair source.

- 000 = Reserved (default)
- 001 = TA3 (Internal) - Use Timer A3 output as PWM source
- 010 = ADC SAMPLE2 (Internal) - Use ADC SAMPLE2 result as PWM source
  - If the ADC conversion result in SAMPLE2 is greater than the value programmed into the High Limit register HLMT2, then PWM4 is set to 0 and PWM5 is set to 1
  - If the ADC conversion result in SAMPLE2 is less than the value programmed into the Low Limit register LLMT2, then PWM4 is set to 1 and PWM5 is set to 0
- 011 = CMPAO (Internal) - Use Comparator A output as PWM source
- 100 = CMPBO (Internal) - Use Comparator B output as PWM source

security mode is enabled, the 56F8025 will disable the core EOnCE debug capabilities. Normal program execution is otherwise unaffected.

7.2 Flash Access Lock and Unlock Mechanisms

There are several methods that effectively lock or unlock the on-chip flash.

7.2.1 Disabling EOnCE Access

On-chip flash can be read by issuing commands across the EOnCE port, which is the debug interface for the 56800E CPU. The TCK, TMS, TDO, and TDI pins comprise a JTAG interface onto which the EOnCE port functionality is mapped. When the device boots, the chip-level JTAG TAP (Test Access Port) is active and provides the chip's boundary scan capability and access to the ID register, but proper implementation of flash security will block any attempt to access the internal flash memory via the EOnCE port when security is enabled.

7.2.2 Flash Lockout Recovery Using JTAG

If the device is secured, one lockout recovery mechanism is the complete erasure of the internal flash contents, including the configuration field, thus disabling security (the protection register is cleared). This does not compromise security, as the entire contents of the user's secured code stored in flash are erased before security is disabled on the device on the next reset or power-up sequence.

To start the lockout recovery sequence via JTAG, the JTAG public instruction (LOCKOUT_RECOVERY) must first be shifted into the chip-level TAP controller's instruction register. Once the LOCKOUT_RECOVERY instruction has been shifted into the instruction register, the clock divider value must be shifted into the corresponding 7-bit data register. After the data register has been updated, the user must transition the TAP controller into the RUN-TEST/IDLE state for the lockout sequence to commence. The controller must remain in this state until the erase sequence is complete. Refer to the **56F802x and 56F803x Peripheral Reference Manual** for more details, or contact Freescale.

Note: Once the lockout recovery sequence has completed, the user must reset both the JTAG-TAP controller and device to return to normal unsecured operation. Power-on reset will reset both too.

7.2.3 Flash Lockout Recovery using CodeWarrior

CodeWarrior can unlock a device by selecting the *Debug* menu, then selecting *DSP56800E*, followed by *Unlock Flash*. Another mechanism is also built into CodeWarrior using the device's memory configuration file. The command "*Unlock_Flash_on_Connect 1*" in the *.cfg* file accomplishes the same task as using the *Debug* menu.

This lockout recovery mechanism is the complete erasure of the internal flash contents, including the configuration field, thus disabling security (the protection register is cleared).

7.2.4 Flash Lockout Recovery without mass erase

A user can un-secure a secured device by programming the word $0000 into program memory location $00 7FF7. After completing the programming, both the JTAG TAP controller and the device must be reset

Table 10-4 Recommended Operating Conditions
($V_{REFL\ x}$= 0V, V_{SSA} = 0V, V_{SS} = 0V)

Characteristic	Symbol	Notes	Min	Typ	Max	Unit
Supply voltage	V_{DD}, V_{DDA}		3	3.3	3.6	V
ADC Reference Voltage High	V_{REFHx}		3.0		V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		-0.1	0	0.1	V
Device Clock Frequency Using relaxation oscillator Using external clock source	FSYSCLK		 1 0		 32 32	MHz
Input Voltage High (digital inputs)	V_{IH}	Pin Groups 1, 2	2.0		5.5	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2	-0.3		0.8	V
Oscillator Input Voltage High XTAL driven by an external clock source	V_{IHOSC}	Pin Group 4	2.0		V_{DDA} + 0.3	V
Oscillator Input Voltage Low	V_{ILOSC}	Pin Group 4	-0.3		0.8	V
Output Source Current High at V_{OH} min.)[1] When programmed for low drive strength When programmed for high drive strength	I_{OH}	 Pin Group 1 Pin Group 1	 — —		 -4 -8	mA
Output Source Current Low (at V_{OL} max.)[1] When programmed for low drive strength When programmed for high drive strength	I_{OL}	 Pin Groups 1, 2 Pin Groups 1, 2	 — —		 4 8	mA
Ambient Operating Temperature (Extended Industrial)	T_A		-40		105	°C
Flash Endurance (Program Erase Cycles)	N_F	T_A = -40°C to 125°C	10,000		—	cycles
Flash Data Retention	T_R	T_J <= 85°C avg	15		—	years
Flash Data Retention with <100 Program/Erase Cycles	t_{FLRET}	T_J <= 85°C avg	20	—	—	years

1. Total chip source or sink current cannot exceed 75mA

Default Mode

Pin Group 1: GPIO, TDI, TDO, TMS, TCK

Pin Group 2: $\overline{\text{RESET}}$, GPIOA7

Pin Group 3: ADC and Comparator Analog Inputs

Pin Group 4: XTAL, EXTAL

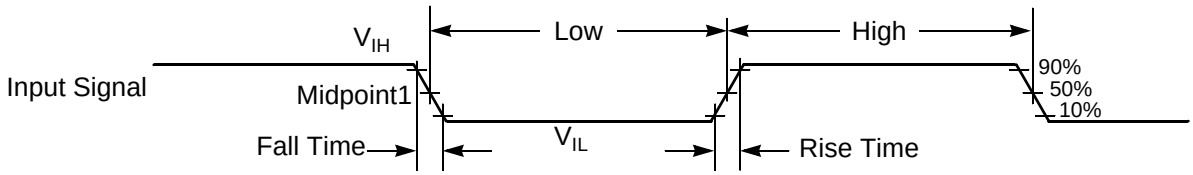
and tantalum capacitors tend to provide better performance tolerances. The output voltage can be measured directly on the V_{CAP} pin. The specifications for this regulator are shown in **Table 10-8**.

Table 10-8. Regulator Parameters

Characteristic	Symbol	Min	Typical	Max	Unit
Short Circuit Current	I_{SS}	—	450	650	mA
Short Circuit Tolerance (V_{CAP} shorted to ground)	T_{RSC}	—	—	30	minutes

10.3 AC Electrical Characteristics

Tests are conducted using the input levels specified in **Table 10-5**. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in **Figure 10-2**.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 10-2 Input Signal Measurement References

Figure 10-3 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

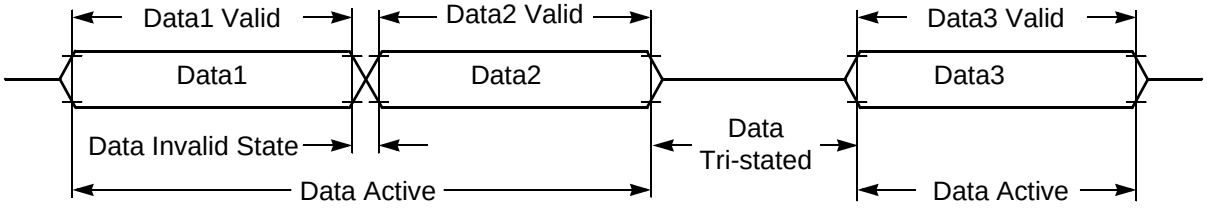


Figure 10-3 Signal States

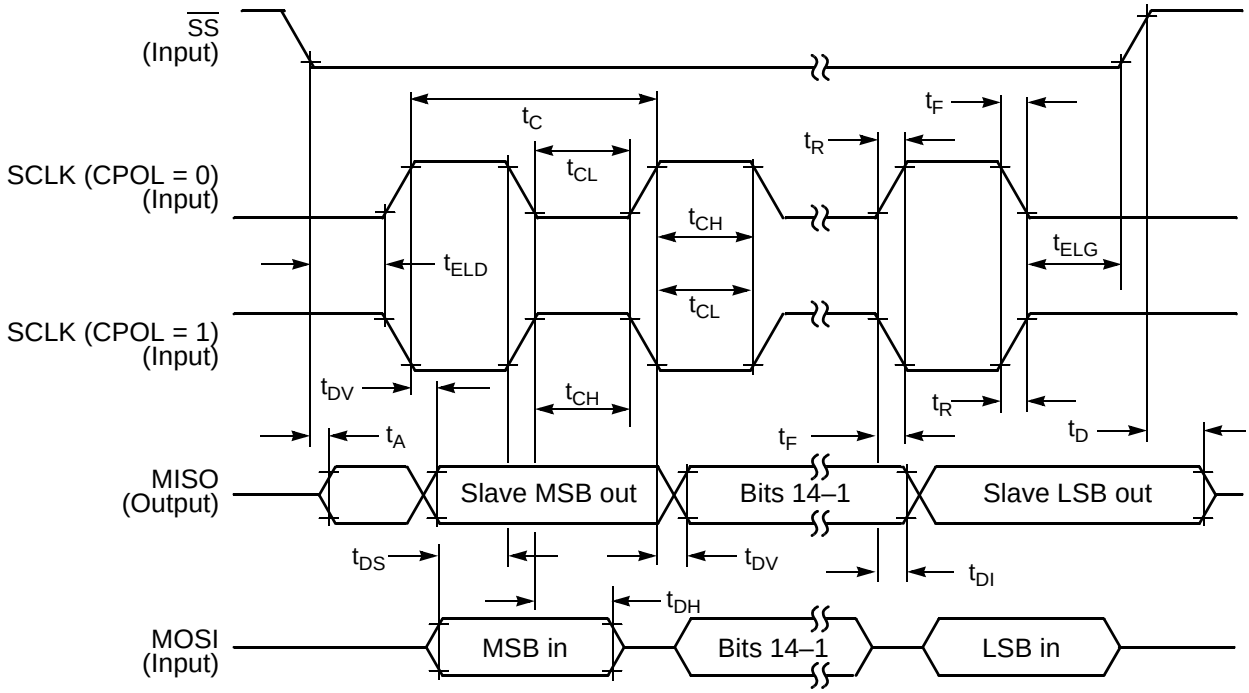


Figure 10-10 SPI Slave Timing (CPHA = 1)

10.10 Quad Timer Timing

Table 10-15 Timer Timing[1, 2]

Characteristic	Symbol	Min	Max	Unit	See Figure
Timer input period	P_{IN}	2T + 6	—	ns	10-11
Timer input high / low period	P_{INHL}	1T + 3	—	ns	10-11
Timer output period	P_{OUT}	125	—	ns	10-11
Timer output high / low period	P_{OUTHL}	50	—	ns	10-11

1. In the formulas listed, T = the clock cycle. For 32MHz operation, T = 31.25ns.
2. Parameters listed are guaranteed by design.

10.18 Power Consumption

See **Section 10.1** for a list of IDD requirements for the 56F8035/56F8025. This section provides additional detail which can be used to optimize power consumption for a given application.

Power consumption is given by the following equation:

Total power = A: internal [static component]
+B: internal [state-dependent component]
+C: internal [dynamic component]
+D: external [dynamic component]
+E: external [static component]

A, the internal [static component], is comprised of the DC bias currents for the oscillator, leakage currents, PLL, and voltage references. These sources operate independently of processor state or operating frequency.

B, the internal [state-dependent component], reflects the supply current required by certain on-chip resources only when those resources are in use. These include RAM, Flash memory and the ADCs.

C, the internal [dynamic component], is classic $C*V^2*F$ CMOS power dissipation corresponding to the 56800E core and standard cell logic.

D, the external [dynamic component], reflects power dissipated on-chip as a result of capacitive loading on the external pins of the chip. This is also commonly described as $C*V^2*F$, although simulations on two of the I/O cell types used on the 56800E reveal that the power-versus-load curve does have a non-zero Y-intercept.

Table 10-22 I/O Loading Coefficients at 10MHz

	Intercept	Slope
8mA drive	1.3	0.11mW / pF
4mA drive	1.15mW	0.11mW / pF

Power due to capacitive loading on output pins is (first order) a function of the capacitive load and frequency at which the outputs change. **Table 10-22** provides coefficients for calculating power dissipated in the I/O cells as a function of capacitive load. In these cases:

$$TotalPower = \Sigma((\text{Intercept} + \text{Slope}*\text{Cload})*\text{frequency}/10\text{MHz})$$

where:

- Summation is performed over all output pins with capacitive loads
- TotalPower is expressed in mW

- Cload is expressed in pF

Because of the low duty cycle on most device pins, power dissipation due to capacitive loads was found to be fairly low when averaged over a period of time.

E, the external [static component], reflects the effects of placing resistive loads on the outputs of the device. Sum the total of all V^2/R or IV to arrive at the resistive load contribution to power. Assume V = 0.5 for the purposes of these rough calculations. For instance, if there is a total of eight PWM outputs driving 10mA into LEDs, then P = 8*.5*.01 = 40mW.

In previous discussions, power consumption due to parasitics associated with pure input pins is ignored, as it is assumed to be negligible.

Part 11 Packaging

11.1 56F8035/56F8025 Package and Pin-Out Information

This section contains package and pin-out information for the 56F8035/56F8025. This device comes in a 44-pin Low-profile Quad Flat Pack (LQFP). **Figure 11-1** shows the package outline, **Figure 11-2** shows the mechanical parameters and **Table 11-1** lists the pin-out.

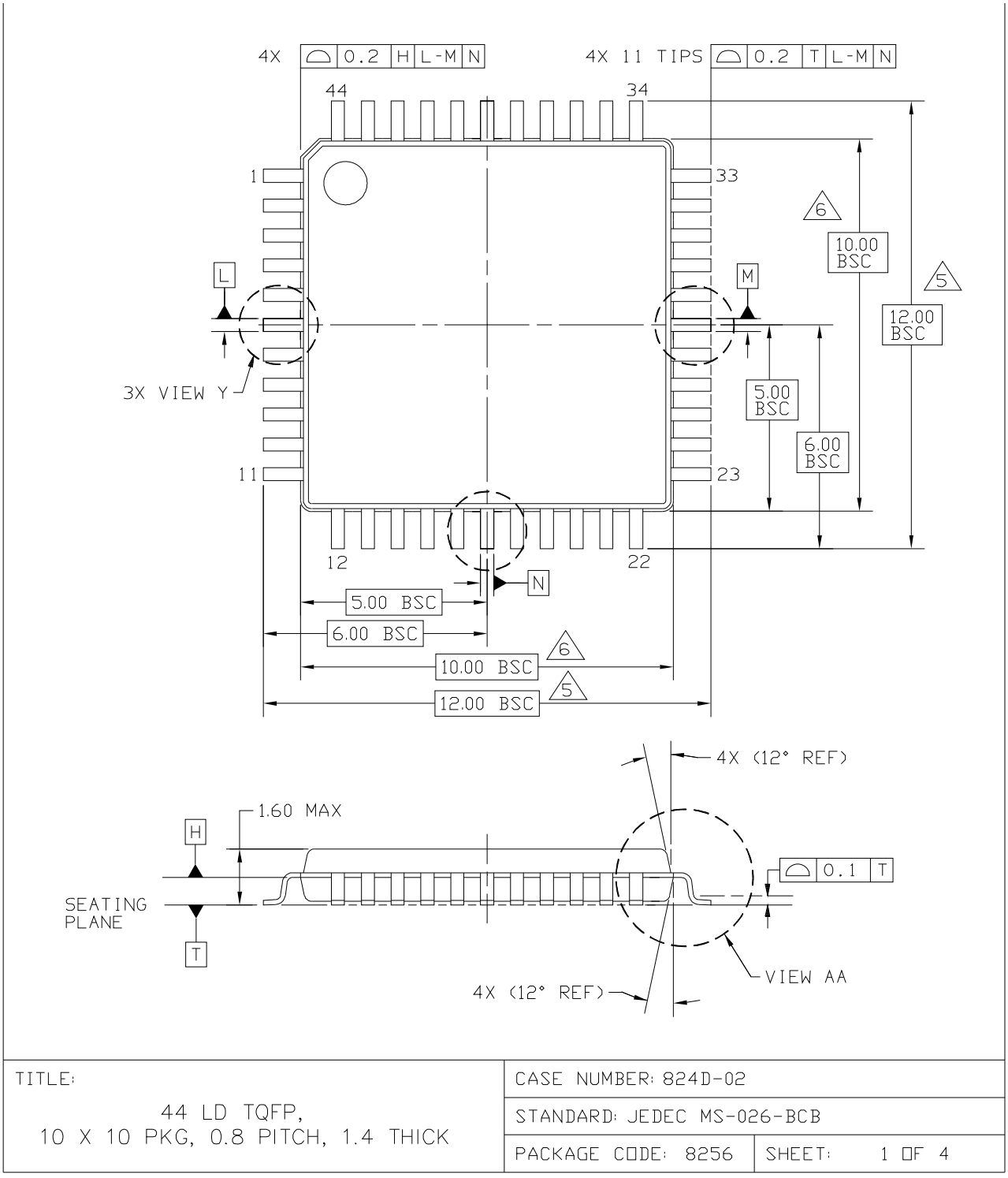


Figure 11-2 56F8035/56F8025 44-Pin LQFP Mechanical Information (1 of 3)

Please see **www.freescale.com** for the most current case outline.

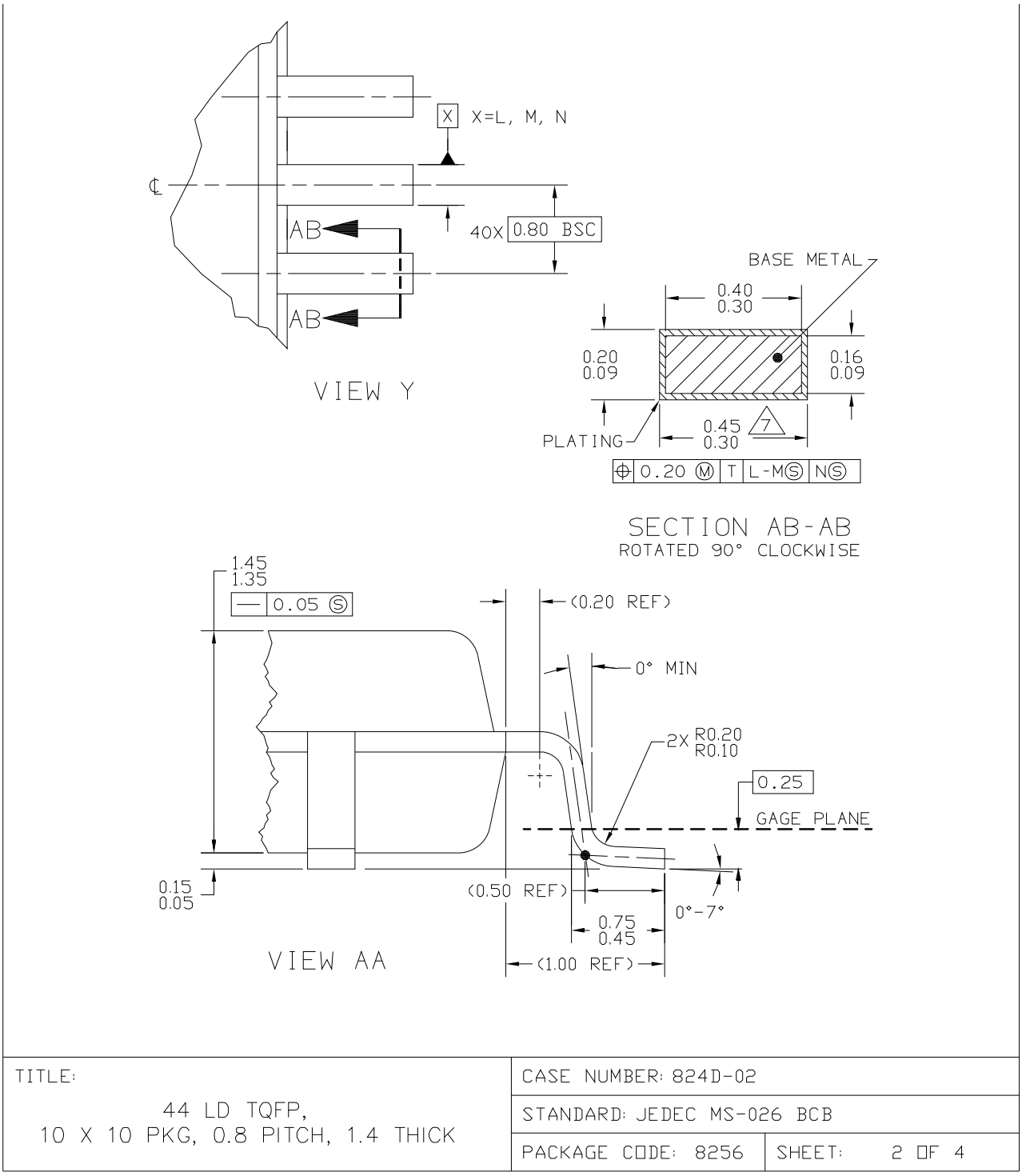


Figure 11-3 56F8035/56F8025 44-Pin LQFP Mechanical Information (2 of 3)

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