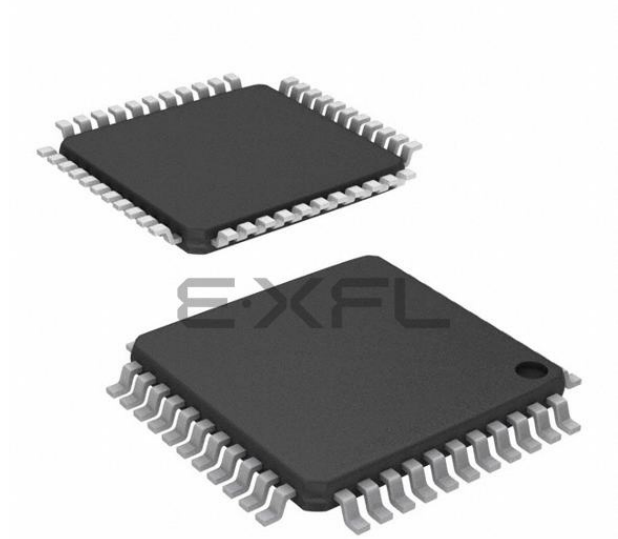

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Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8035vldr

Document Revision History

Version History	Description of Change
Rev. 6	In the table **Recommended Operating Conditions**, removed the line “XTAL not driven by an external clock“ from the characteristic: “Oscillator Input Voltage High XTAL not driven by an external clock XTAL driven by an external clock source“ Changed COUTB_A to CMPBO throughout Added MC56F8035 device Added MC56F8025MLD to the orderable parts In the **System Integration Module (SIM) chapter**, fixed typos Added IPS0_PSRC2 field to SIM_IPS0 register

Please see http://www.freescale.com for the most current data sheet revision.

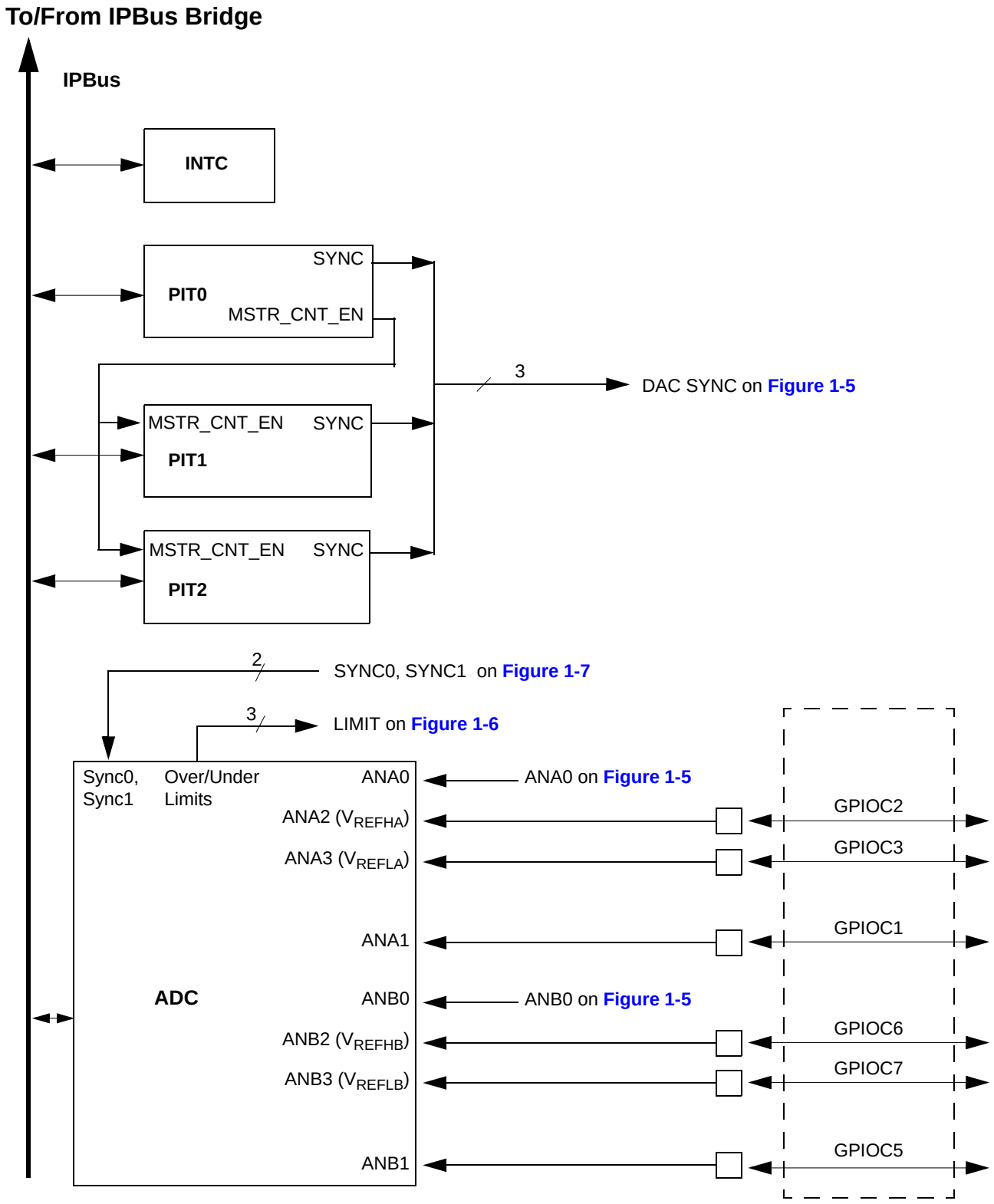

Figure 1-3 56F8035/56F8025 I/O Pin-Out Muxing (Part 1/5)

2.2 56F8035/56F8025 Signal Pins

After reset, each pin is configured for its primary function (listed first). Any alternate functionality must be programmed.

Table 2-3 56F8035/56F8025 Signal and Package Information for the 44-Pin LQFP

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
V_{DD}	29	Supply	Supply	**I/O Power** — This pin supplies 3.3V power to the chip I/O interface.
V_{DD}	35			
V_{SS}	17	Supply	Supply	V_{SS} — These pins provide ground for chip logic and I/O drivers.
V_{SS}	28			
V_{SS}	36			
V_{DDA}	11	Supply	Supply	**ADC Power** — This pin supplies 3.3V power to the ADC modules. It must be connected to a clean analog power supply.
V_{SSA}	12	Supply	Supply	**ADC Analog Ground** — This pin supplies an analog ground to the ADC modules.
V_{CAP}	18	Supply	Supply	V_{CAP} — Connect this pin to a 2.2µF or greater bypass capacitor in order to bypass the core voltage regulator, required for proper chip operation. See Section 10.2.1.
V_{CAP}	34			
$\overline{\text{RESET}}$ (GPIOA7)	21	Input Input/Open Drain Output	Input, internal pull-up enabled	**Reset** — This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the chip is initialized and placed in the reset state. A Schmitt trigger input is used for noise immunity. The internal reset signal will be deasserted synchronous with the internal clocks after a fixed number of internal clocks. **Port A GPIO** — This GPIO pin can be individually programmed as an input or open drain output pin. Note that $\overline{\text{RESET}}$ functionality is disabled in this mode and the chip can only be reset via POR, COP reset, or software reset. After reset, the default state is $\overline{\text{RESET}}$.

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Table 2-3 56F8035/56F8025 Signal and Package Information for the 44-Pin LQFP

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOA6	24	Input/ Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(FAULT0)		Input		**Fault0** — This fault input pin is used for disabling selected PWM outputs in cases where fault conditions originate off-chip.
(TA0)				**TA0** — Timer A, Channel 0. After reset, the default state is GPIOA6. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
GPIOA8	26	Input/ Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(FAULT1)		Input		**Fault1** — This fault input pin is used for disabling selected PWM outputs in cases where fault conditions originate off-chip.
(TA2)		Input/ Output		**TA2** — Timer A, Channel 2.
(CMPAI1)		Input		**Comparator A, Input 1** — This is an analog input to Comparator A. After reset, the default state is GPIOA8. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
GPIOA9	5	Input/ Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(FAULT2)		Input		**Fault2** — This fault input pin is used for disabling selected PWM outputs in cases where fault conditions originate off-chip.
(TA3)		Input/ Output		**TA2** — Timer A, Channel 3.
(CMPBI1)		Input		**Comparator B, Input 1** — This is an analog input to Comparator B. After reset, the default state is GPIOA9. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.

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Table 2-3 56F8035/56F8025 Signal and Package Information for the 44-Pin LQFP

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
TDO **(GPIOD1)**	44	Output Input/ Output	Output tri-stated, internal pull-up enabled	**Test Data Output** — This tri-stateable output pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and changes on the falling edge of TCK. **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TDO.
TCK **(GPIOD2)**	19	Input Input/ Output	Input, internal pull-up enabled	**Test Clock Input** — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pull-up resistor. A Schmitt trigger input is used for noise immunity. **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TCK.
TMS **(GPIOD3)**	43	Input Input/ Output	Input, internal pull-up enabled	**Test Mode Select Input** — This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TMS. **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.

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Table 4-1 Chip Memory Configurations

On-Chip Memory	56F8035	56F8025	Use Restrictions
Program Flash (PFLASH)	32K x 16 or 64KB	16K x 16 or 32KB	Erase/Program via Flash interface unit and word writes to CDBW
Unified RAM (RAM)	4K x 16 or 8KB	2K x 16 or 4KB	Usable by both the Program and Data memory spaces

4.2 Interrupt Vector Table

Table 4-2 provides the 56F8035/56F8025's reset and interrupt priority structure, including on-chip peripherals. The table is organized with higher-priority vectors at the top and lower-priority interrupts lower in the table. As indicated, the priority of an interrupt can be assigned to different levels, allowing some control over interrupt priorities. All level 3 interrupts will be serviced before level 2, and so on. For a selected priority level, the lowest vector number has the highest priority.

The location of the vector table is determined by the Vector Base Address (VBA). Please see Section 5.6.8 for the reset value of the VBA.

By default, the chip reset address and COP reset address will correspond to vector 0 and 1 of the interrupt vector table. In these instances, the first two locations in the vector table must contain branch or JMP instructions. All other entries must contain JSR instructions.

Table 4-2 Interrupt Vector Table Contents[1]

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
core			P:$00	Reserved for Reset Overlay[2]
core			P:$02	Reserved for COP Reset Overlay
core	2	3	P:$04	Illegal Instruction
core	3	3	P:$06	SW Interrupt 3
core	4	3	P:$08	HW Stack Overflow
core	5	3	P:$0A	Misaligned Long Word Access
core	6	1-3	P:$0C	EOnCE Step Counter
core	7	1-3	P:$0E	EOnCE Breakpoint Unit
core	8	1-3	P:$10	EOnCE Trace Buffer
core	9	1-3	P:$12	EOnCE Transmit Register Empty
core	10	1-3	P:$14	EOnCE Receive Register Full
core	11	2	P:$16	SW Interrupt 2
core	12	1	P:$18	SW Interrupt 1
core	13	0	P:$1A	SW Interrupt 0
	14			Reserved
LVI	15	1-3	P:$1E	Low-Voltage Detector (Power Sense)
PLL	16	1-3	P:$20	Phase-Locked Loop

Table 4-10 Analog-to-Digital Converter Registers Address Map (Continued) (ADC_BASE = $00 F080)

Register Acronym	Address Offset	Register Description
ADC_LOLIM1	$1D	Low Limit Register 1
ADC_LOLIM2	$1E	Low Limit Register 2
ADC_LOLIM3	$1F	Low Limit Register 3
ADC_LOLIM4	$20	Low Limit Register 4
ADC_LOLIM5	$21	Low Limit Register 5
ADC_LOLIM6	$22	Low Limit Register 6
ADC_LOLIM7	$23	Low Limit Register 7
ADC_HILIM0	$24	High Limit Register 0
ADC_HILIM1	$25	High Limit Register 1
ADC_HILIM2	$26	High Limit Register 2
ADC_HILIM3	$27	High Limit Register 3
ADC_HILIM4	$28	High Limit Register 4
ADC_HILIM5	$29	High Limit Register 5
ADC_HILIM6	$2A	High Limit Register 6
ADC_HILIM7	$2B	High Limit Register 7
ADC_OFFST0	$2C	Offset Register 0
ADC_OFFST1	$2D	Offset Register 1
ADC_OFFST2	$2E	Offset Register 2
ADC_OFFST3	$2F	Offset Register 3
ADC_OFFST4	$30	Offset Register 4
ADC_OFFST5	$31	Offset Register 5
ADC_OFFST6	$32	Offset Register 6
ADC_OFFST7	$33	Offset Register 7
ADC_PWR	$34	Power Control Register
ADC_CAL	$35	Calibration Register
		Reserved

Table 4-11 Pulse Width Modulator Registers Address Map (PWM_BASE = $00 F0C0)

Register Acronym	Address Offset	Register Description
PWM_CTRL	$0	Control Register
PWM_FCTRL	$1	Fault Control Register
PWM_FLTACK	$2	Fault Status Acknowledge Register
PWM_OUT	$3	Output Control Register
PWM_CNTR	$4	Counter Register
PWM_CMOD	$5	Counter Modulo Register
PWM_VAL0	$6	Value Register 0

5.6.1.5 EOnCE Transmit Register Empty Interrupt Priority Level (TX_REG IPL)— Bits 7–6

This field is used to set the interrupt priority level for the EOnCE Transmit Register Empty IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.6 EOnCE Trace Buffer Interrupt Priority Level (TRBUF IPL)— Bits 5–4

This field is used to set the interrupt priority level for the EOnCE Trace Buffer IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.7 EOnCE Breakpoint Unit Interrupt Priority Level (BKPT_U IPL)— Bits 3–2

This field is used to set the interrupt priority level for the EOnCE Breakpoint Unit IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.8 EOnCE Step Counter Interrupt Priority Level (STPCNT IPL)— Bits 1–0

This field is used to set the interrupt priority level for the EOnCE Step Counter IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.8 Vector Base Address Register (VBA)

Base + $7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	VECTOR_BASE_ADDRESS													
Write																
RESET[1]	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

1. The 56F8035 resets to a value of 0 x 0000. This corresponds to reset addresses of 0 x 000000.
The 56F8025 resets to a value of 0 x 0080. This corresponds to reset addresses of 0 x 004000.

Figure 5-10 Vector Base Address Register (VBA)

5.6.8.1 Reserved—Bits 15–14

This bit field is reserved. Each bit must be set to 0.

5.6.8.2 Vector Address Bus (VAB) Bits 13–0

The value in this register is used as the upper 14 bits of the interrupt vector VAB[20:0]. The lower 7 bits are determined based on the highest priority interrupt and are then appended onto VBA before presenting the full VAB to the Core.

5.6.9 Fast Interrupt Match 0 Register (FIM0)

Base + $8	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0					
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-11 Fast Interrupt Match 0 Register (FIM0)

5.6.9.1 Reserved—Bits 15–6

This bit field is reserved. Each bit must be set to 0.

5.6.9.2 Fast Interrupt 0 Vector Number (FAST INTERRUPT 0)—Bits 5–0

These values determine which IRQ will be Fast Interrupt 0. Fast Interrupts vector directly to a service routine based on values in the Fast Interrupt Vector Address registers without having to go to a jump table first. IRQs used as Fast Interrupts *must* be set to priority level 2. Unexpected results will occur if a Fast Interrupt vector is set to any other priority. A Fast Interrupt automatically becomes the highest-priority level 2 interrupt regardless of its location in the interrupt table prior to being declared as Fast Interrupt. Fast Interrupt 0 has priority over Fast Interrupt 1. To determine the vector number of each IRQ, refer to the vector table.

5.6.15.1 IRQ Pending (PENDING)—Bits 16–2

These register bit values represent the pending IRQs for interrupt vector numbers 2 through 16. Ascending IRQ numbers correspond to ascending bit locations.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.15.2 Reserved—Bit 0

This bit field is reserved. It must be set to 1.

5.6.16 IRQ Pending Register 1 (IRQP1)

Base + $F	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING[32:17]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-18 IRQ Pending Register 1 (IRQP1)

5.6.16.1 IRQ Pending (PENDING)—Bits 32–17

These register bit values represent the pending IRQs for interrupt vector numbers 17 through 32. Ascending IRQ numbers correspond to ascending bit locations.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.17 IRQ Pending Register 2 (IRQP2)

Base + $10	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING[48:33]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-19 IRQ Pending Register 2 (IRQP2)

5.6.17.1 IRQ Pending (PENDING)—Bits 48–33

These register bit values represent the pending IRQs for interrupt vector numbers 33 through 48. Ascending IRQ numbers correspond to ascending bit locations.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

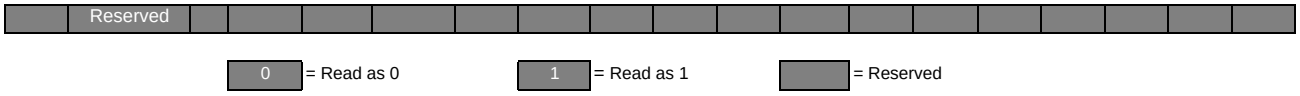

Figure 6-1 SIM Register Map Summary

6.3.1 SIM Control Register (SIM_CTRL)

Base + $0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	ONCE EBL	SW RST	STOP_ DISABLE		WAIT_ DISABLE	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-2 SIM Control Register (SIM_CTRL)

6.3.1.1 Reserved—Bits 15–6

This bit field is reserved. Each bit must be set to 0.

6.3.1.2 OnCE Enable (ONCEEBL)—Bit 5

- 0 = OnCE clock to 56800E core enabled when core TAP is enabled
- 1 = OnCE clock to 56800E core is always enabled

Note: Using default state “0” is recommended.

6.3.1.3 Software Reset (SWRST)—Bit 4

- Writing 1 to this field will cause the device to reset
- Read is zero

6.3.1.4 Stop Disable (STOP_DISABLE)—Bits 3–2

- 00 = Stop mode will be entered when the 56800E core executes a STOP instruction
- 01 = The 56800E STOP instruction will not cause entry into Stop mode
- 10 = Stop mode will be entered when the 56800E core executes a STOP instruction and the STOP_DISABLE field is write-protected until the next reset
- 11 = The 56800E STOP instruction will not cause entry into Stop mode and the STOP_DISABLE field is write-protected until the next reset

6.3.1.5 Wait Disable (WAIT_DISABLE)—Bits 1–0

- 00 = Wait mode will be entered when the 56800E core executes a WAIT instruction
- 01 = The 56800E WAIT instruction will not cause entry into Wait mode
- 10 = Wait mode will be entered when the 56800E core executes a WAIT instruction and the WAIT_DISABLE field is write-protected until the next reset
- 11 = The 56800E WAIT instruction will not cause entry into Wait mode and the WAIT_DISABLE field is write-protected until the next reset

6.3.9.3 Digital-to-Analog Clock Enable 1 (DAC1)—Bit 13

- 0 = The clock is not provided to the DAC1 module (the DAC1 module is disabled)
- 1 = The clock is enabled to the DAC1 module

6.3.9.4 Digital-to-Analog Clock Enable 0 (DAC0)—Bit 12

- 0 = The clock is not provided to the DAC0 module (the DAC0 module is disabled)
- 1 = The clock is enabled to the DAC0 module

6.3.9.5 Reserved—Bit 11

This bit field is reserved. It must be set to 0.

6.3.9.6 Analog-to-Digital Converter Clock Enable (ADC)—Bit 10

- 0 = The clock is not provided to the ADC module (the ADC module is disabled)
- 1 = The clock is enabled to the ADC module

6.3.9.7 Reserved—Bits 9–7

This bit field is reserved. Each bit must be set to 0.

6.3.9.8 Inter-Integrated Circuit IPBus Clock Enable (I2C)—Bit 6

- 0 = The clock is not provided to the I^2C module (the I^2C module is disabled)
- 1 = The clock is enabled to the I^2C module

6.3.9.9 Reserved—Bit 5

This bit field is reserved. It must be set to 0.

6.3.9.10 QSCI 0 Clock Enable (QSCI0)—Bit 4

- 0 = The clock is not provided to the QSCI0 module (the QSCI0 module is disabled)
- 1 = The clock is enabled to the QSCI0 module

6.3.9.11 Reserved—Bit 3

This bit field is reserved. It must be set to 0.

6.3.9.12 QSPI 0 Clock Enable (QSPI0)—Bit 2

- 0 = The clock is not provided to the QSPI0 module (the QSPI0 module is disabled)
- 1 = The clock is enabled to the QSPI0 module

6.3.9.13 Reserved—Bit 1

This bit field is reserved. It must be set to 0.

6.3.9.14 PWM Clock Enable (PWM)—Bit 0

- 0 = The clock is not provided to the PWM module (the PWM module is disabled)

- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.11.5 Reserved—Bit 11

This bit field is reserved. It must be set to 0.

6.3.11.6 Analog-to-Digital Converter Clock Stop Disable (ADC_SD)—Bit 10

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.11.7 Reserved—Bits 9–7

This bit field is reserved. Each bit must be set to 0.

6.3.11.8 Inter-Integrated Circuit Clock Stop Disable (I2C_SD)—Bit 6

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.11.9 Reserved—Bit 5

This bit field is reserved. It must be set to 0.

6.3.11.10 QSCI0 Clock Stop Disable (QSCI0_SD)—Bit 4

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.11.11 Reserved—Bit 3

This bit field is reserved. It must be set to 0.

6.3.11.12 QSPI0 Clock Stop Disable (QSPI0_SD)—Bit 2

Each bit controls clocks to the indicated peripheral.

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.11.13 Reserved—Bit 1

This bit field is reserved. It must be set to 0.

6.3.11.14 PWM Clock Stop Disable (PWM_SD)—Bit 0

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.19.1 Reserved—Bits 15–9

This bit field is reserved. Each bit must be set to 0.

6.3.19.2 Configure GPIOB11 (GPS_B11)—Bit 8

This field selects the alternate function for GPIOB11.

- 0 = CMPBO - Comparator B Output (default)
- 1 = Reserved

6.3.19.3 Reserved—Bit 7

This bit field is reserved. It must be set to 0.

6.3.19.4 Configure GPIOB10 (GPS_B10)—Bit 6

This field selects the alternate function for GPIOB10.

- 0 = CMPAO - Comparator A Output (default)
- 1 = Reserved

6.3.19.5 Reserved—Bits 5–1

This bit field is reserved. Each bit must be set to 0.

6.3.19.6 Configure GPIOB7 (GPS_B7)—Bit 0

This field selects the alternate function for GPIOB7.

- 0 = TXD0 - QSCI0 Transmit Data (default)
- 1 = SCL - I^2C Serial Clock

6.3.20 SIM GPIO Peripheral Select Register for GPIOC and GPIOD (SIM_GPSCD)

See **Section 6.3.16** for general information about GPIO Peripheral Select Registers.

Base + $17	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	GPS_D5	0	0	0	0	0	0	0	0	0	0	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-23 GPIO Peripheral Select Register for GPIOC and GPIOD (SIM_GPSCD)

6.3.20.1 Reserved—Bits 15–13

This bit field is reserved. Each bit must be set to 0.

6.3.20.2 Configure GPIOD5 (GPS_D5)—Bit 12

This field selects the alternate function for GPIOD5.

Base + $1A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	IPS2_ TA3	0	0	0	IPS2_ TA2	0	0	0	IPS2_ TA1	0	0	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-27 Internal Peripheral Source Select Register for TMRA (SIM_IPS2)

6.3.23.1 Reserved—Bits 15–13

This bit field is reserved. Each bit must be set to 0.

6.3.23.2 Select Input Source for TA3 (IPS2_TA3)—Bit 12

This field selects the alternate input source signal to feed Quad Timer A, input 3.

- 0 = I/O pin (External) - Use Timer A3 input/output pin
- 1 = PWM SYNC (Internal) - Use PWM reload synchronization signal

6.3.23.3 Reserved—Bits 11–9

This bit field is reserved. Each bit must be set to 0.

6.3.23.4 Select Input Source for TA2 (IPS2_TA2)—Bit 8

This field selects the alternate input source signal to feed Quad Timer A, input 2.

- 0 = I/O pin (External) - Use Timer A2 input/output pin
- 1 = CMPBO (Internal) - Use Comparator B output

6.3.23.5 Reserved—Bits 7–5

This bit field is reserved. Each bit must be set to 0.

6.3.23.6 Select Input Source for TA1 (IPS2_TA1)—Bit 4

This field selects the alternate input source signal to feed Quad Timer A, input 1.

- 0 = I/O pin (External) - Use Timer A1 input/output pin
- 1 = CMPAO (Internal) - Use Comparator A output

6.3.23.7 Reserved—Bits 3–0

This bit field is reserved. Each bit must be set to 0.

For Timer A to detect the PWM SYNC signal, the clock rate of both the PWM module and Timer A module must be identical, at either the system clock rate or 3X system clock rate.

6.4 Clock Generation Overview

The SIM uses the master clock (2X system clock) at a maximum of 64MHz from the OCCS module to produce a system clock at a maximum of 32MHz for the peripheral, core, and memory. It divides the

security mode is enabled, the 56F8025 will disable the core EOnCE debug capabilities. Normal program execution is otherwise unaffected.

7.2 Flash Access Lock and Unlock Mechanisms

There are several methods that effectively lock or unlock the on-chip flash.

7.2.1 Disabling EOnCE Access

On-chip flash can be read by issuing commands across the EOnCE port, which is the debug interface for the 56800E CPU. The TCK, TMS, TDO, and TDI pins comprise a JTAG interface onto which the EOnCE port functionality is mapped. When the device boots, the chip-level JTAG TAP (Test Access Port) is active and provides the chip's boundary scan capability and access to the ID register, but proper implementation of flash security will block any attempt to access the internal flash memory via the EOnCE port when security is enabled.

7.2.2 Flash Lockout Recovery Using JTAG

If the device is secured, one lockout recovery mechanism is the complete erasure of the internal flash contents, including the configuration field, thus disabling security (the protection register is cleared). This does not compromise security, as the entire contents of the user's secured code stored in flash are erased before security is disabled on the device on the next reset or power-up sequence.

To start the lockout recovery sequence via JTAG, the JTAG public instruction (LOCKOUT_RECOVERY) must first be shifted into the chip-level TAP controller's instruction register. Once the LOCKOUT_RECOVERY instruction has been shifted into the instruction register, the clock divider value must be shifted into the corresponding 7-bit data register. After the data register has been updated, the user must transition the TAP controller into the RUN-TEST/IDLE state for the lockout sequence to commence. The controller must remain in this state until the erase sequence is complete. Refer to the **56F802x and 56F803x Peripheral Reference Manual** for more details, or contact Freescale.

Note: Once the lockout recovery sequence has completed, the user must reset both the JTAG-TAP controller and device to return to normal unsecured operation. Power-on reset will reset both too.

7.2.3 Flash Lockout Recovery using CodeWarrior

CodeWarrior can unlock a device by selecting the *Debug* menu, then selecting *DSP56800E*, followed by *Unlock Flash*. Another mechanism is also built into CodeWarrior using the device's memory configuration file. The command "*Unlock_Flash_on_Connect 1*" in the *.cfg* file accomplishes the same task as using the *Debug* menu.

This lockout recovery mechanism is the complete erasure of the internal flash contents, including the configuration field, thus disabling security (the protection register is cleared).

7.2.4 Flash Lockout Recovery without mass erase

A user can un-secure a secured device by programming the word $0000 into program memory location $00 7FF7. After completing the programming, both the JTAG TAP controller and the device must be reset

Table 8-2 GPIO External Signals Map (Continued)

GPIO Function	Peripheral Function	LQFP Package Pin	Notes
GPIOD0	TDI	41	Defaults to TDI
GPIOD1	TDO	44	Defaults to TDO
GPIOD2	TCK	19	Defaults to TCK
GPIOD3	TMS	43	Defaults to TMS
GPIOD4	EXTAL	38	Defaults to D4
GPIOD5	XTAL / CLKIN	37	SIM register SIM_GPSCD is used to select between XTAL and CLKIN. Defaults to D5

8.3 Reset Values

Tables **8-1** and **8-2** detail registers for the 56F8035/56F8025; Figures **8-1** through **8-4** summarize register maps and reset values.

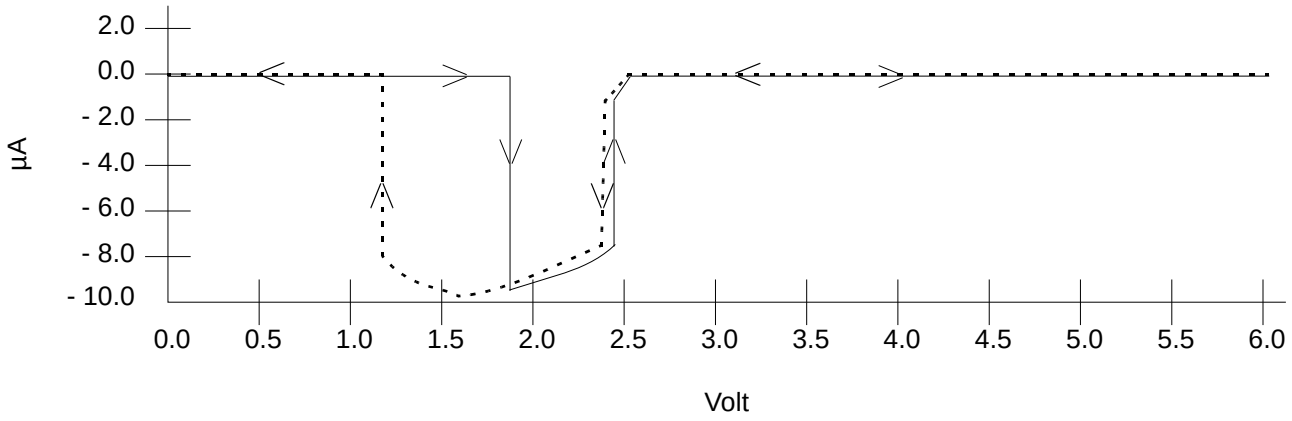

Figure 10-1 I_{IN}/I_{OZ} vs. V_{IN} (Typical; Pull-Up Disabled)

Table 10-6 Current Consumption per Power Supply Pin

Mode	Conditions	Typical @ 3.3V, 25°C		Maximum@ 3.6V, 25°C	
		I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
RUN	32MHz Device Clock Relaxation Oscillator on PLL powered on Continuous MAC instructions with fetches from Program Flash All peripheral modules enabled. TMR and PWM using 1X Clock ADC/DAC powered on and clocked Comparator powered on	48mA	18.8mA	—	—
WAIT	32MHz Device Clock Relaxation Oscillator on PLL powered on Processor Core in WAIT state All Peripheral modules enabled. TMR and PWM using 1X Clock ADC/DAC/Comparator powered off	29mA	0µA	—	—
STOP	4MHz Device Clock Relaxation Oscillator on PLL powered off Processor Core in STOP state All peripheral module and core clocks are off ADC/DAC/Comparator powered off	5.4mA	0µA	—	—

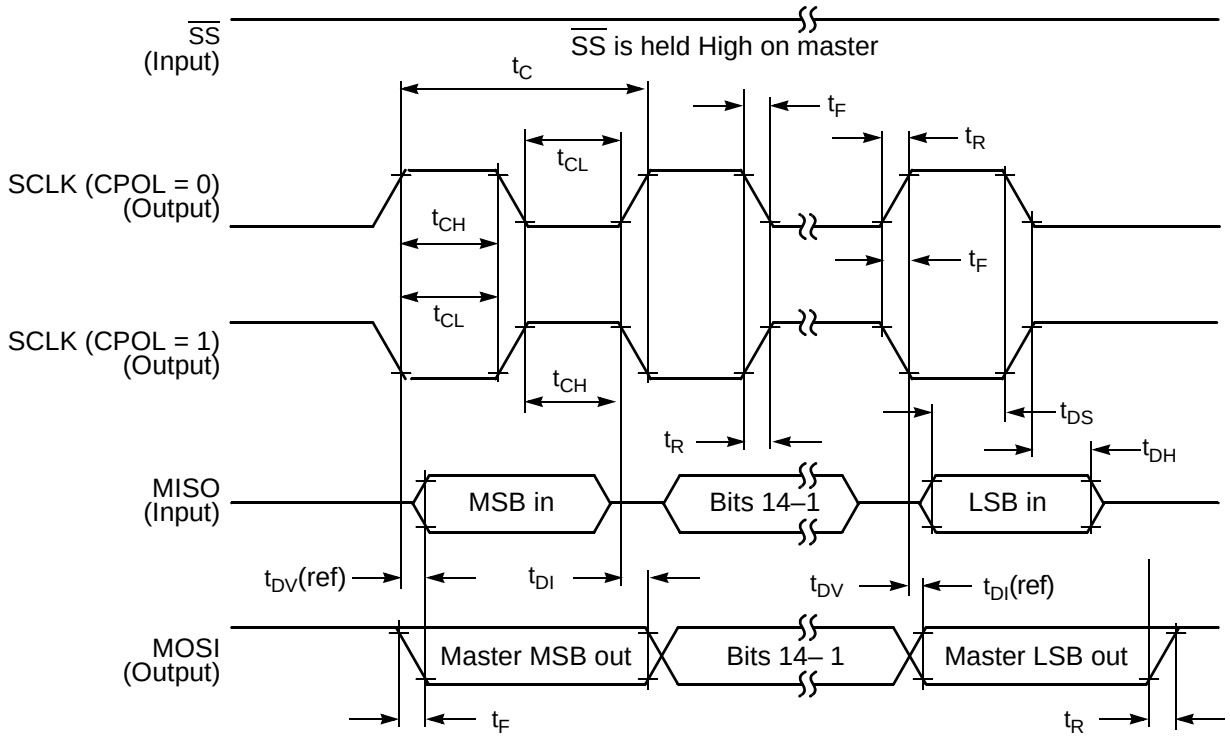

Figure 10-8 SPI Master Timing (CPHA = 1)

Table 14-1 Legacy and Revised Acronyms (Continued)

Register Name	Peripheral Reference Manual		Data Sheet		Processor Expert Acronym	Memory Address	
	New Acronym	Legacy Acronym	New Acronym	Legacy Acronym		Start	End
Clear Receive Done Interrupt Register	CLRRXDONE		I2C_CLR_RXDONE		I2C_CLR_RXDONE	0xF2AC	
Clear Activity Interrupt Register	CLRACT		I2C_CLRACTIVITY		I2C_CLRACTIVITY	0xF2AE	
Clear Stop Detect Interrupt Register	CLRSTPDET		I2C_CLR_STOPDET		I2C_CLR_STOPDET	0xF2B0	
Clear Start Detect Interrupt Register	CLRSTDET		I2C_CLR_STAR_DET		I2C_CLR_STAR_DET	0xF2B2	
Clear General Call Interrupt Register	CLRGC		I2C_CLR_GENCALL		I2C_CLR_GENCALL	0xF2B4	
Enable Register	ENBL		I2C_ENABLE		I2C_ENABLE	0xF2B6	
Status Register	STAT		I2C_STAT		I2C_STAT	0xF2B8	
Transmit FIFO Level Register	TXFLR		I2C_TXFLR		I2C_TXFLR	0xF2BA	
Receive FIFO Level Register	RXFLR		I2C_RXFLR		I2C_RXFLR	0xF2BC	
Transmit Abort Source Register	TXABRTSRC		I2C_TX_ABRTSRC		I2C_TX_ABRTSRC	0xF2C0	
Component Parameter 1 Register	COMPARM1		I2C_COMPARM1		I2C_COMPARM1	0xF2FA	
Component Parameter 2 Register	COMPARM2		I2C_COMPARM2		I2C_COMPARM2	0xF2FB	
Component Version 1 Register	COMVER1		I2C_COMVER1		I2C_COMVER1	0xF2FC	
Component Version 2 Register	COMVER2		I2C_COMVER2		I2C_COMVER2	0xF2FD	
Component Type 1 Register	COMTYP1		I2C_COMTYP1		I2C_COMTYP1	0xF2FE	
Component Type 2 Register	COMTYP2		I2C_COMTYP2		I2C_COMTYP2	0xF2FF	
On-Clock Chip Synthesis (OCCS) Module							
Control Register	CTRL	PLLCR	OCCS_CTRL	PLLCR	PLLCR	0xF130	
Divide-By Register	DIVBY	PLLDB	OCCS_DIVBY	PLLDB	PLLDB	0xF131	
Status Register	STAT	PLLSR	OCCS_STAT	PLLSR	PLLSR	0xF132	
Oscillator Control Register	OCTRL	OSCTL	OCCS_OCTRL	OSCTL	OSCTL	0xF135	
Clock Check Register	CLKCHK		OCCS_CLCHK	PLLCLCHK	OCCS_CLCHK	0xF136	
Protection Register	PROT		OCCS_PROT	PLLPROT	OCCS_PROT	0xF137	
Clock Divider Register	CLKDIV	FMCLKD	FM_CLKDIV	FMCLKD	FMCLKD	0xF400	
Configuration Register	CNFG	FMCR	FM_CNFG	FMCR	FMCR	0xF401	
Security High Half Register	SECHI	FMSECH	FM_SECHI	FMSECH	FMSECH	0xF403	
Security Low Half Register	SECLO	FMSECL	FM_SECLO	FMSECL	FMSECL	0xF404	