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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

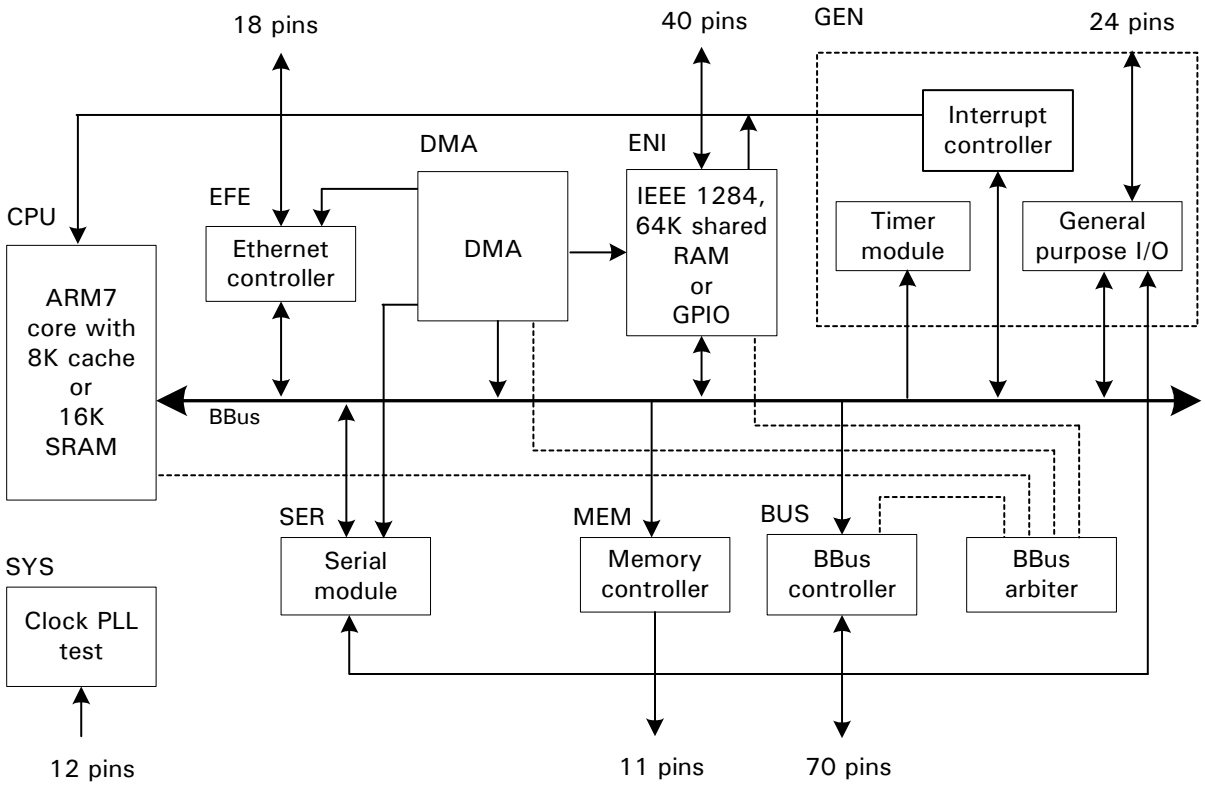
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Network Processor
Core Processor	ARM7®
Program Memory Type	External Program Memory
Controller Series	NET+50
RAM Size	16K x 8
Interface	EBI/EMI, Ethernet, DMA, HDLC, IEEE1284/ENI, SPI, UART
Number of I/O	40
Voltage - Supply	2.25V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	208-LFBGA
Supplier Device Package	208-BGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/digi-international/net-50-bin

NET+50 block diagram

The following diagram provides an overview of the modules that make up the NET+50 device:



Key features

CPU core

- Full 32-bit ARM7TDMI RISC processor
- 32-bit internal bus
- 16-bit Thumb mode
- 8 KB cache, configurable as 16 KB RAM
- 15 general-purpose 32-bit registers
- 32-bit program counter and status register
- Five supervisor modes, one user mode

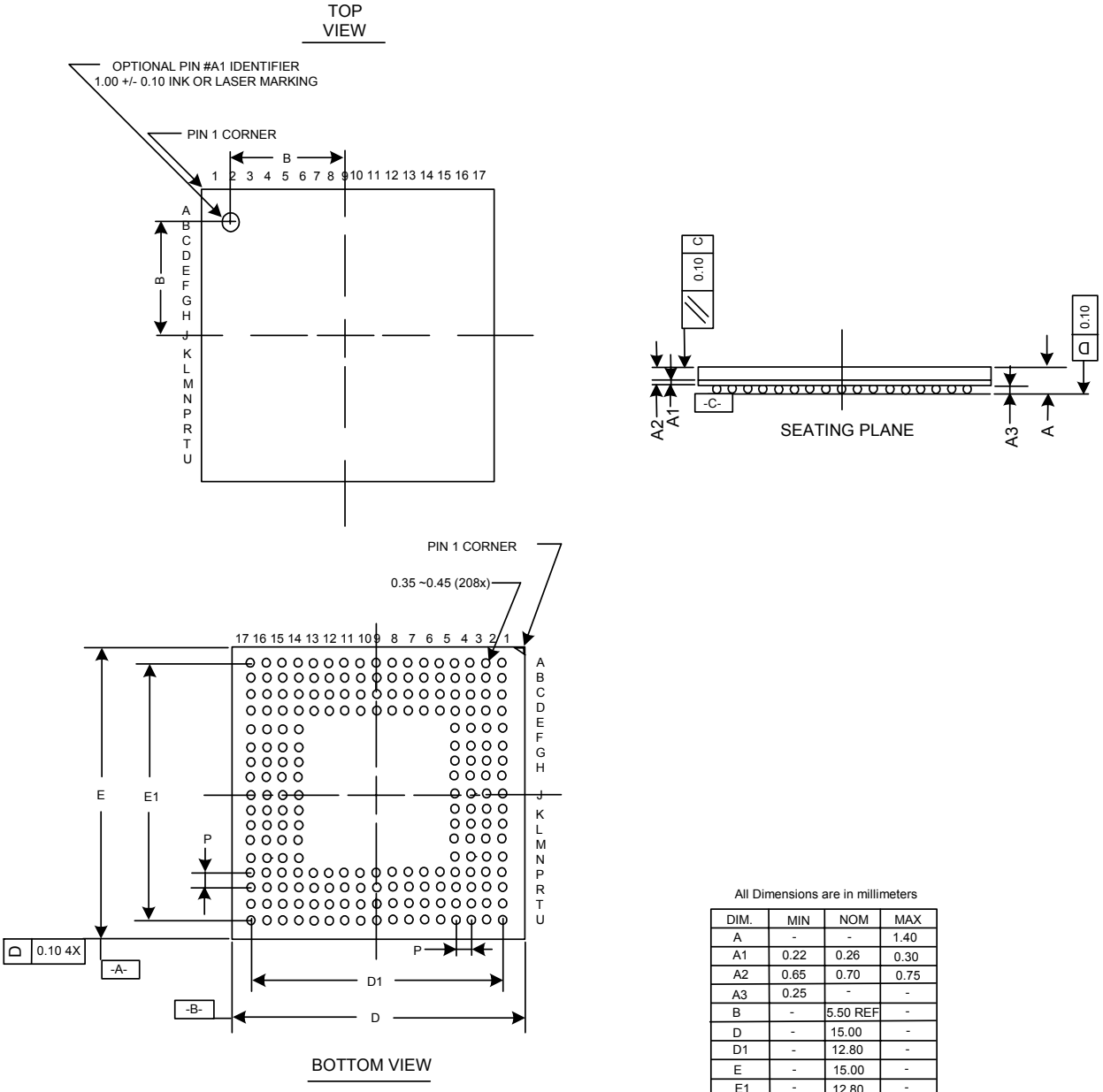
Integrated 10/100 Ethernet MAC

- 10/100 MII-based PHY interface
- 10 Mbit ENDEC interface
- Supports TP-PMD and fiber-PMD devices
- Full-duplex and half-duplex modes
- Optional 4B/5B coding
- Full statistics gathering (SNMP and RMON)
- Station, broadcast, and multicast address detection and filtering
- 128-byte transmit FIFO, 2 KB receive FIFO
- Intelligent receive-side buffer selection

Packaging dimensions and pinout

The NET+50 is available in two package options — a ball-grid array (BGA) or a plastic quad flat pack (PQFP).

BGA packaging and pinout diagram



All Dimensions are in millimeters

DIM.	MIN	NOM	MAX
A	-	-	1.40
A1	0.22	0.26	0.30
A2	0.65	0.70	0.75
A3	0.25	-	-
B	-	5.50 REF	-
D	-	15.00	-
D1	-	12.80	-
E	-	15.00	-
E1	-	12.80	-
P	-	0.80	-

System bus interface (cont.)

Signal	BGA	PQFP	I/O	OD	Description
ADDR11	C3 †	99	I/O	4	
ADDR10	A5 †	98	I/O	4	
ADDR9	D4 †	97	I/O	4	
ADDR8	C4 †	96	I/O	4	
ADDR7	B5 †	95	I/O	4	
ADDR6	A6 †	94	I/O	4	
ADDR5	D5 †	93	I/O	4	
ADDR4	C5 †	92	I/O	4	
ADDR3	B6 †	91	I/O	4	
ADDR2	A7 †	90	I/O	4	
ADDR1	D6 †	89	I/O	4	
ADDR0	C6 †	88	I/O	4	
DATA31	T3	162	I/O	4	Data bus
DATA30	R4	161	I/O	4	
DATA29	U3	160	I/O	4	
DATA28	U2	159	I/O	4	
DATA27	R2	155	I/O	4	
DATA26	R1	154	I/O	4	
DATA25	P1	153	I/O	4	
DATA24	P2	152	I/O	4	
DATA23	R3	151	I/O	4	
DATA22	N1	150	I/O	4	
DATA21	P4	149	I/O	4	
DATA20	P3	148	I/O	4	
DATA19	N2	147	I/O	4	
DATA18	M1	146	I/O	4	
DATA17	N4	145	I/O	4	
DATA16	L1	142	I/O	4	
DATA15	M4	141	I/O	4	
DATA14	M3	140	I/O	4	
DATA13	L2	139	I/O	4	
DATA12	K1	138	I/O	4	

System bus interface (cont.)

Signal	BGA	PQFP	I/O	OD	Description
DATA11	L4	137	I/O	4	
DATA10	L3	136	I/O	4	
DATA9	K2	135	I/O	4	
DATA8	J1	134	I/O	4	
DATA7	K4	133	I/O	4	
DATA6	K3	132	I/O	4	
DATA5	J4	129	I/O	4	
DATA4	J3	128	I/O	4	
DATA3	H2	127	I/O	4	
DATA2	G1	126	I/O	4	
DATA1	H4	125	I/O	4	
DATA0	H3	124	I/O	4	
TS*	no connect				
BE3*	G2	123	I/O	2	Byte enable D31:D24
BE2*	F1	122	I/O	2	Byte enable D23:D16
BE1*	G4	121	I/O	2	Byte enable D15:D08
BE0*	G3	120	I/O	2	Byte enable D07:D00
RW*	U4	163	I/O	2	Transfer direction
TA*	R5 †	165	I/O	8	Data transfer acknowledge
TEA*	T4 †	166	I/O	8	Transfer error/last acknowledge
BR*	no connect				
BG*	no connect				
BUSY*	no connect				

Chip select controller

Signal		BGA	PQFP	I/O	OD	Description	
CS0*		T11	191	O	4	Chip select (boot select)	
CS1*	RAS1*	R12	192	O	4	Chip select	DRAM RAS*
CS2*	RAS2*	P12	193	O	4	Chip select	DRAM RAS*
CS3*	RAS3*	U11	194	O	4	Chip select	DRAM RAS*
CS4*	RAS4*	T12	195	O	4	Chip select	DRAM RAS*
CAS3*	SDRAS*	T13	199	O	4	DRAM column strobe D31:24	SDRAM RAS*
CAS2*	SDCAS*	U12	198	O	4	DRAM column strobe D23:16	SDRAM CAS*
CAS1*	SDWE*	P13	197	O	4	DRAM column strobe D15:08	SDRAM WE*
CAS0*	SD(AP)	R13	196	O	4	DRAM column strobe D07:00	SDRAM (AP)
WE*		R11	190	O	4	Write enable	
OE*		P11	189	O	4	Output enable	

Ethernet interface

MII	10BaseT	BGA	PQFP	I/O	OD	MII	10BaseT
MDC	LB*	D7	85	O	2	MII clock	Loopback enable
MDIO	UTPSTP*	C7 †	84	I/O	2	MII data	Cable type
TXCLK	TXCLK	B8	83	I		TX clock	
TXD0	TXD	A9	82	O	2	TX data 0	TX data
TXD1	PDN* (OD)	D8	81	O	2	TX data 1	Power down
TXD2	NTHRES	C8	80	O	2	TX data 2	Normal threshold
TXD3	THIN	D9	77	O	2	TX data 3	Enable Thinnet
TXER	LTE	C9	76	O	2	TX code error	Link test enable
TXEN	TXEN	B10	75	O	2	TX enable	
COL	TXCOL	A11	74	I		Collision	
CRS	RXCRS	D10	73	I		Carrier sense	
RXCLK	RXCLK	C10	72	I		RX clock	
RXD0	RXD	B11	71	I		RX data 0	RX data
RXD1	MANSENSE	A12	70	I		RX data 1	Sense jumper
RXD2	JABBER	D11	69	I		RX data 2	Jabber
RXD3	REVPOL	C11	68	I		RX data 3	Reverse polarity
RXER	LINKPUL*	B12	67	I		RX error	Link pulse detection
RXDV	AUTOMAN	A13	66	I		RX data valid	10B2 selected

ENI/Parallel 1284 Interface (cont.)

IEEE1284	ENI	GPIO	BGA	PFQP	I/O	OD	Description
PSELECT1	PA12	GPIG4	J14	25	I		
PSELECT2	PA13	GPIOF3	H15	28	I/O	2	Or ENI DMA output PDRQI*
PSELECT3	PA14	GPIOF2	H14	29	I/O	2	Or ENI DMA output PDRQO*
PSELECT4	PA15	GPIG5	J17	30	I		Or ENI DMA input PDACK*
FAULT1*	PA16	GPIG6	H16	31	I		
FAULT2*	PCS*	GPIG7	H17	34	I		
FAULT3*	PRW*	GPIOF0	G14	33	I/O	2	
FAULT4*	PBRW*	GPIOF1	G15	32	I/O	2	

Clock generation

Signal	BGA	PQFP	I/O	OD	Description
XTAL1	U7	178	I		2.5 V crystal oscillator circuit
XTAL2	T8	179	O		
PLLVDD	U8	182			2.5 V PLL clean power
PLLLPF	P9	181			PLL loop filter capacitor
PLLVSS	R9	180			PLL clean ground
PLLTST*	P8 †	177	I		2.5 V PLL test mode
BISTEN*	R10 †	184	I		Enable internal BIST operation
SCANEN*	P10 †	185	I		Enable internal SCAN testing

System reset

Signal	BGA	PQFP	I/O	OD	Description
RESET*	T2 †	158	I		System reset *

Debug support for ARM core

Signal	BGA	PQFP	I/O	OD	Description
TDI	T6 †	171	I		Test data in
TDO	U5	170	O	2	Test data out
TMS	R7 †	172	I		Test mode select
TRST*	R8	174	I		Test mode reset (input current sink)
TCK	P7	173	I		Test mode clock

ARM debugging features

The ARM7TDMI core contains hardware extensions for advanced debugging. These extensions facilitate development and testing of application software, operating systems, and the hardware itself.

The debug extensions let you stop the core on a given instruction fetch (break-point) or data access (watchpoint), or asynchronously by a debug request. In such cases, the ARM processor is in *debug state* so you can examine the core's internal state and the system's external state. When the examination is complete, you can restore the core and system state, and resume program execution.

The ARM processor is put into debug state by an internal functional unit called *ICEBreaker*. In debug state, the core isolates itself from the memory system. You can examine the core while all other system activities — for example, DMA operations — continue normally.

You can examine the ARM processor's internal state through the 5-pin interface for debugging. This interface lets you serially insert instructions into the core's pipe-line without using the external data bus. Therefore, in debug state, you can insert a store-multiple into the instruction pipeline to dump the contents of the processor's registers. Data can be serially shifted out without affecting the rest of the system.

DC characteristics and other specifications

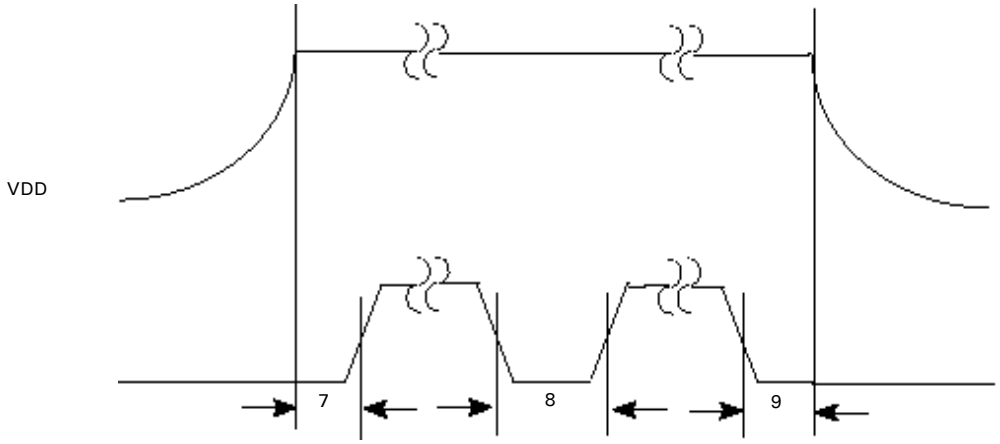
DC inputs

Symbol	Characteristic	Conditions	Min.	Typical	Max.	Unit
V_{DD}	DC supply voltage — core		2.25	2.5	2.75	V
V_{CC}	DC supply voltage — I/O		3.0	3.3	3.6	V
V_{IH}	Input high voltage		2.0		3.6	V
V_{IL}	Input low voltage		V_{SS} – 0.3		0.8	V
I_{IL}	Input buffer	$V_{IN} = V_{CC}$	-10		10	µA
	Input buffer with current sink		99		429	
I_{IH}	Input buffer	$V_{IN} = V_{SS}$	-10		10	µA
	Input buffer with current source		130		352	
C_{IN}	Input capacitance	Any input		7		pF
V_T	Switching threshold	Any input	1.4	2.0		V

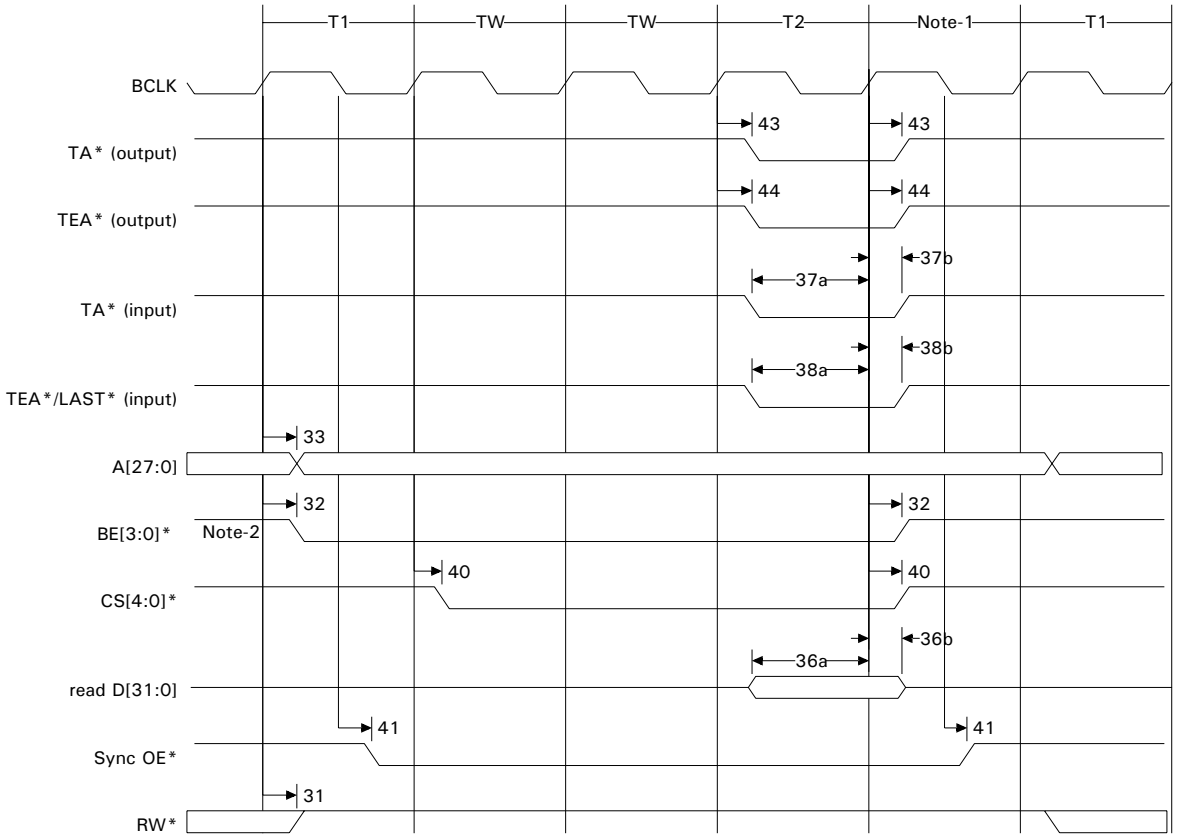
Timing data and diagrams

Reset timing

Number	Characteristic	Min.	Max.	Unit
7	V_{DD} at 3.0 V to RESET* high	40		ms
8	RESET* pulse width low	$10/F_{SYSCLK}$		µs
9	RESET* low to V_{DD} below 3.0 V	$8/F_{SYSCLK}$		µs



SRAM Sync Read (Wait = 2)



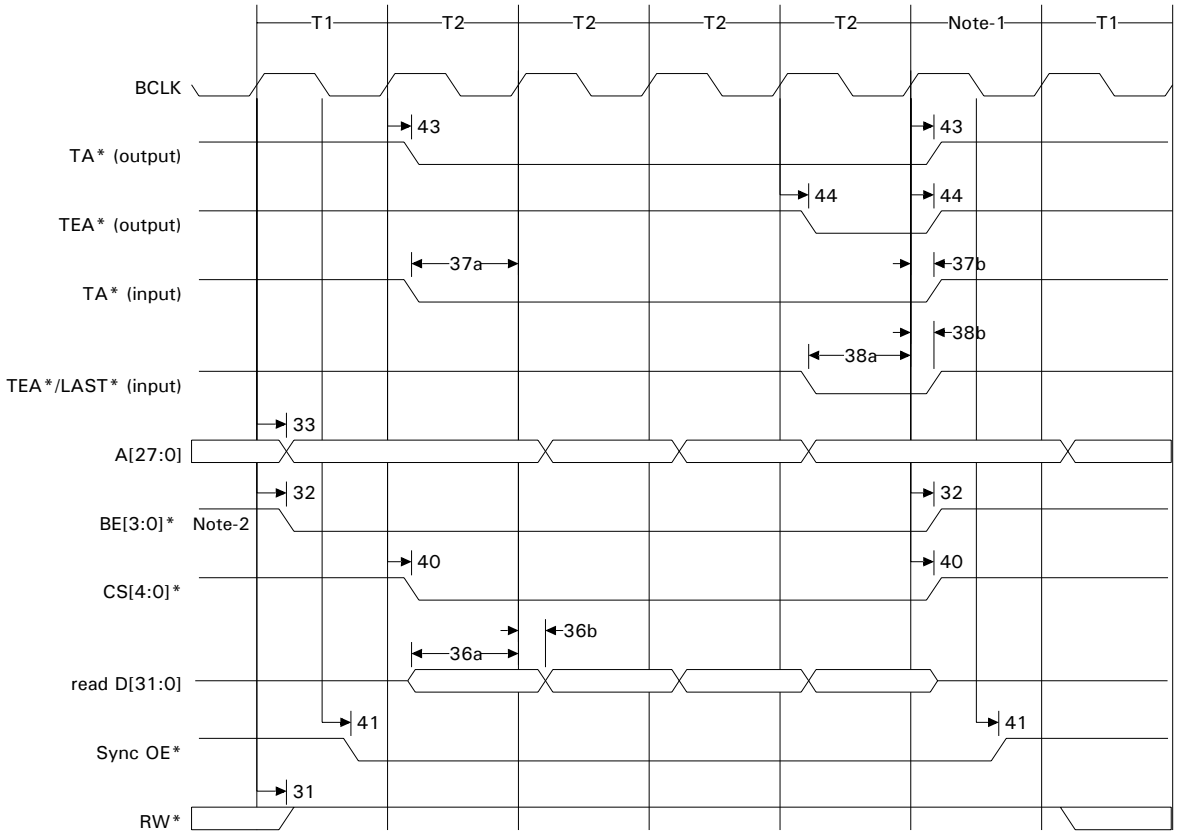
Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

SRAM Sync Burst Read (2-111, Wait = 0, BCYC = 00)



Notes:

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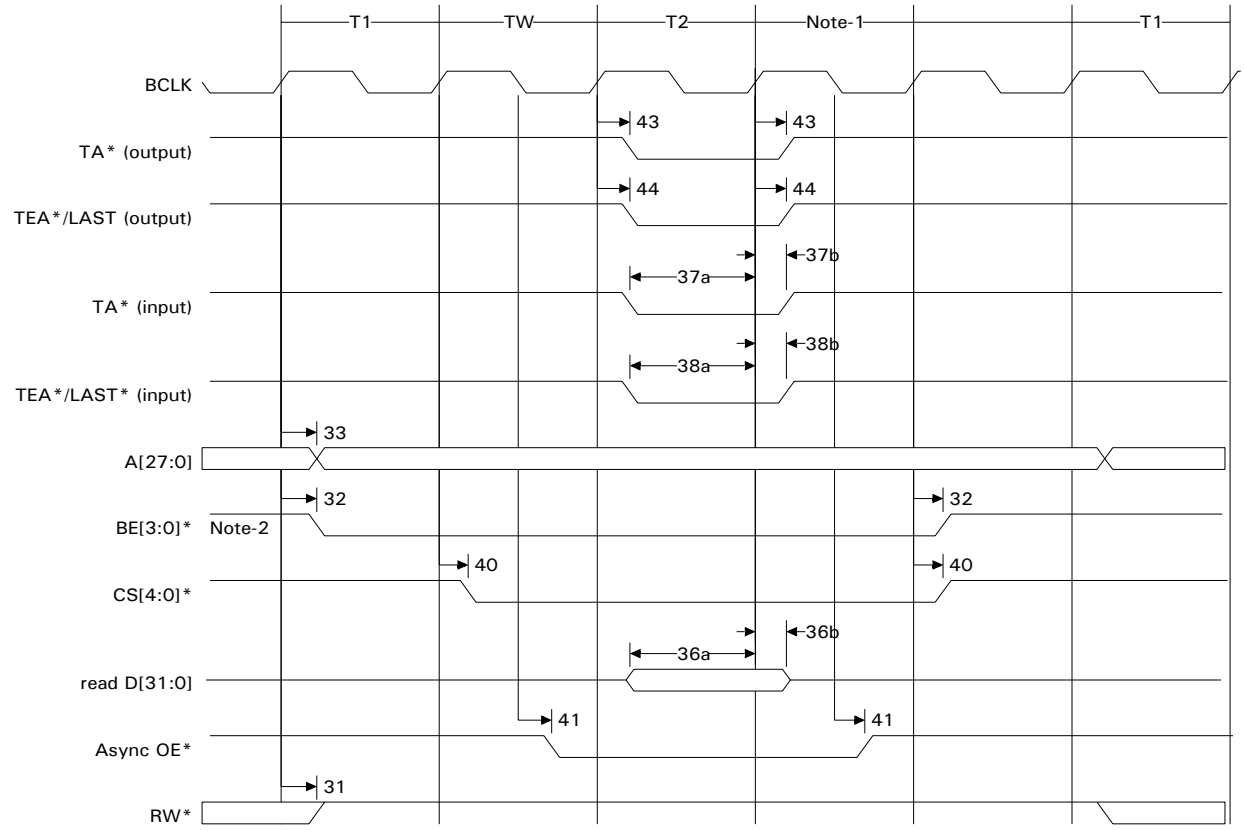
2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

SRAM Async Read (Wait = 2)



Notes:

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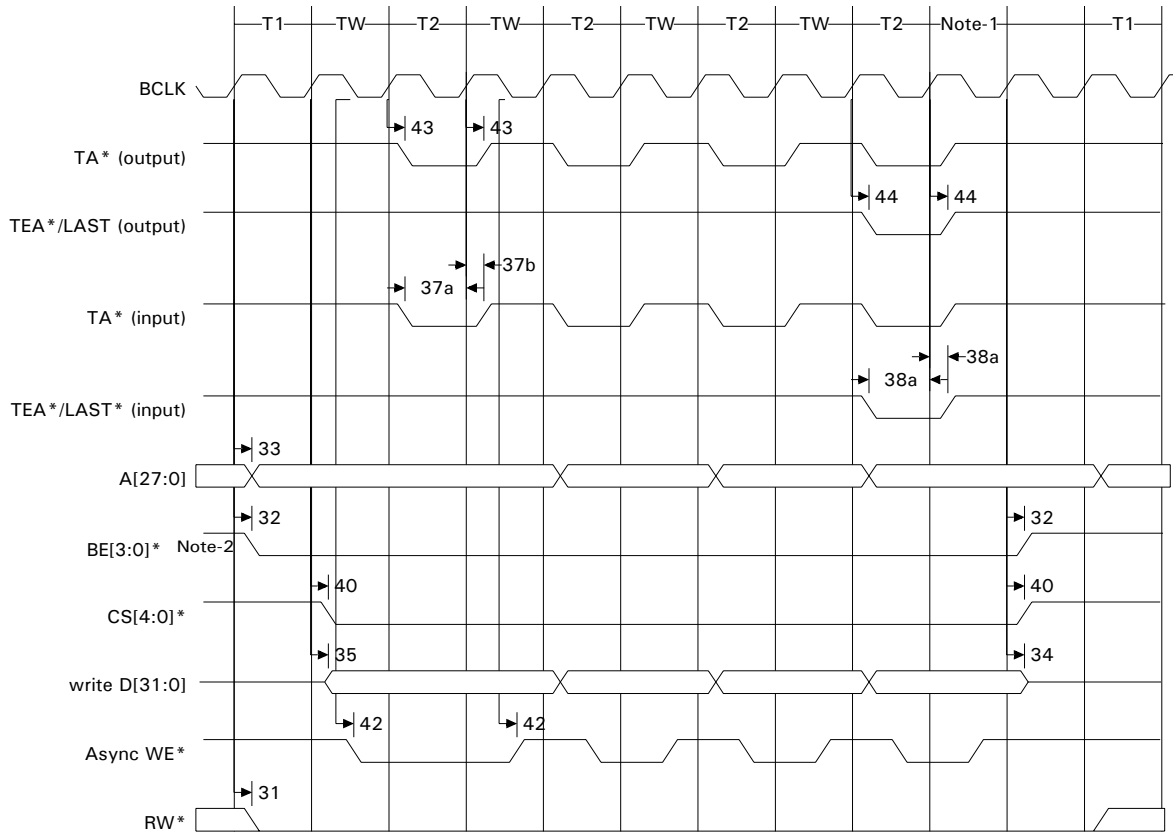
2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 The TW cycles are present when the WAIT field is set to 2 or more.

SRAM Async Burst Write (Wait = 2, BCYC = 01)



Notes:

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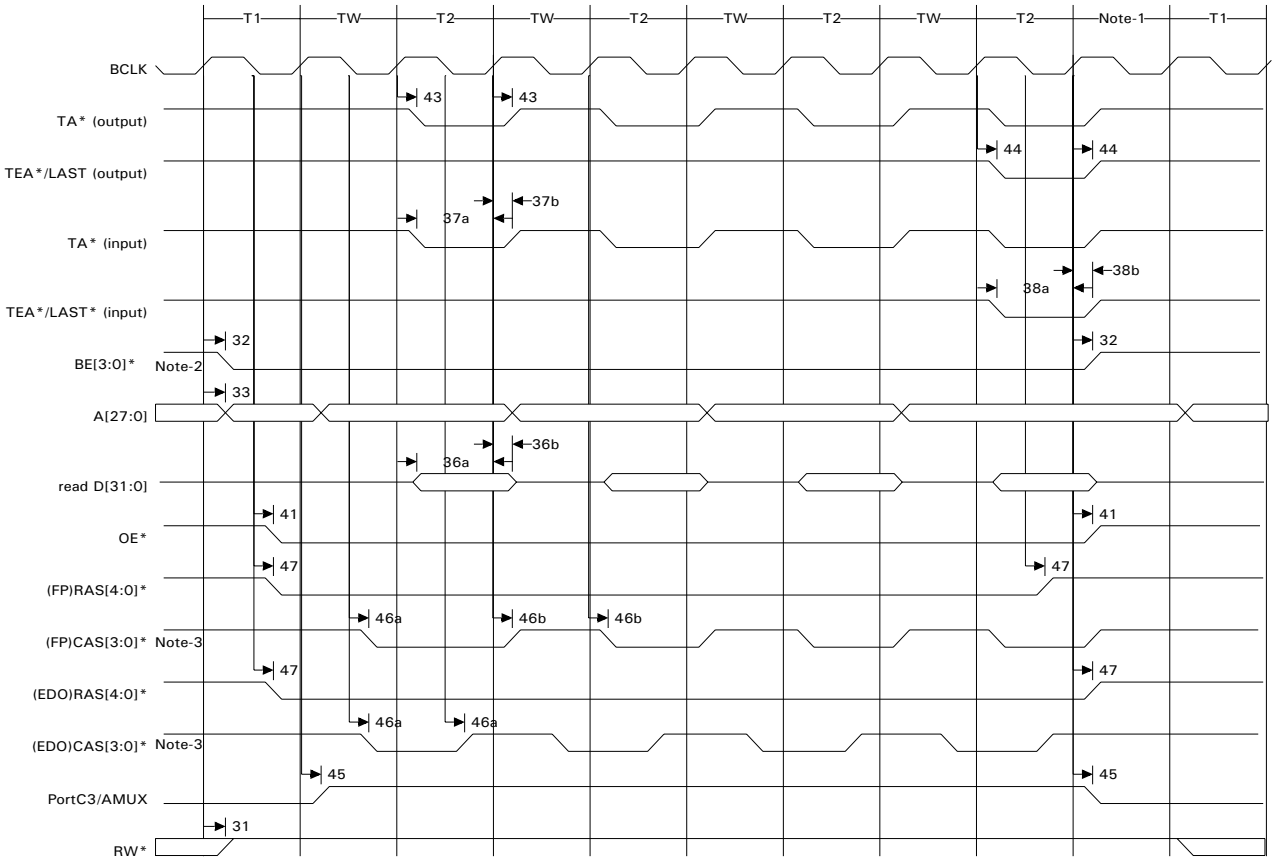
2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 The TW cycles are present when the WAIT field is set to 2 or more.

Fast Page and EDO DRAM Burst Read



Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

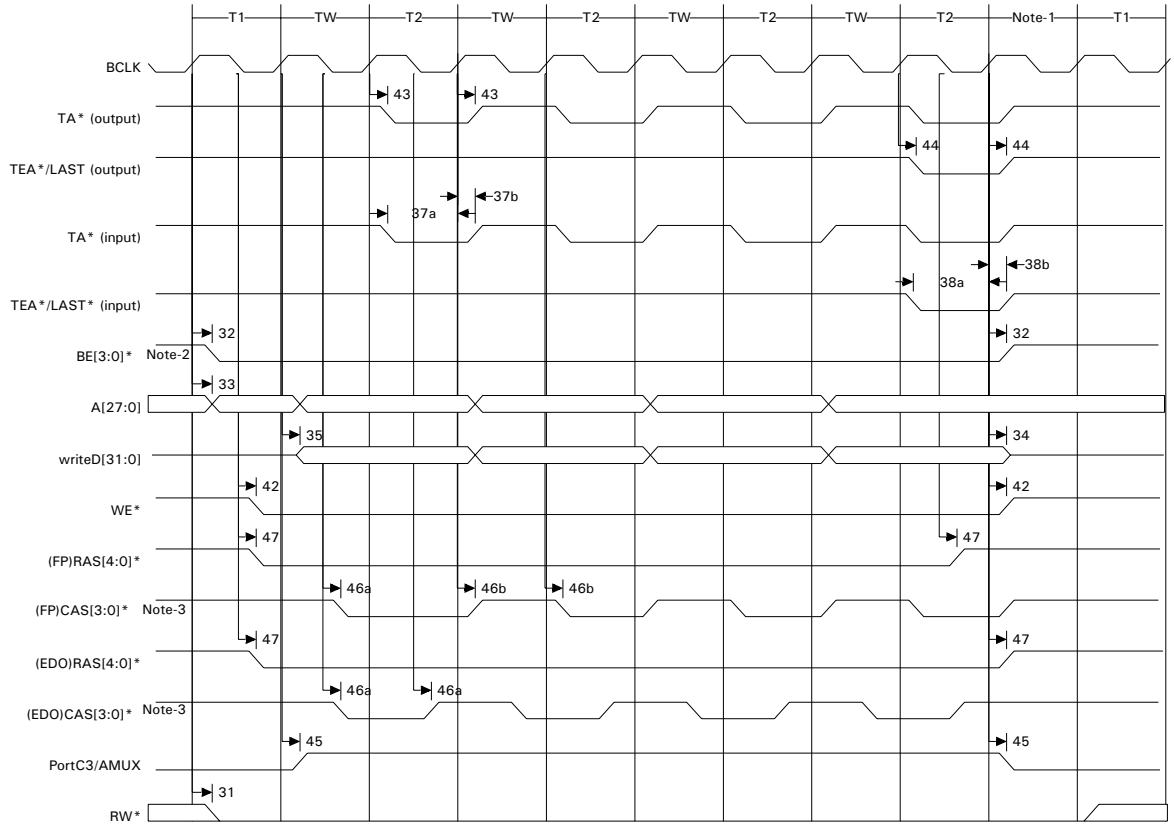
8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 Port size determines which CAS* signals are active:

8-bit port = CAS3*
16-bit port = CAS[3:2]*
32-bit port = CAS[3:0]*

4 The BCYC field in the Chip Select Option register should never be set to 00 for Fast Page and EDO DRAM.

Fast Page and EDO DRAM Burst Write



Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

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32-bit port = BE[3:0]*

3 Port size determines which CAS* signals are active:

8-bit port = CAS3*
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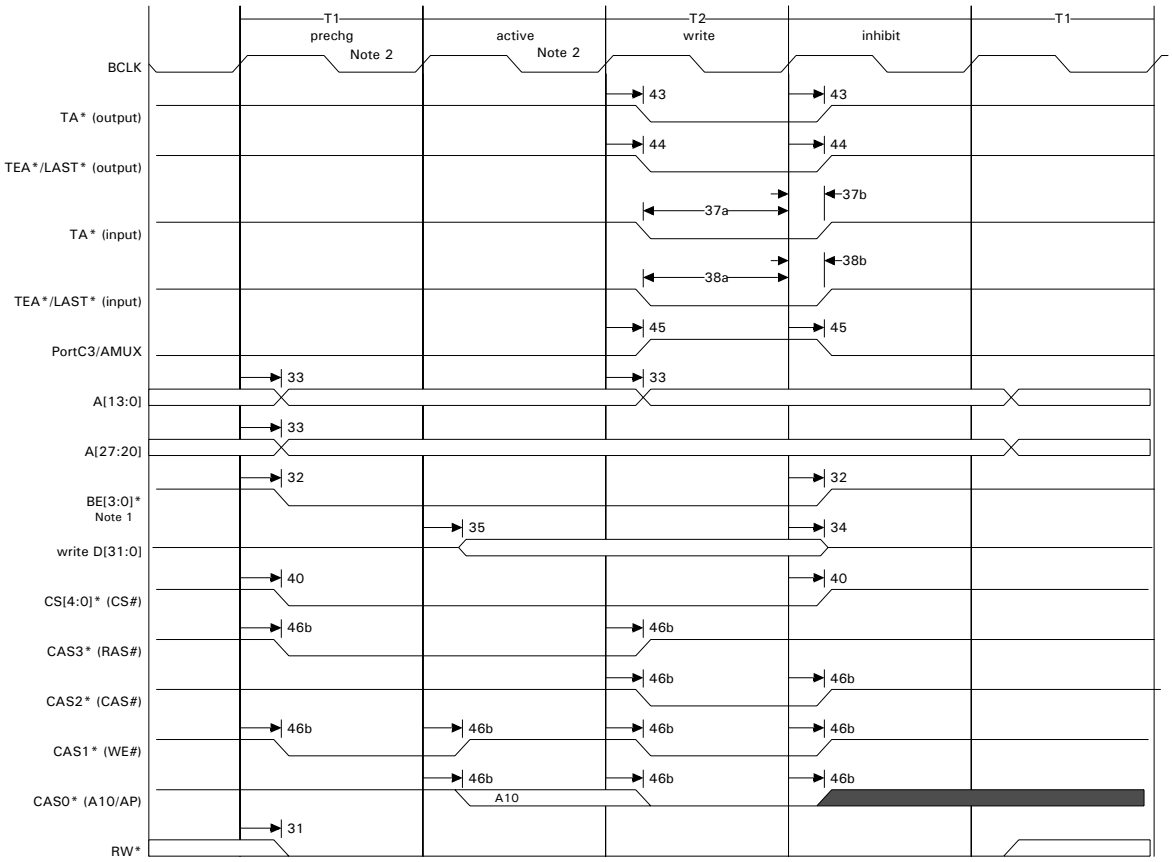
32-bit port = CAS[3:0]*

4 The BCYC field in the Chip Select Option register should never be set to 00 for Fast Page and EDO DRAM.

SDRAM Write



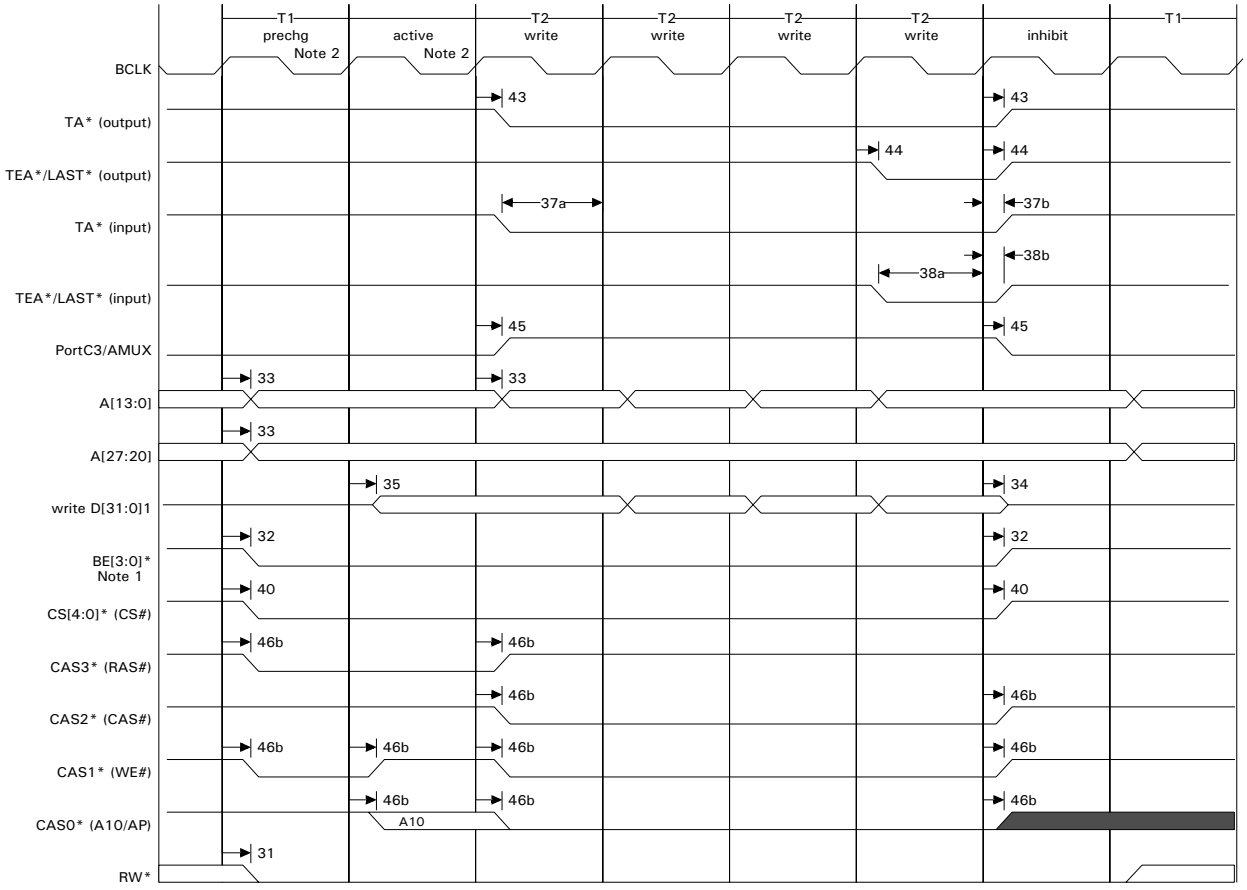
Notes:

1 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

2 The Precharge command or Active command or both are not always present. They depend on the address of the previous SDRAM access.When the Active command is not present, parameter 35 (write D[31:0]) is not valid until the Write (T2) cycle.

SDRAM Burst Write



Notes:

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8-bit port = BE3*
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2 The Precharge command or Active command or both are not always present. They depend on the address of the previous SDRAM access.When the Active command is not present, parameter 35 (write D[31:0]) is not valid until the Write (T2) cycle.

ENI timing

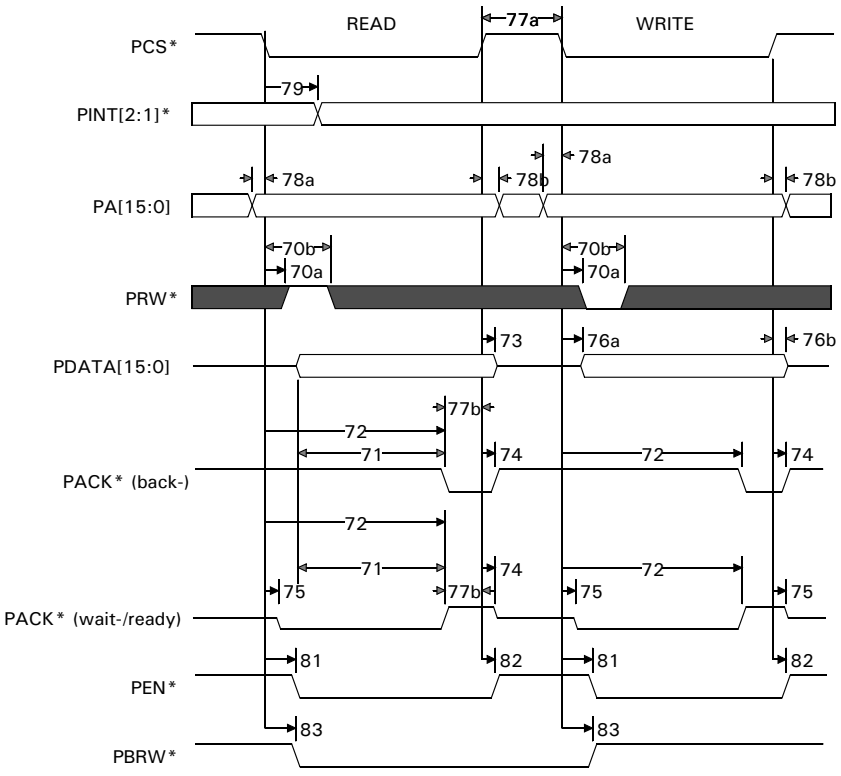
The data shown is independent of SYS_CLK and BCLK settings. Units are nanoseconds (ns).

Num	Characteristic	Note	Min	Max
70a	PCS*/PDACK* low to PRW* sampled	1		T_{SYS} - 2.5
70b	PCS*/PDACK* low to PRW* hold time	1	$4*T_{SYS}$	
71	Read Data Valid to PACK* valid		T_{SYS}	
72	PCS*/PDACK* low to PACK* low	3	T_{SYS}	$6*T_{SYS}$
72a	PCS* low to PACK* low	4	$7*T_{SYS}$	Determined by shared RAM access time
72b	PCS*/PACK* low to PACK* low	5	$2*T_{SYS}$	$4*T_{SYS}$
72c	PCS* low to PACK* valid (shared RAM only)	6	$7*T_{SYS}$	Determined by shared RAM access time
73	PCS*/PDACK* high to PDATA high impedance		0	7.84
74	PCS*/PDACK* high to PACK* high		0	13
75	PCS*/PDACK* low to PACK* (wait-) low		0	14
76a	PCS*/PDACK* low to Write Data valid			$2*T_{SYS}$
76b	PCS*/PDACK* high to Write Data hold time		0	
77a	PCS*/PDACK* width high (recovery)		16	
77b	PACK* low to PCS*/PDACK* high (hold)	8	0	
77c	PDACK* minimum low		120	
78a	Address valid to PCS* low		0	
78b	PCS* high to Address hold time		0	
79	PCS* low to PINT1/2 change (write)		$3*T_{SYS}$	$5*T_{SYS}$
80a	PDACK* low to PDRQI*, PDRQO* high			$5*T_{SYS}$
80b	PDRQO* high width		$5*T_{SYS}$	
80c	PDRQI* high width		$4*T_{SYS}$	
80d	PDACK* low to PINT2 low			14
80e	PDACK* high to PINT2 high		15	
81	PCS*/PDACK* low to PEN* low	2	$1*T_{SYS}$	$3*T_{SYS}$
82	PCS*/PDACK* high to PEN* high	2	0	13
83	PCS*/PDACK* low to PBRW* low	2	$1*T_{SYS}$	$2*T_{SYS}$
84a	PRW* valid to PDACK* low (setup)	1	0	
84b	PDACK* high to PRW* hold time	1	0	
85	PDACK* low to PDATA valid	7	$3*T_{SYS}$	$5*T_{SYS}$
85a	PDACK* low to PDATA valid	7	$1*T_{SYS}$	$2*T_{SYS}$

Notes:

1. Parameters 70a and 70b apply only when the ENI FAST bit is set to 0. When ENI FAST is set to 1, parameters 84a and 84b apply.
2. The PEN* and PBRW* signals control an external bi-directional data bus transceiver for the PDATA bus that can drive only 2 mA.
3. Parameter 72 applies only to ENI registers when FAST is set to 0. This does *not* apply to shared RAM access.
4. Parameter 72a applies to all shared RAM accesses when FAST is set to 0. The max specification for PCS* to PACK* valid is larger for shared RAM accesses. The additional delay depends on the speed of the external RAM assigned to provide the physical shared RAM. Consequently, the maximum specification for shared RAM accesses is system-dependent.
5. Parameter 72b applies to ENI register accesses when FAST is set to 1.
6. Parameter 72c applies to ENI shared RAM accesses when FAST is set to 1.
7. Parameter 85 applies when FAST is set to 0. Parameter 85a applies when FAST is set to 1.
8. Parameter 77c can be reduced to $3*T_{SYS}$ when FAST is set to 1.

ENI Shared RAM and Register Cycle timing



ENI Single Direction DMA timing