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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

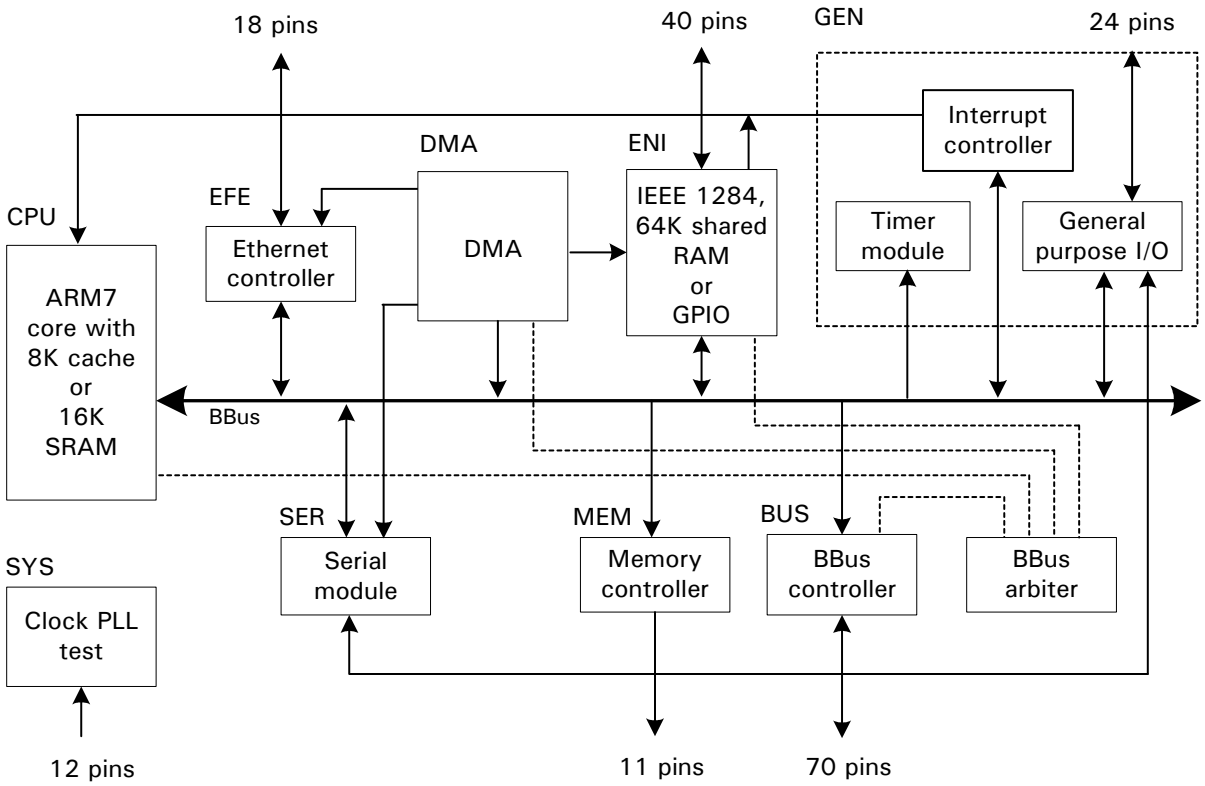
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Network Processor
Core Processor	ARM7®
Program Memory Type	External Program Memory
Controller Series	NET+50
RAM Size	16K x 8
Interface	EBI/EMI, Ethernet, DMA, HDLC, IEEE1284/ENI, SPI, UART
Number of I/O	40
Voltage - Supply	2.25V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	208-LFBGA
Supplier Device Package	208-BGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/digi-international/net-50-binp

NET+50 block diagram

The following diagram provides an overview of the modules that make up the NET+50 device:



Key features

CPU core

- Full 32-bit ARM7TDMI RISC processor
- 32-bit internal bus
- 16-bit Thumb mode
- 8 KB cache, configurable as 16 KB RAM
- 15 general-purpose 32-bit registers
- 32-bit program counter and status register
- Five supervisor modes, one user mode

Integrated 10/100 Ethernet MAC

- 10/100 MII-based PHY interface
- 10 Mbit ENDEC interface
- Supports TP-PMD and fiber-PMD devices
- Full-duplex and half-duplex modes
- Optional 4B/5B coding
- Full statistics gathering (SNMP and RMON)
- Station, broadcast, and multicast address detection and filtering
- 128-byte transmit FIFO, 2 KB receive FIFO
- Intelligent receive-side buffer selection

Operating frequency

- 44-MHz maximum system clock, requiring only a simple external 18.432-MHz crystal
- Supports external oscillators

ENI/P1284 Interface

- ENI host interface
- Four IEEE 1284 parallel ports
- 64 KB shared RAM ENI interface — 8- or 16-bit
- Full-duplex FIFO mode interface — 8- or 16-bit
- 32-byte transmit/receive FIFO mode FIFOs

Programmable timers

- Two independent, 27-bit timers (2 μs–20.7 hours)
- Watchdog timer (interrupt or reset on expiration)
- Bus timer

Serial port

- Two fully independent serial ports (UART, HDLC, SPI)
- Digital phase locked loop (DPLL) for receive clock extractions
- 32 byte transmit/receive FIFOs
- Internal programmable bit-rate generators
- Bit rates 75–230400 in 16X mode, 1200 bps – 4 Mbps in 1X mode. (Higher rates may be possible depending on the board design.)

10-channel DMA controller

- Two channels dedicated to Ethernet transmit and receive
- Four channels dedicated to serial transmit and receive
- Four channels (two at a time) configurable for external peripherals
- Flexible buffer management

Bus interface

- Five independent, programmable chip selects with 256 Mb addressing per chip select
- All chip selects support SRAM, EDO DRAM, SDRAM, and devices such as flash and EEPROM with SRAM interfaces
- Supports 8-, 16-, and 32-bit peripherals
- Dynamic bus sizing support
- Supports ASYNC and SYNC peripheral timing
- Internal DRAM address multiplexing
- Internal refresh controller (CAS before RAS)
- Burst-mode support
- 0–15 wait states per chip select
- Bootstrap support

Power and operating voltages

- 552 mW maximum (typically, 484 mW), outputs switching
- 3.3 V — I/O
- 2.5 V — core

Serial port (cont)

- Odd, even, or no parity
- 5, 6, 7, or 8 bits
- 1 or 2 stop bits
- Internal and external clock support
- Receive-side character and buffer gap timers
- Four receive-side data match detectors

UARTs, SPI, and GPIO

GPIO	UART / HDLC	Special / DMA mode	BGA	PQFP	I/O	OD	SPI slave mode	SPI master mode
PORTA7	TXDA		G17 †	38	I/O	2	SPI-S-TXD-O-A	SPI-M-TXD-O-A
PORTA6	DTRA*	DRQ1*	F16 †	39	I/O	2		
PORTA5	RTSA*		E15 †	40	I/O	2		
PORTA4		RXCA	E14 †	41	I/O	2	SPI-S-CLK-I-A	SPI-M-CLK-O-A
PORTA3	RXDA		F17 †	42	I/O	2	SPI-S-RXD-I-A	SPI-M-RXD-I-A
PORTA2	DSRA*	DAK1*	E16 †	43	I/O	2		
PORTA1	CTSA*		D15 †	44	I/O	2		
PORTA0	DCDA*	DON1*	D14 †	45	I/O	2		
PORTB7	TXDB		E17 †	46	I/O	2	SPI-S-TXD-O-B	SPI-M-TXD-O-B
PORTB6	DTRB*	DRQ2*	C15 †	47	I/O	2		
PORTB5	RTSB*		D16 †	48	I/O	2	Reject* Ethernet packet	
PORTB4		RXCB	D17 †	49	I/O	2	SPI-S-CLK-I-B	SPI-M-CLK-O-B
PORTB3	RXDB		C17 †	50	I/O	2	SPI-S-RXD-I-B	SPI-M-RXD-O-B
PORTB2	DSRB*	DAK2*	C16 †	51	I/O	2		
PORTB1	CTSB*		B16 †	54	I/O	2	RPSF* Ethernet frame boundary	
PORTB0	DCDB*	DON2*	A16 †	55	I/O	2		
PORTC7		TXCA	A15 †	56	I/O	2	SPI-S-EN-I-A	SPI-M-EN-O-A
PORTC6	RIA*	IRQO*	C14 †	57	I/O	2		
PORTC5		TXCB	B15 †	58	I/O	2	SPI-S-EN-I-B	SPI-M-EN-O-B
PORTC4	RIB*		A14 †	59	I/O	2		
PORTC3		AMUX	D13 †	60	I/O	8	Interrupt 3	
PORTC2			C13 †	61	I/O	8	Interrupt 2	
PORTC1			B14 †	62	I/O	8	Interrupt 1	
PORTC0			B13 †	63	I/O	8	Interrupt 0	

DMA controller module

DMA register key: 0xFF90*nnnn* where *nnnn* = DMAx + Offset							
DMA*x*:						**Offset:**	
1A:	00	2:	80	6:	100	00	Buffer descriptor pointer
1B:	20	3:	A0	7:	120	10	Buffer control register
1C:	40	4:	C0	8:	140	14	Buffer status register
1D:	60	5:	E0	9:	160		
				10:	180		

Examples:	
0xFF90 0000	DMA 1A buffer descriptor pointer
0xFF90 0010	DMA 1A buffer control register
0xFF90 0014	DMA 1A buffer status register

Ethernet controller module

Address	Register	Address	Register
0xFF80 0000	General control register	0xFF80 0440 – 0478	Transmit control registers
0xFF80 0004	General status register	0xFF80 0480 – 0488	Receive control registers
0xFF80 0008	FIFO data register	0xFF80 040C0	Link fail counter
0xFF80 000C	FIFO last word data register	0xFFB0 0500	10 Mbit jabber counter
0xFF80 0010	TX status register	0xFFB0 0504	10 Mbit loss of carrier counter
0xFF80 0014	RX status register	0xFFB0 0540 – 0550	MII control registers
0xFF80 0400 – 0404	MAC configuration and test registers	0xFFB0 0580 – 059C	Status registers
0xFF80 0408 – 040C	PCS configuration and test registers	0xFFB0 05C0	SAL address filter register
0xFF80 0410 – 0414	STL configuration and test registers	0xFFB0 05C4 – 05DC	SAL hash table registers

Serial controller module

Address	Register	Address	Register
0xFFD0 0000 – 0030	Channel 1 registers	0xFFD0 0040 – 0070	Channel 2 registers

ARM debugging features

The ARM7TDMI core contains hardware extensions for advanced debugging. These extensions facilitate development and testing of application software, operating systems, and the hardware itself.

The debug extensions let you stop the core on a given instruction fetch (break-point) or data access (watchpoint), or asynchronously by a debug request. In such cases, the ARM processor is in *debug state* so you can examine the core's internal state and the system's external state. When the examination is complete, you can restore the core and system state, and resume program execution.

The ARM processor is put into debug state by an internal functional unit called *ICEBreaker*. In debug state, the core isolates itself from the memory system. You can examine the core while all other system activities — for example, DMA operations — continue normally.

You can examine the ARM processor's internal state through the 5-pin interface for debugging. This interface lets you serially insert instructions into the core's pipe-line without using the external data bus. Therefore, in debug state, you can insert a store-multiple into the instruction pipeline to dump the contents of the processor's registers. Data can be serially shifted out without affecting the rest of the system.

DC characteristics and other specifications

DC inputs

Symbol	Characteristic	Conditions	Min.	Typical	Max.	Unit
V_{DD}	DC supply voltage — core		2.25	2.5	2.75	V
V_{CC}	DC supply voltage — I/O		3.0	3.3	3.6	V
V_{IH}	Input high voltage		2.0		3.6	V
V_{IL}	Input low voltage		V_{SS} – 0.3		0.8	V
I_{IL}	Input buffer	$V_{IN} = V_{CC}$	-10		10	µA
	Input buffer with current sink		99		429	
I_{IH}	Input buffer	$V_{IN} = V_{SS}$	-10		10	µA
	Input buffer with current source		130		352	
C_{IN}	Input capacitance	Any input		7		pF
V_T	Switching threshold	Any input	1.4	2.0		V

DC outputs

Symbol	Characteristic	Conditions	Min.	Max.	Unit
V_{OL}	Output low voltage		0	0.4	V
V_{OH}	Output high voltage		2.4	V_{CC}	V
I_{OZ}	High-Z leakage current	$V_O = V_{SS}$	-10	10	µA
I_{OS}	Output short circuit current	V_{CC} = 3.6V, V_O (low) = V_{CC}		55	µA
		V_{CC} = 3.6V, V_O (high) = V_{SS}	-55		
C_{IO}	Input/output capacitance	Any input, output, or I/O		7	pF

DC absolute maximum voltages

Characteristic	Min.	Max.
Supply voltage 2.5 V — core	-0.3	3.15
Supply voltage 3.3 V — I/O	-0.3	4.00
Input voltage	-0.3	4.50
Output voltage	-0.3	4.50

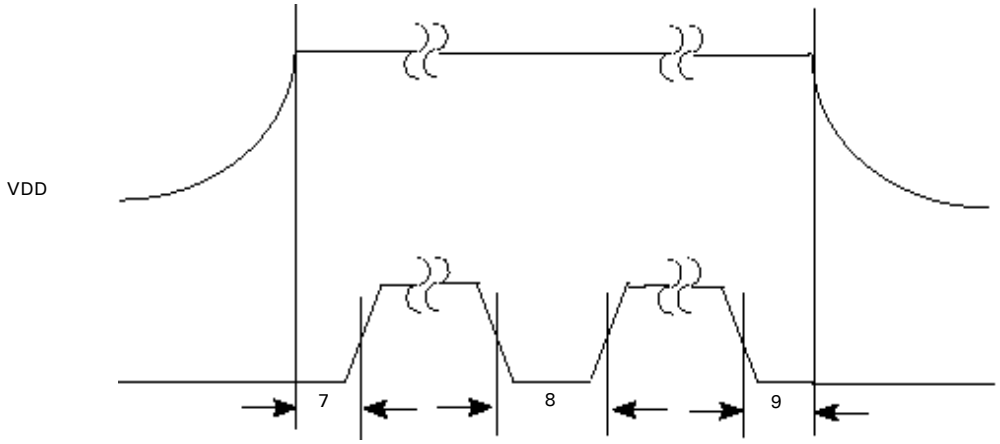
Temperature considerations

Characteristic	Min.	Max.
Thermal resistance — junction to ambient	37°C/W	
Operating junction temperature (°C)	-40°	100°
Operating ambient temperature (°C)	-40°	85°
Storage temperature (°C)	-60°	150°

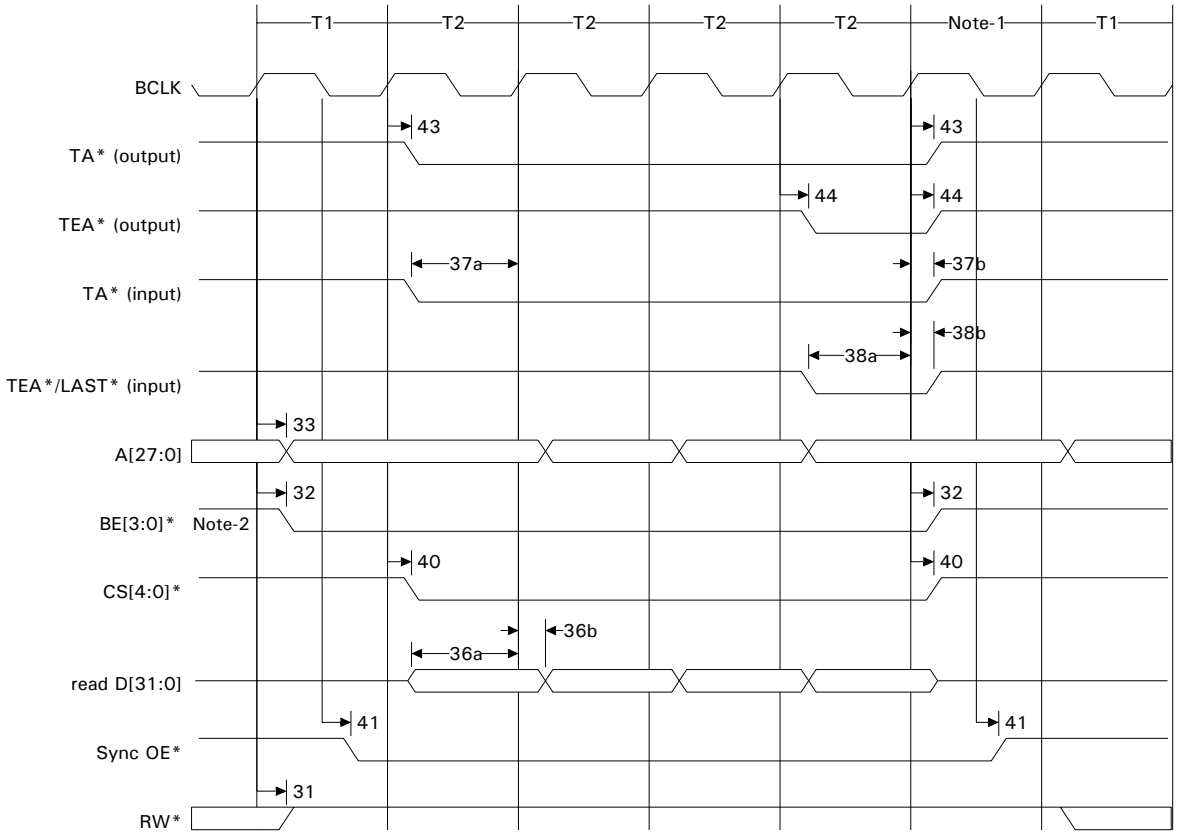
Timing data and diagrams

Reset timing

Number	Characteristic	Min.	Max.	Unit
7	V_{DD} at 3.0 V to RESET* high	40		ms
8	RESET* pulse width low	$10/F_{SYSCLK}$		µs
9	RESET* low to V_{DD} below 3.0 V	$8/F_{SYSCLK}$		µs



SRAM Sync Burst Read (2-111, Wait = 0, BCYC = 00)



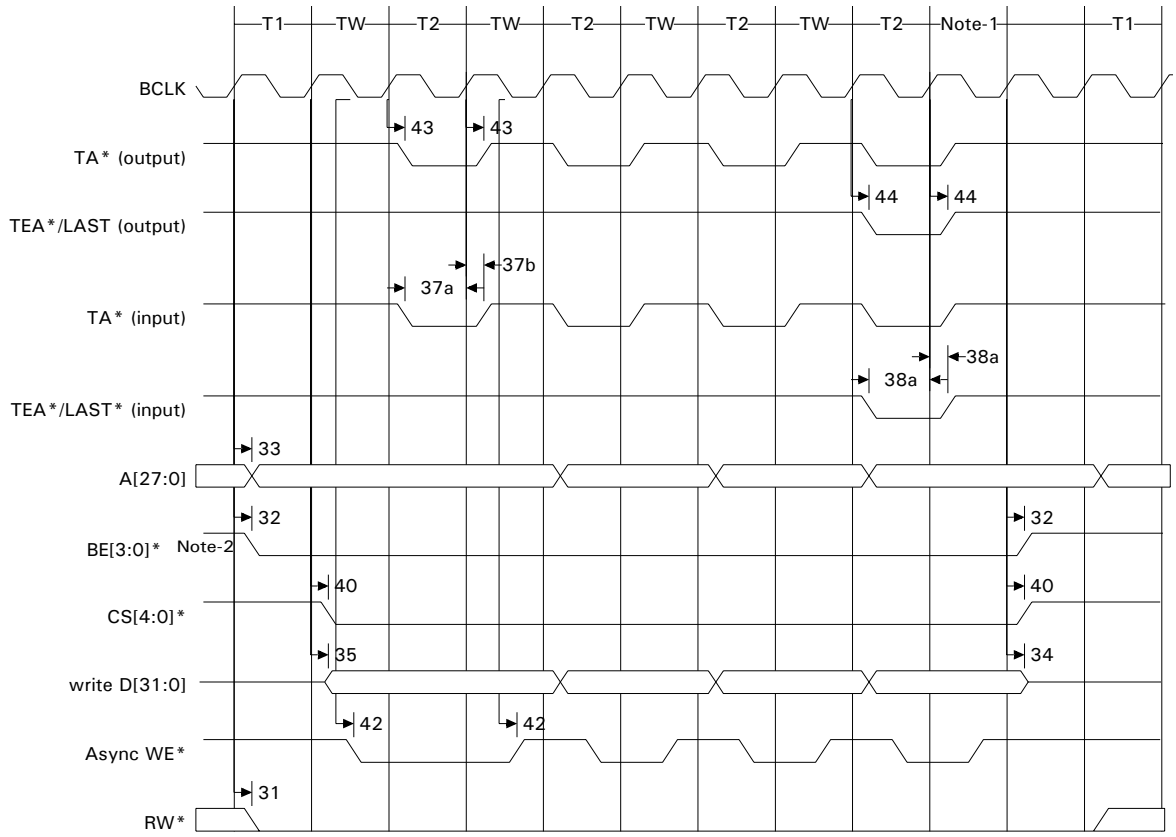
Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

SRAM Async Burst Write (Wait = 2, BCYC = 01)



Notes:

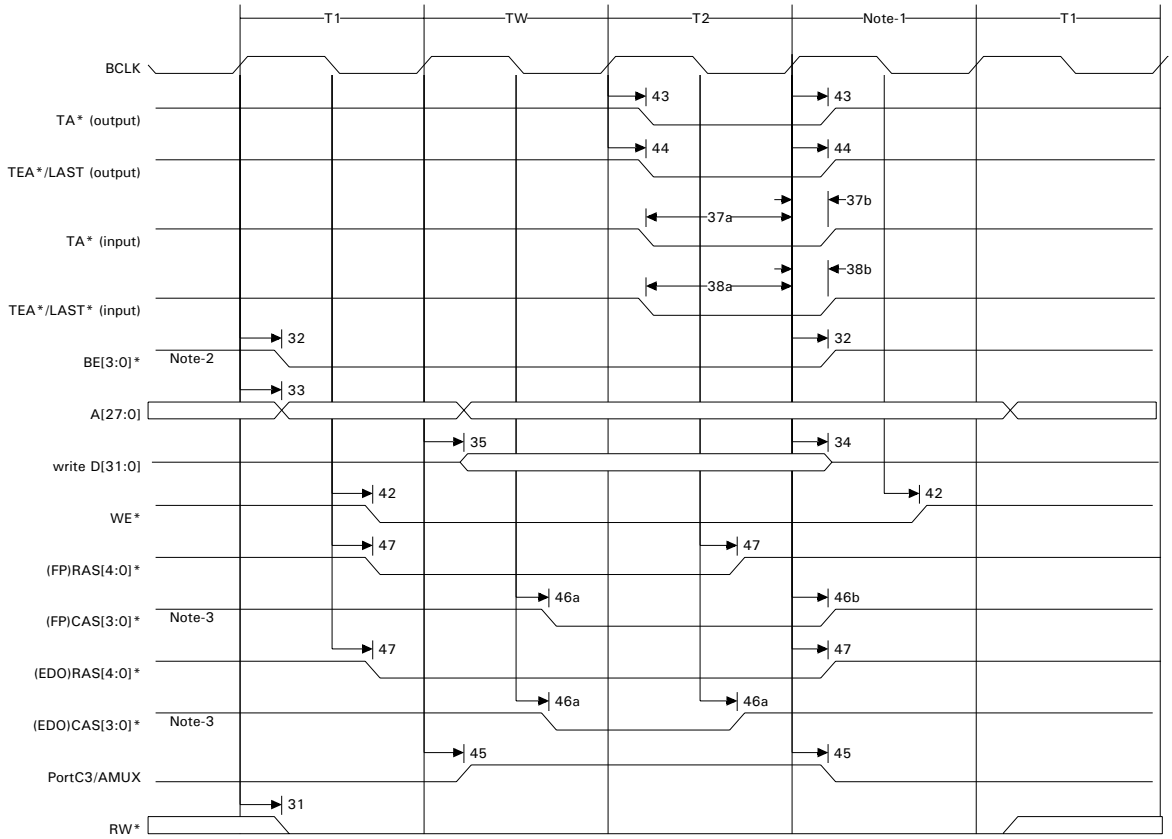
1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 The TW cycles are present when the WAIT field is set to 2 or more.

Fast Page and EDO DRAM Write



Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

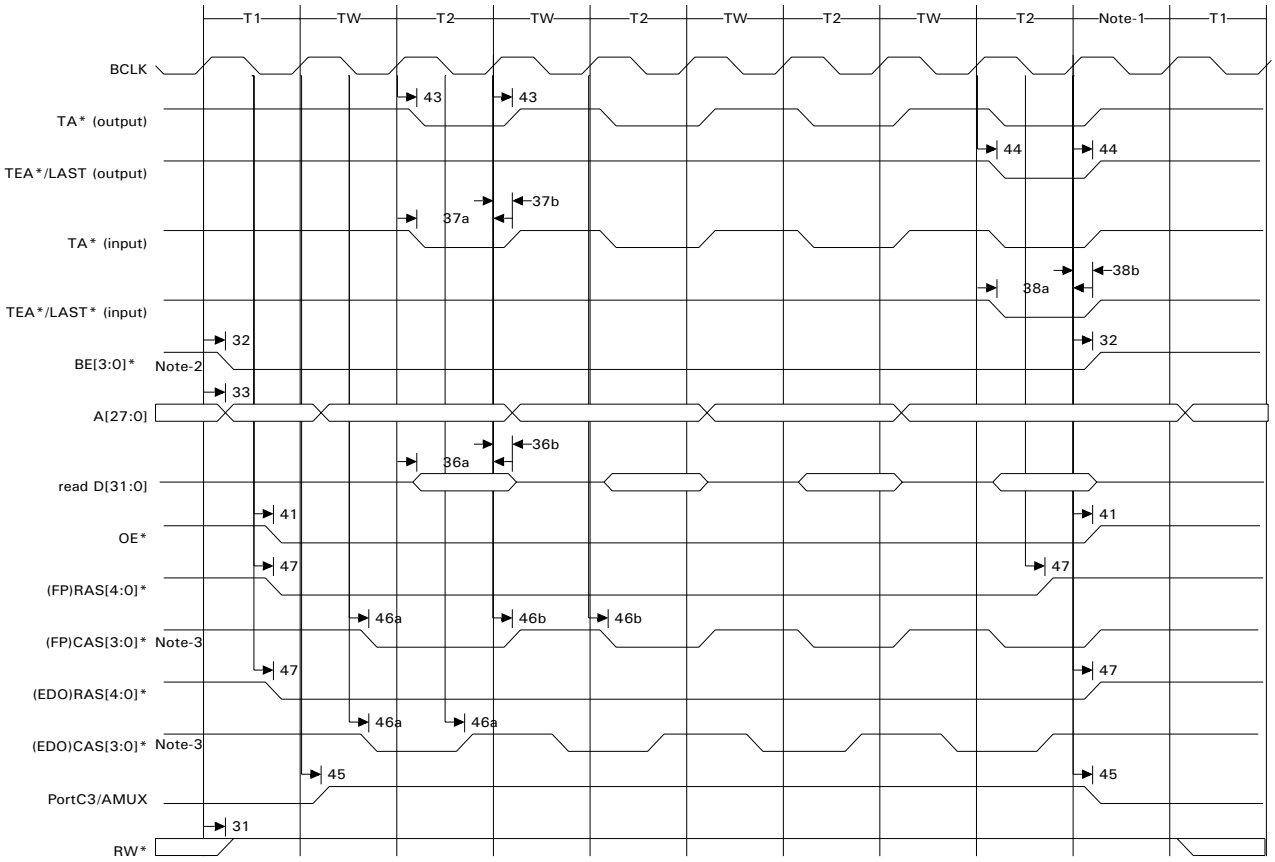
2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 Port size determines which CAS* signals are active:

8-bit port = CAS3*
16-bit port = CAS[3:2]*
32-bit port = CAS[3:0]*

Fast Page and EDO DRAM Burst Read



Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

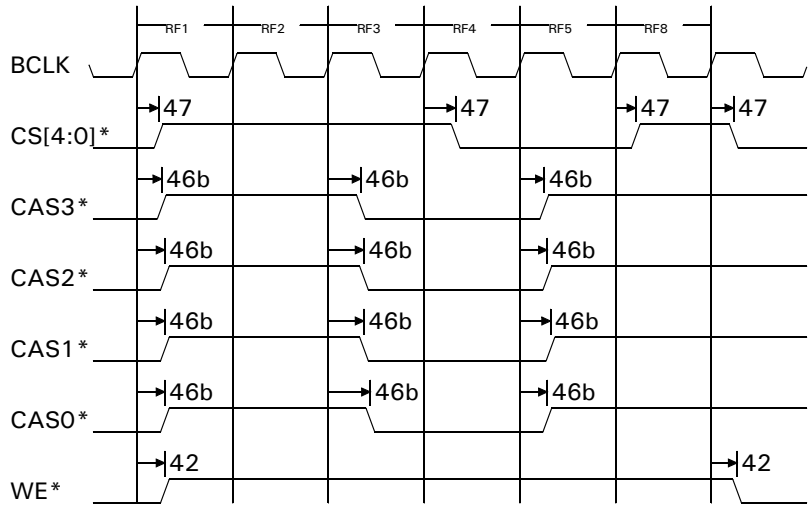
8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 Port size determines which CAS* signals are active:

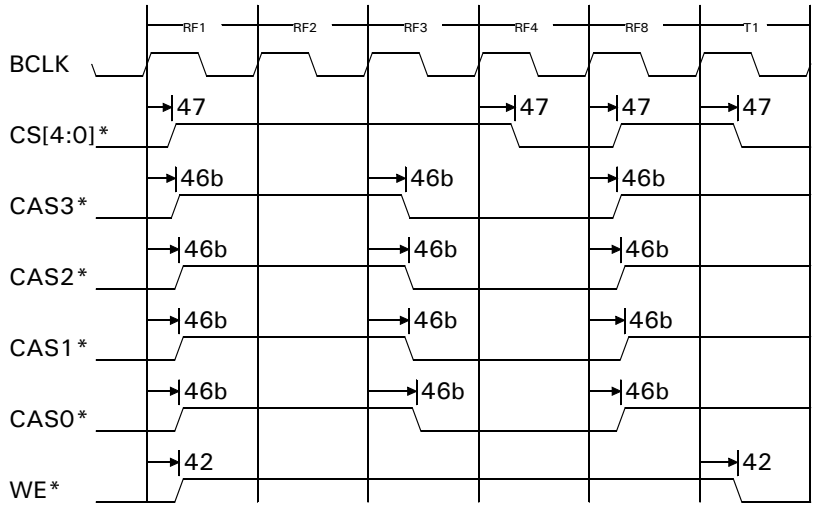
8-bit port = CAS3*
16-bit port = CAS[3:2]*
32-bit port = CAS[3:0]*

4 The BCYC field in the Chip Select Option register should never be set to 00 for Fast Page and EDO DRAM.

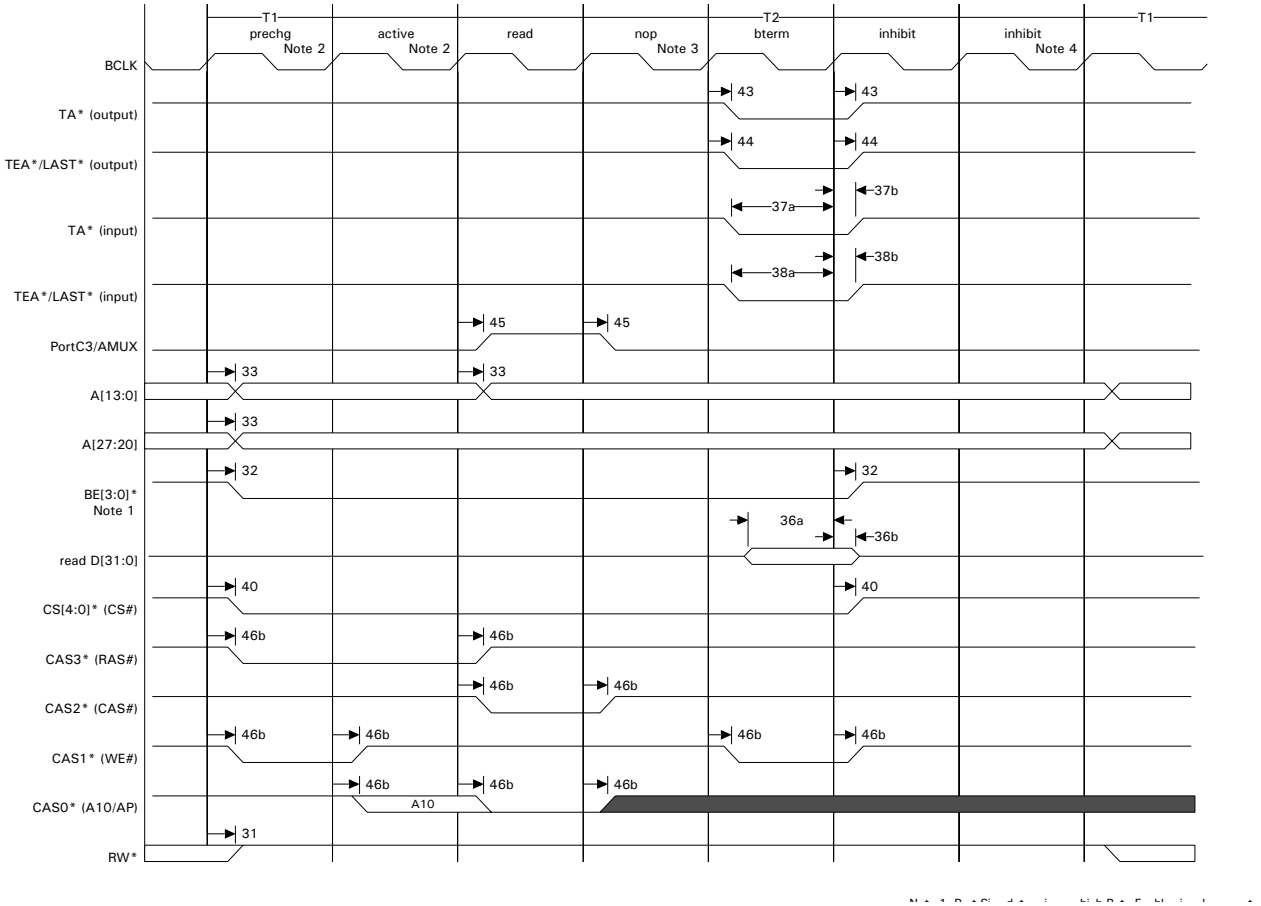
Fast Page and EDO DRAM Refresh (RCYC = 2)



Fast Page and EDO DRAM Refresh (RCYC = 3)



SDRAM Read (CAS Latency = 2)



Notes:

1 Port size determines which byte enable signals are active:

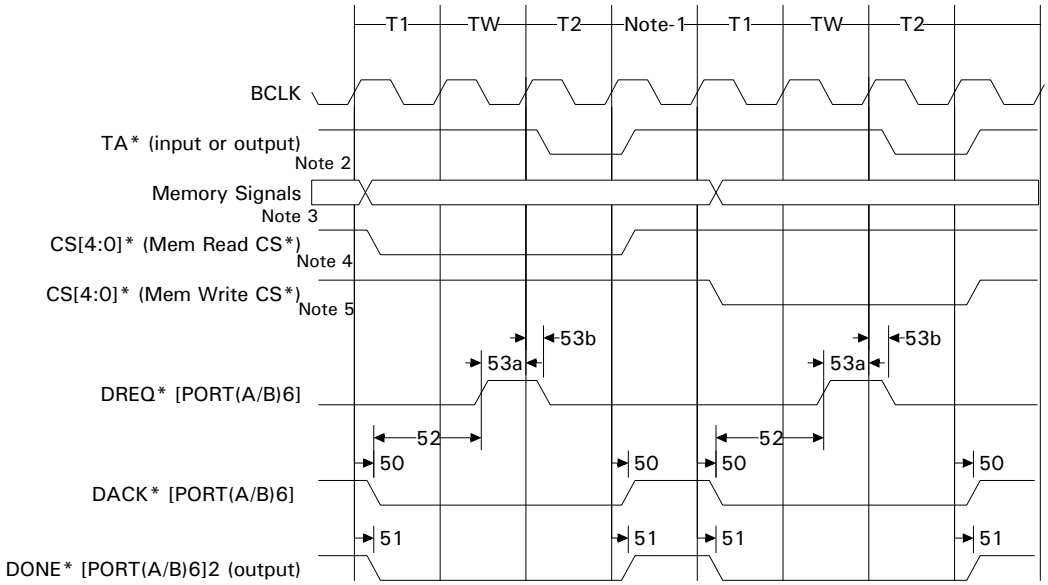
8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

2 The Precharge command or Active command or both are not always present. They depend on the address of the previous SDRAM access.

3 If CAS latency = 3, there are:

- Two NOPs between the Read and Burst Terminate commands
- Three Inhibit commands after the Burst Terminate command

External Memory to Memory DMA



Notes:

1 Between memory cycles, 0, 1, or 2 null periods can occur. Contact the factory for details.

2 TA* is shown here for reference. Its timing is available on the diagrams in the sections referenced below.

3 The memory signals consist of:

DATA[31:0]	CS/RAS[4:0]*	OE*
ADDR[27:0]	CAS[3:0]*	WE*
BE[3:0]*	RW*	PORTC3/AMUX

The timing of these signals depends on how the memory is configured. See the timing diagrams in the sections referenced below.

4 The timing of the chip select associated with the buffer descriptor's source address depends on how that chip select is configured.

5 The timing of the chip select associated with the buffer descriptor's destination address depends on how that chip select is configured.

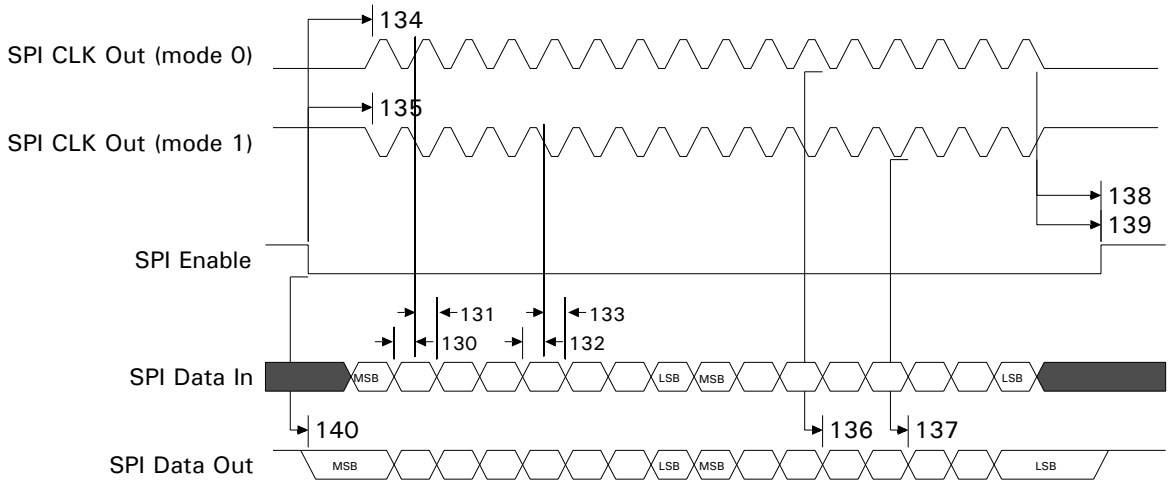
See also

- "SRAM timing" on page 20
- "Fast Page and EDO DRAM timing" on page 30
- "SDRAM timing" on page 37

SPI master and slave timing

SPI Master Mode 0 and 1 (Two-Byte Transfer)

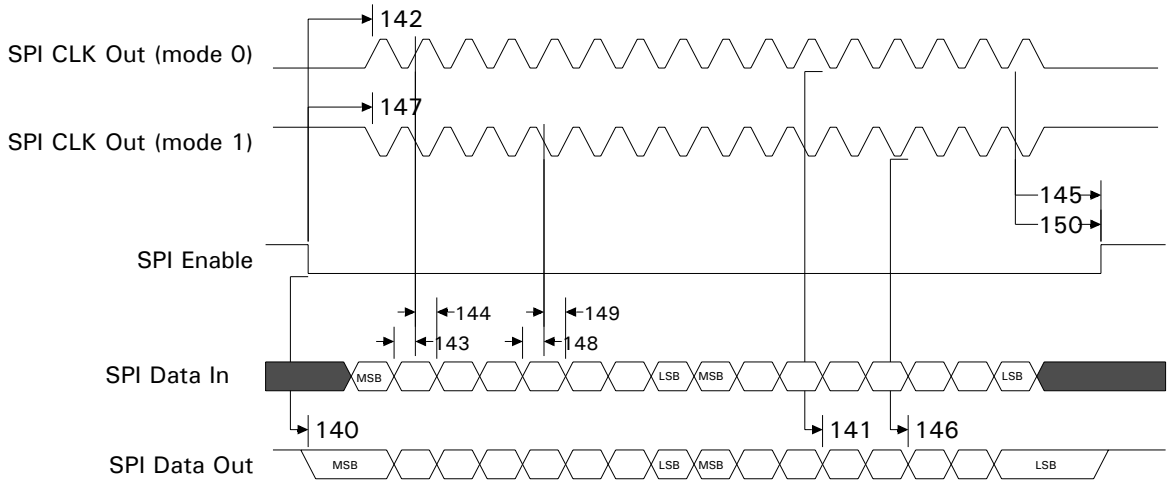
Number	Characteristic	Min.	Max.	Unit
130	Data In valid to mode 0 rising clock (setup)	20		ns
131	Mode 0 rising clock to Data In valid (hold)	0		ns
132	Data In valid to mode 1 falling clock (setup)	20		ns
133	Mode 1 falling clock to Data In valid (hold)	0		ns
134	Enable low to mode 0 first rising clock		1.5	Bit-Time
135	Enable low to mode 1 first falling clock		1.5	Bit-Time
136	Mode 0 falling edge to Data Out valid	-Tsys	Tsys	ns
137	Mode 1 rising edge to Data Out valid	-Tsys	Tsys	ns
138	Mode 0 last falling clock to Enable high		1.5	Bit-Time
139	Mode 1 last rising clock to Enable high		1.5	Bit-Time
140	Enable low to Data Out valid	-Tsys	Tsys	ns



SPI Slave Mode 0 and 1 (Two-Byte Transfer)

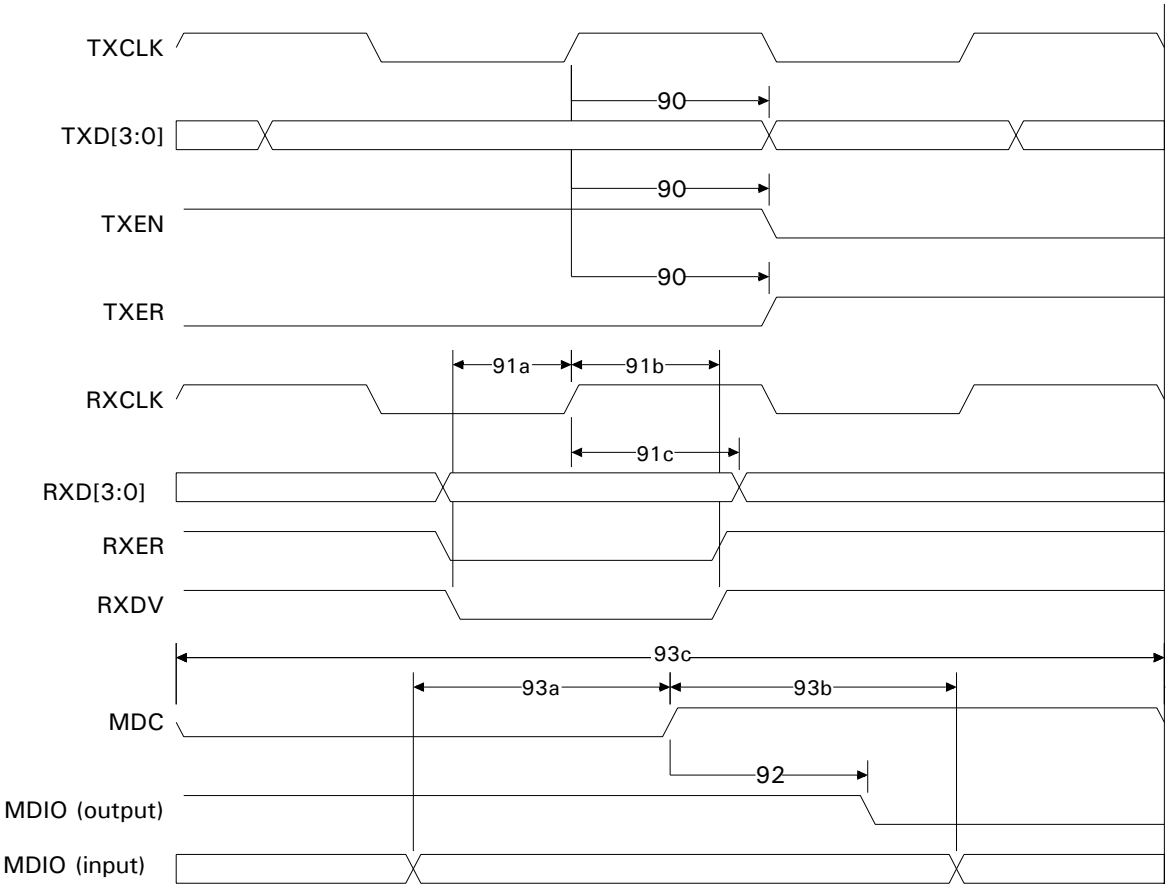
Number	Characteristic	Min.	Max.
141	Mode 0 SPI Clock high to TXD valid	3 * T_{SYS}	4 * T_{SYS}
142	Mode 0 SPI Enable low to SPI Clock high (setup)	0	
143	Mode 0 RXD Input valid to SPI Clock high (setup)	3.4	
144	Mode 0 SPI Clock high to RXD input change (hold)	4 * T_{SYS}	
145	Mode 0 SPI Clock high to SPI Enable high (hold)	4 * T_{SYS}	
146	Mode 1 SPI Clock low to TXD valid	3 * T_{SYS}	4 * T_{SYS}
147	Mode 1 SPI Enable low to SPI Clock low (setup)	0	
148	Mode 1 RXD Input valid to SPI Clock low (setup)	3.4	
149	Mode 1 SPI Clock low to RXD input change (hold)	4 * T_{SYS}	
150	Mode 1 SPI Clock low to SPI Enable high (hold)	4 * T_{SYS}	

Minimum and maximum are in nanoseconds (ns).



Ethernet timing

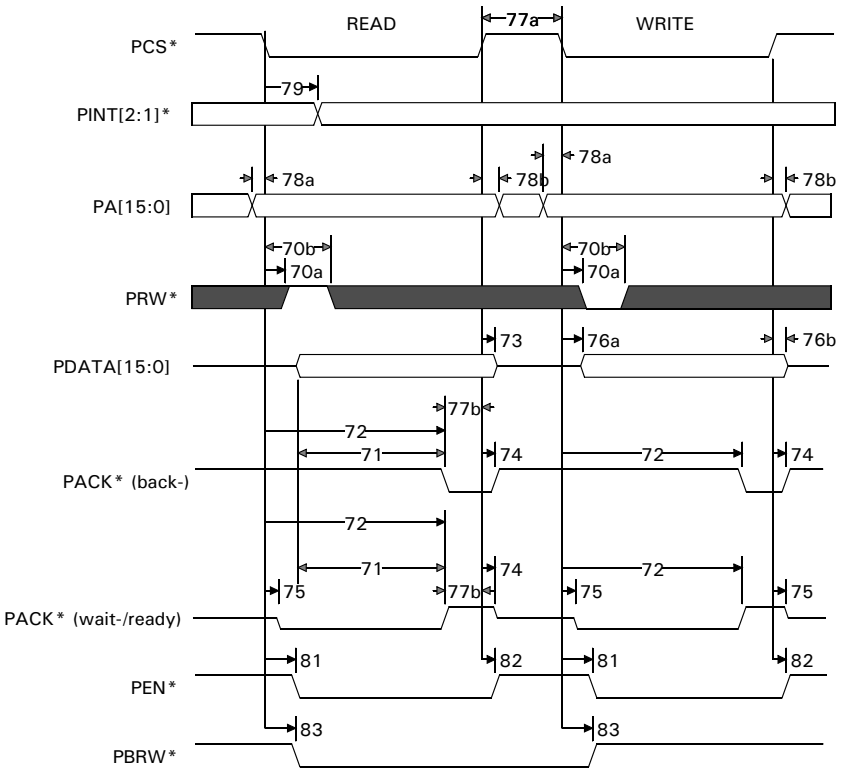
Number	Characteristic	Min.	Max.	Unit
90	TXCLK high to TXD, TXEN, TXER valid	5	17	ns
91a	RXD, RXER, RXDV valid to RXCLK high (setup)	8		ns
91b	RXCLK high to RXD, RXER, RXDV hold time	0		ns
91c	RXCLK high to RXD hold time	0		ns
92	MDC high to MDIO change	40	50	ns
93a	MDIO valid to MDC high (setup)	10		ns
93b	MDC high to MDIO hold time	0		ns
93c	MDC cycle time		SYSCLK/10	
94	RXCLK high to RPSF* change		6.5	ns
95a	REJECT* valid to RXCLK high (setup)	2.6		ns
95b	REJECT* valid from RXCLK high (hold)	0		ns
96	CRS low to RXCLK idle	27		Bit-Time



Notes:

1. Parameters 70a and 70b apply only when the ENI FAST bit is set to 0. When ENI FAST is set to 1, parameters 84a and 84b apply.
2. The PEN* and PBRW* signals control an external bi-directional data bus transceiver for the PDATA bus that can drive only 2 mA.
3. Parameter 72 applies only to ENI registers when FAST is set to 0. This does *not* apply to shared RAM access.
4. Parameter 72a applies to all shared RAM accesses when FAST is set to 0. The max specification for PCS* to PACK* valid is larger for shared RAM accesses. The additional delay depends on the speed of the external RAM assigned to provide the physical shared RAM. Consequently, the maximum specification for shared RAM accesses is system-dependent.
5. Parameter 72b applies to ENI register accesses when FAST is set to 1.
6. Parameter 72c applies to ENI shared RAM accesses when FAST is set to 1.
7. Parameter 85 applies when FAST is set to 0. Parameter 85a applies when FAST is set to 1.
8. Parameter 77c can be reduced to $3*T_{SYS}$ when FAST is set to 1.

ENI Shared RAM and Register Cycle timing



P/N: 91001374_B (formerly 8820002A)

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