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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Network Processor
Core Processor	ARM7®
Program Memory Type	External Program Memory
Controller Series	NET+50
RAM Size	16K x 8
Interface	EBI/EMI, Ethernet, DMA, HDLC, IEEE1284/ENI, SPI, UART
Number of I/O	40
Voltage - Supply	2.25V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	208-LFBGA
Supplier Device Package	208-BGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/digi-international/net-50-bit

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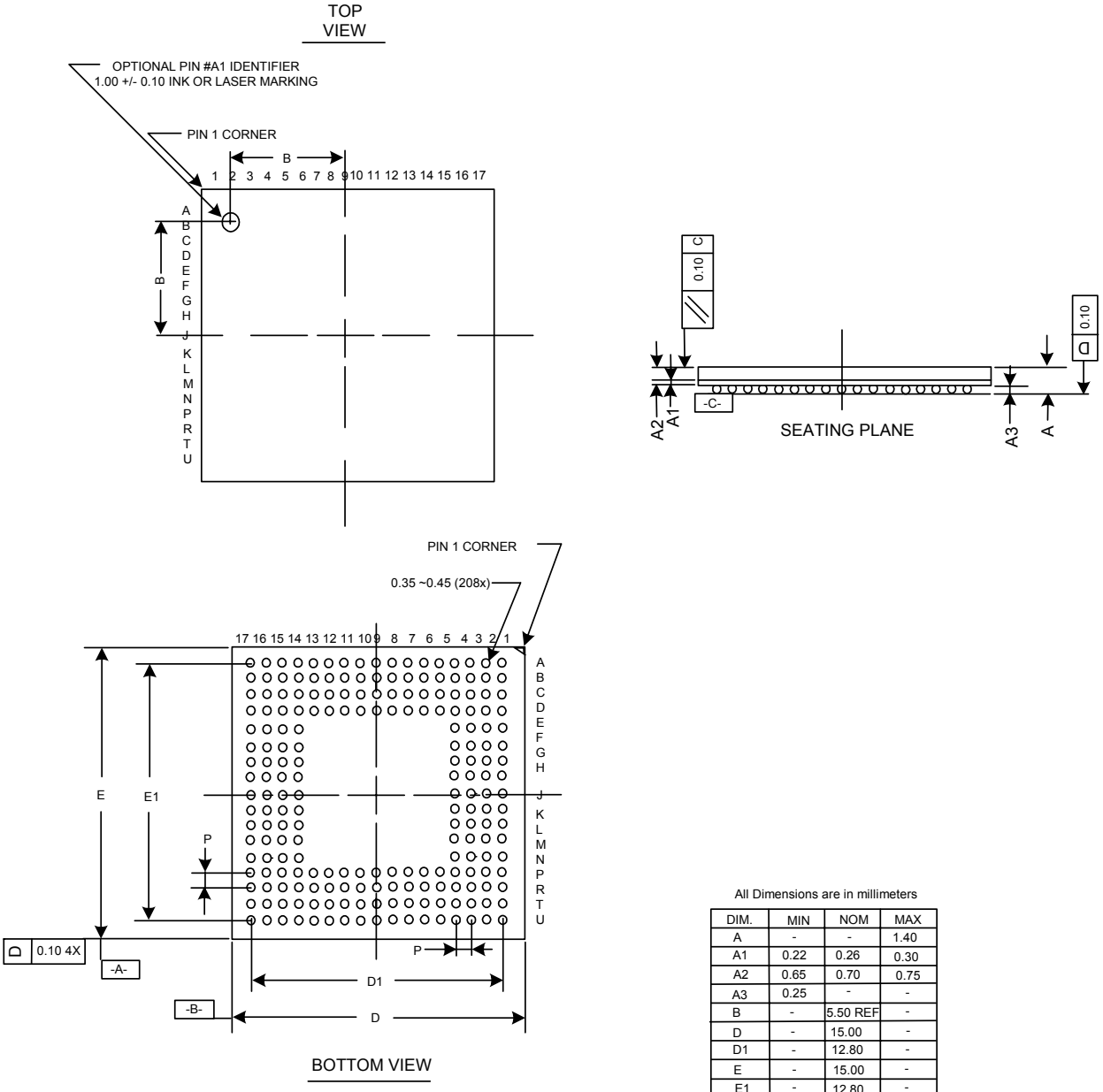
Packaging dimensions and pinout

The NET+50 is available in two package options — a ball-grid array (BGA) or a plastic quad flat pack (PQFP).

BGA packaging and pinout diagram

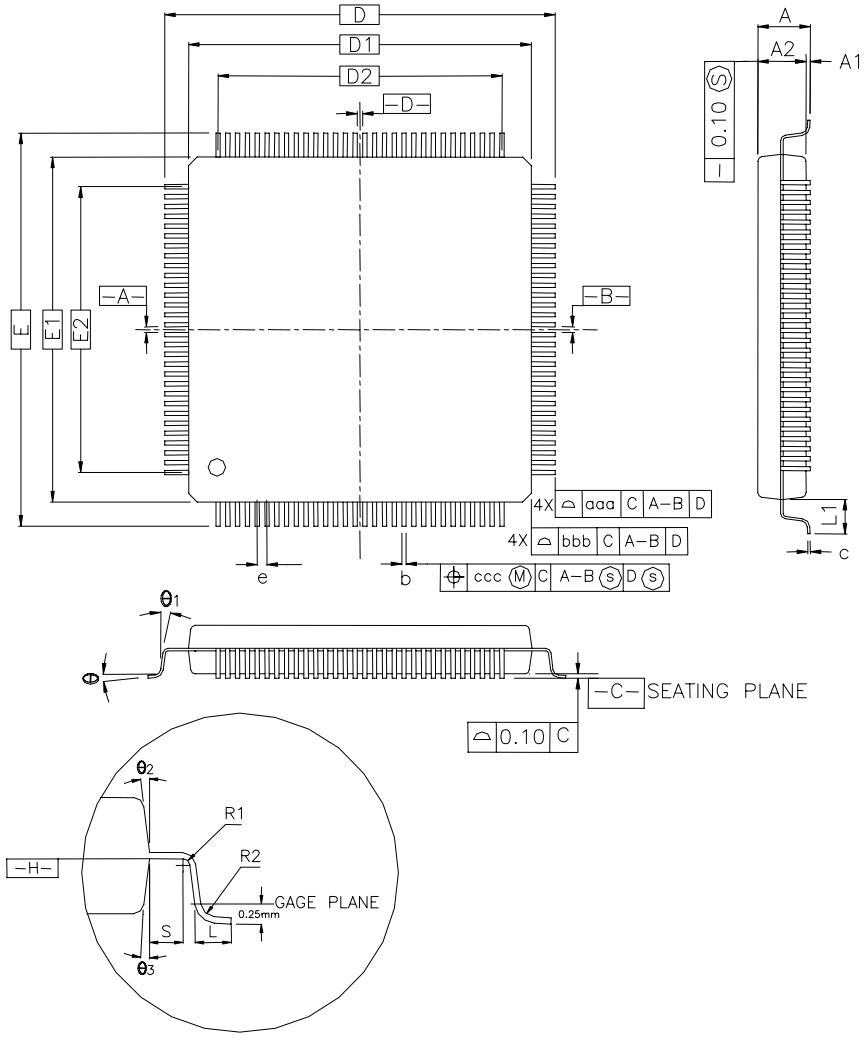


All Dimensions are in millimeters

DIM.	MIN	NOM	MAX
A	-	-	1.40
A1	0.22	0.26	0.30
A2	0.65	0.70	0.75
A3	0.25	-	-
B	-	5.50 REF	-
D	-	15.00	-
D1	-	12.80	-
E	-	15.00	-
E1	-	12.80	-
P	-	0.80	-

PQFP packaging and pinout diagrams

PQFP packaging



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	4.10	—	—	0.161
A_1	0.25	—	—	0.010	—	—
A_2	3.20	3.32	3.60	0.126	0.131	0.142
D	31.20 BASIC			1.228 BASIC		
D_1	28.00 BASIC			1.102 BASIC		
E	31.20 BASIC			1.228 BASIC		
E_1	28.00 BASIC			1.102 BASIC		
R_2	0.13	—	0.30	0.005	—	0.012
R_1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ_1	0°	—	—	0°	—	—
θ_2	8° REF			8° REF		
θ_3	8° REF			8° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L_1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	25.50			1.004		
E2	25.50			1.004		
TOLERANCES OF FORM AND POSITION						
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	0.08			0.003		

System bus interface (cont.)

Signal	BGA	PQFP	I/O	OD	Description
ADDR11	C3 †	99	I/O	4	
ADDR10	A5 †	98	I/O	4	
ADDR9	D4 †	97	I/O	4	
ADDR8	C4 †	96	I/O	4	
ADDR7	B5 †	95	I/O	4	
ADDR6	A6 †	94	I/O	4	
ADDR5	D5 †	93	I/O	4	
ADDR4	C5 †	92	I/O	4	
ADDR3	B6 †	91	I/O	4	
ADDR2	A7 †	90	I/O	4	
ADDR1	D6 †	89	I/O	4	
ADDR0	C6 †	88	I/O	4	
DATA31	T3	162	I/O	4	Data bus
DATA30	R4	161	I/O	4	
DATA29	U3	160	I/O	4	
DATA28	U2	159	I/O	4	
DATA27	R2	155	I/O	4	
DATA26	R1	154	I/O	4	
DATA25	P1	153	I/O	4	
DATA24	P2	152	I/O	4	
DATA23	R3	151	I/O	4	
DATA22	N1	150	I/O	4	
DATA21	P4	149	I/O	4	
DATA20	P3	148	I/O	4	
DATA19	N2	147	I/O	4	
DATA18	M1	146	I/O	4	
DATA17	N4	145	I/O	4	
DATA16	L1	142	I/O	4	
DATA15	M4	141	I/O	4	
DATA14	M3	140	I/O	4	
DATA13	L2	139	I/O	4	
DATA12	K1	138	I/O	4	

ENI/Parallel 1284 Interface

IEEE1284	ENI	GPIO	BGA	PQFP	I/O	OD	Description
PDATA0	PDATA0	GPIOD0	R14 †	200	I/O	2	
PDATA1	PDATA1	GPIOD1	P14 †	201	I/O	2	
PDATA2	PDATA2	GPIOD2	U13 †	202	I/O	2	
PDATA3	PDATA3	GPIOD3	R15 †	203	I/O	2	
PDATA4	PDATA4	GPIOD4	T14 †	204	I/O	2	
PDATA5	PDATA5	GPIOD5	U14 †	205 †	I/O	2	
PDATA6	PDATA6	GPIOD6	U15 †	206	I/O	2	
PDATA7	PDATA7	GPIOD7	T15 †	207	I/O	2	
POE1*	PDATA8		T16 †	2	I/O	2	
POE2*	PDATA9		T17 †	3	I/O	2	
POE3*	PDATA10		R17 †	4	I/O	2	
POE4*	PDATA11		P15 †	5	I/O	2	
PCLKC1	PDATA12		R16 †	6	I/O	2	
PCLKC2	PDATA13		P17 †	7	I/O	2	
PCLKC3	PDATA14		N14 †	8	I/O	2	
PCLKC4	PDATA15		N15 †	9	I/O	2	
PCLKD1	PACK*	GPIOF7	G16	35	I/O	8	
PCLKD2	PEN*	GPIOF6	P16 †	10	I/O	2	
PCLKD3	PINT1*	GPIOF5	N16	11	I/O	2	
PCLKD4	PINT2*	GPIOF4	M15	12	I/O	2	Or ENI DMA output PDRQIO
ACK1*	PA0	GPIH0	M14	13	I		
ACK2*	PA1	GPIH1	N17	14	I		
ACK3*	PA2	GPIH2	M16	15	I		
ACK4*	PA3	GPIH3	L15	16	I		
BUSY1	PA4	GPIH4	L14	17	I		
BUSY2	PA5	GPIOH5	M17	18	I		
BUSY3	PA6	GPIH6	L16	19	I		
BUSY4	PA7	GPIH7	K15	20	I		
PE1	PA8	GPIG0	K14	21	I		
PE2	PA9	GPIG1	L17	22	I		
PE3	PA10	GPIG2	K16	23	I		
PE4	PA11	GPIG3	J15	24	I		

ENI/Parallel 1284 Interface (cont.)

IEEE1284	ENI	GPIO	BGA	PFQP	I/O	OD	Description
PSELECT1	PA12	GPIG4	J14	25	I		
PSELECT2	PA13	GPIOF3	H15	28	I/O	2	Or ENI DMA output PDRQI*
PSELECT3	PA14	GPIOF2	H14	29	I/O	2	Or ENI DMA output PDRQO*
PSELECT4	PA15	GPIG5	J17	30	I		Or ENI DMA input PDACK*
FAULT1*	PA16	GPIG6	H16	31	I		
FAULT2*	PCS*	GPIG7	H17	34	I		
FAULT3*	PRW*	GPIOF0	G14	33	I/O	2	
FAULT4*	PBRW*	GPIOF1	G15	32	I/O	2	

Clock generation

Signal	BGA	PQFP	I/O	OD	Description
XTAL1	U7	178	I		2.5 V crystal oscillator circuit
XTAL2	T8	179	O		
PLLVDD	U8	182			2.5 V PLL clean power
PLLLPF	P9	181			PLL loop filter capacitor
PLLVSS	R9	180			PLL clean ground
PLLTST*	P8 †	177	I		2.5 V PLL test mode
BISTEN*	R10 †	184	I		Enable internal BIST operation
SCANEN*	P10 †	185	I		Enable internal SCAN testing

System reset

Signal	BGA	PQFP	I/O	OD	Description
RESET*	T2 †	158	I		System reset *

Debug support for ARM core

Signal	BGA	PQFP	I/O	OD	Description
TDI	T6 †	171	I		Test data in
TDO	U5	170	O	2	Test data out
TMS	R7 †	172	I		Test mode select
TRST*	R8	174	I		Test mode reset (input current sink)
TCK	P7	173	I		Test mode clock

Power supply

Signal	BGA	PQFP	Description
V_{CC} DC 3.3 V DC	F15, B17, C12, A2, M2, U9	36, 52, 64, 104, 143, 186	I/O steady state (6 pairs)
V_{SS} DC Gnd Returns	F14, A17, D12, A1, N3, U10	37, 53, 65, 105, 144, 188	
V_{CC} AC 3.3 V	A8, E1, T1, U16	86, 118, 156, 208	I/O switching (4 pairs — see note below on 3.3 V power and GND pads)
V_{SS} AC Gnd Return	B7, F2, U1, U17	87, 119, 157, 1	
V_{DD} CO 2.5 V	K17, A10, H1, T7	26, 78, 130, 175	Core power (4 pairs)
V_{SS} CO Gnd Returns	J16, B9, J2, U6	27, 79, 131, 176	
PLL V_{DD} 2.5 V	U8	182	PLL bead filtered clean power
PLL V_{SS} Gnd Return	R9	180	Power-up reset ground reference
POR V_{SS} Gnd	T9	183	

Additional information about NET+50 pins

- All outputs drive TTL levels. Outputs drive to 0.4 V maximum on low, 2.4 V minimum on high.
- The following pins require a 2.5 V input level:

Signal	BGA	PQFP
XTAL1	U7	178
PLLTST	P8	177
PLLVDD	U8	182

- TRST* (R8, 174) is the only pin that is an input current sink.
- Remaining inputs are TTL levels and are 3.3 V tolerant, allowing integration with 3.3 V devices.
- Regarding 3.3 V power and GND pads: In general, you should use separate power pairs for AC and DC power to prevent the noise in the AC power buses from reaching the DC power buses. Digi recommends (and uses) a ferrite bead to filter the AC power pins.

ARM debugging features

The ARM7TDMI core contains hardware extensions for advanced debugging. These extensions facilitate development and testing of application software, operating systems, and the hardware itself.

The debug extensions let you stop the core on a given instruction fetch (break-point) or data access (watchpoint), or asynchronously by a debug request. In such cases, the ARM processor is in *debug state* so you can examine the core's internal state and the system's external state. When the examination is complete, you can restore the core and system state, and resume program execution.

The ARM processor is put into debug state by an internal functional unit called *ICEBreaker*. In debug state, the core isolates itself from the memory system. You can examine the core while all other system activities — for example, DMA operations — continue normally.

You can examine the ARM processor's internal state through the 5-pin interface for debugging. This interface lets you serially insert instructions into the core's pipe-line without using the external data bus. Therefore, in debug state, you can insert a store-multiple into the instruction pipeline to dump the contents of the processor's registers. Data can be serially shifted out without affecting the rest of the system.

DC characteristics and other specifications

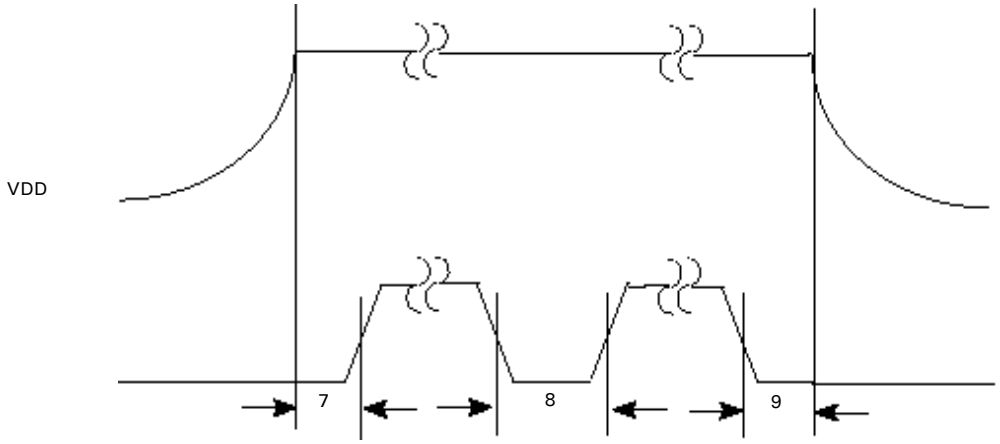
DC inputs

Symbol	Characteristic	Conditions	Min.	Typical	Max.	Unit
V_{DD}	DC supply voltage — core		2.25	2.5	2.75	V
V_{CC}	DC supply voltage — I/O		3.0	3.3	3.6	V
V_{IH}	Input high voltage		2.0		3.6	V
V_{IL}	Input low voltage		V_{SS} – 0.3		0.8	V
I_{IL}	Input buffer	$V_{IN} = V_{CC}$	-10		10	µA
	Input buffer with current sink		99		429	
I_{IH}	Input buffer	$V_{IN} = V_{SS}$	-10		10	µA
	Input buffer with current source		130		352	
C_{IN}	Input capacitance	Any input		7		pF
V_T	Switching threshold	Any input	1.4	2.0		V

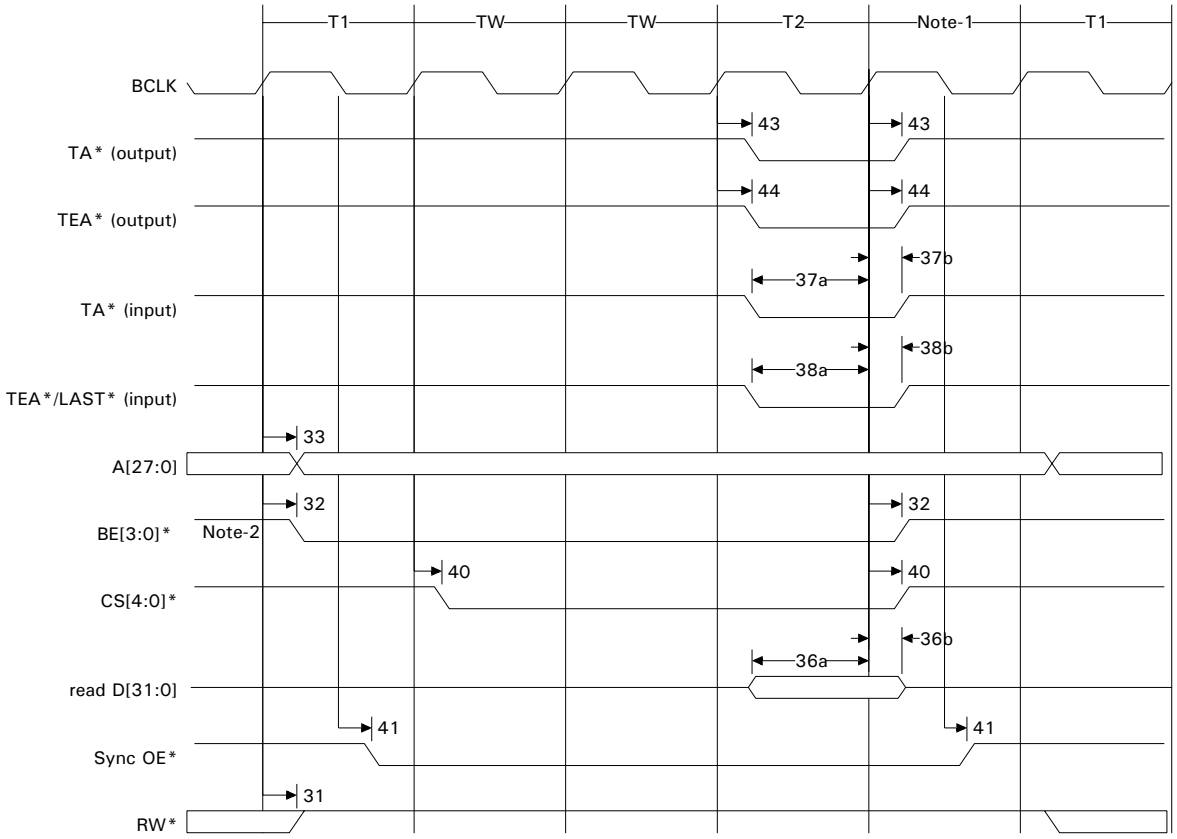
Timing data and diagrams

Reset timing

Number	Characteristic	Min.	Max.	Unit
7	V_{DD} at 3.0 V to RESET* high	40		ms
8	RESET* pulse width low	$10/F_{SYSCLK}$		µs
9	RESET* low to V_{DD} below 3.0 V	$8/F_{SYSCLK}$		µs



SRAM Sync Read (Wait = 2)



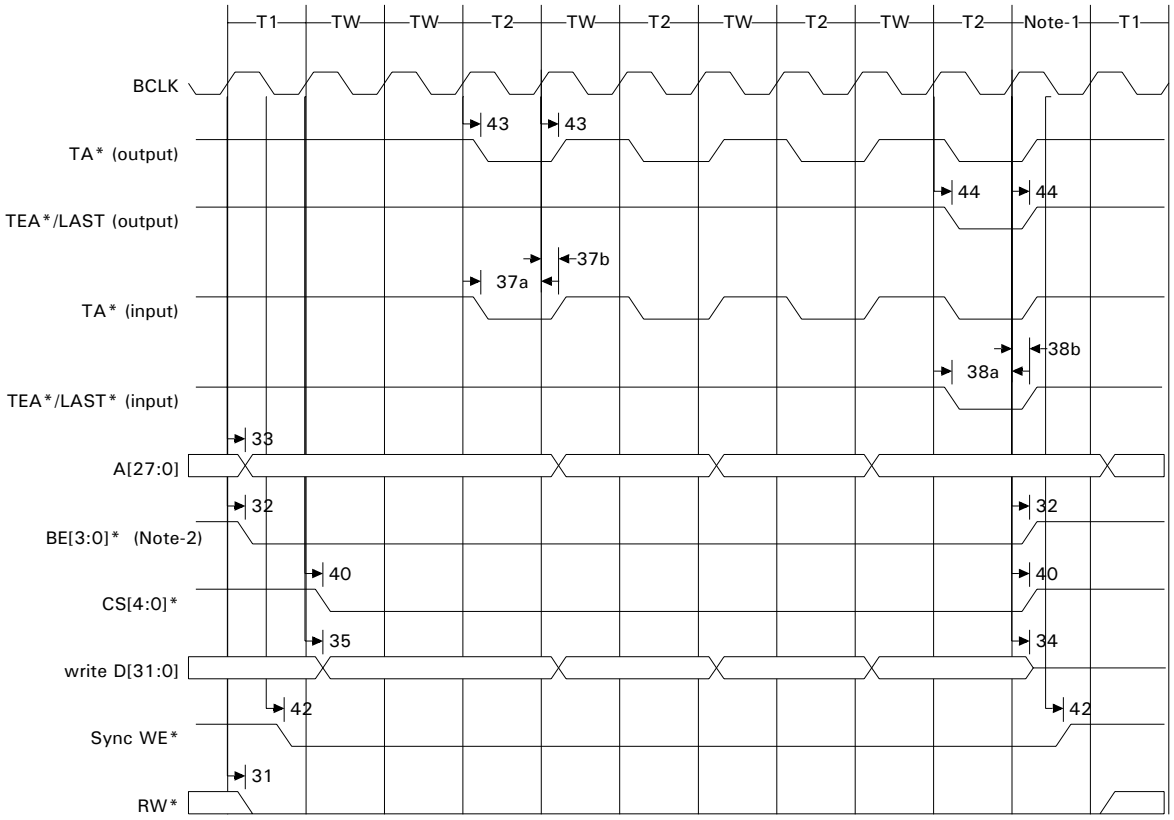
Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

SRAM Sync Burst Write (4-222, Wait = 2, BCYC = 01)



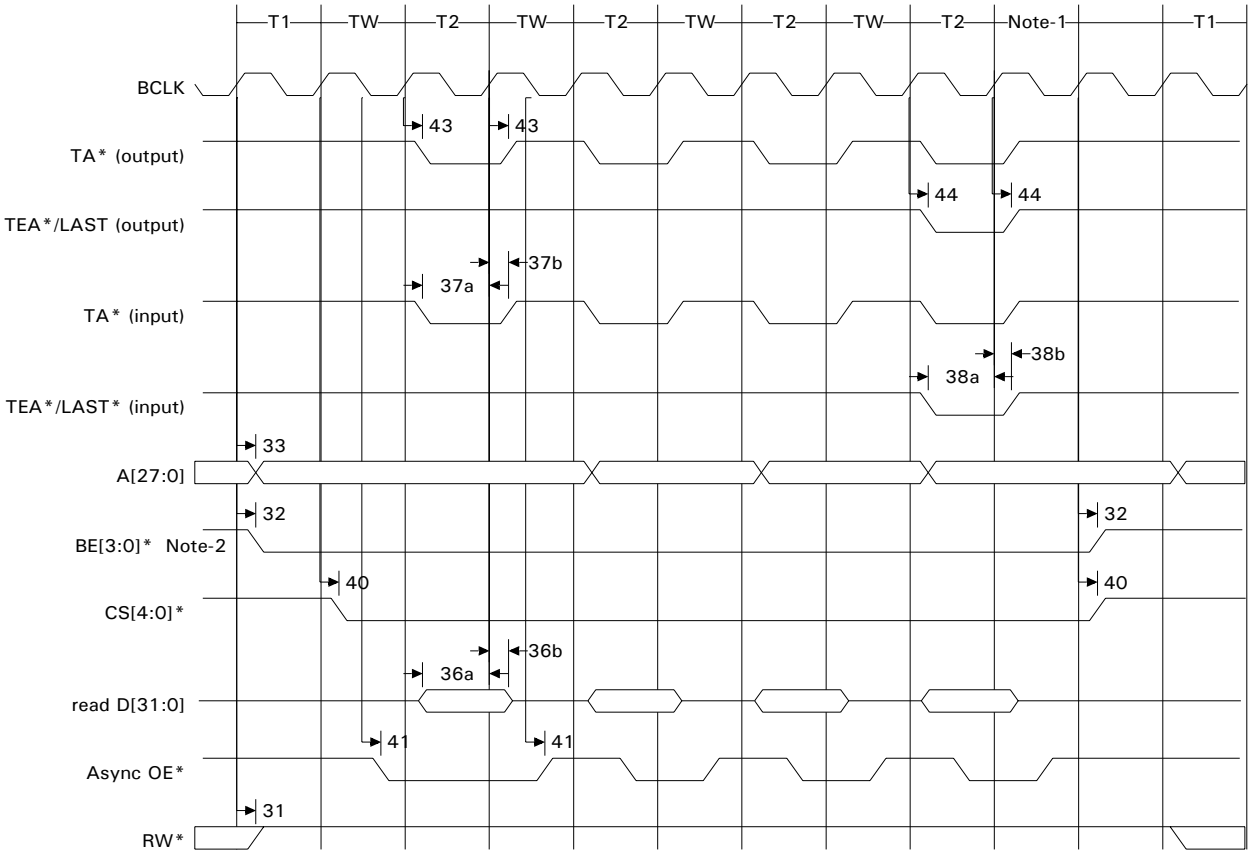
Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

SRAM Async Burst Read (Wait = 2, BCYC = 01)



Notes:

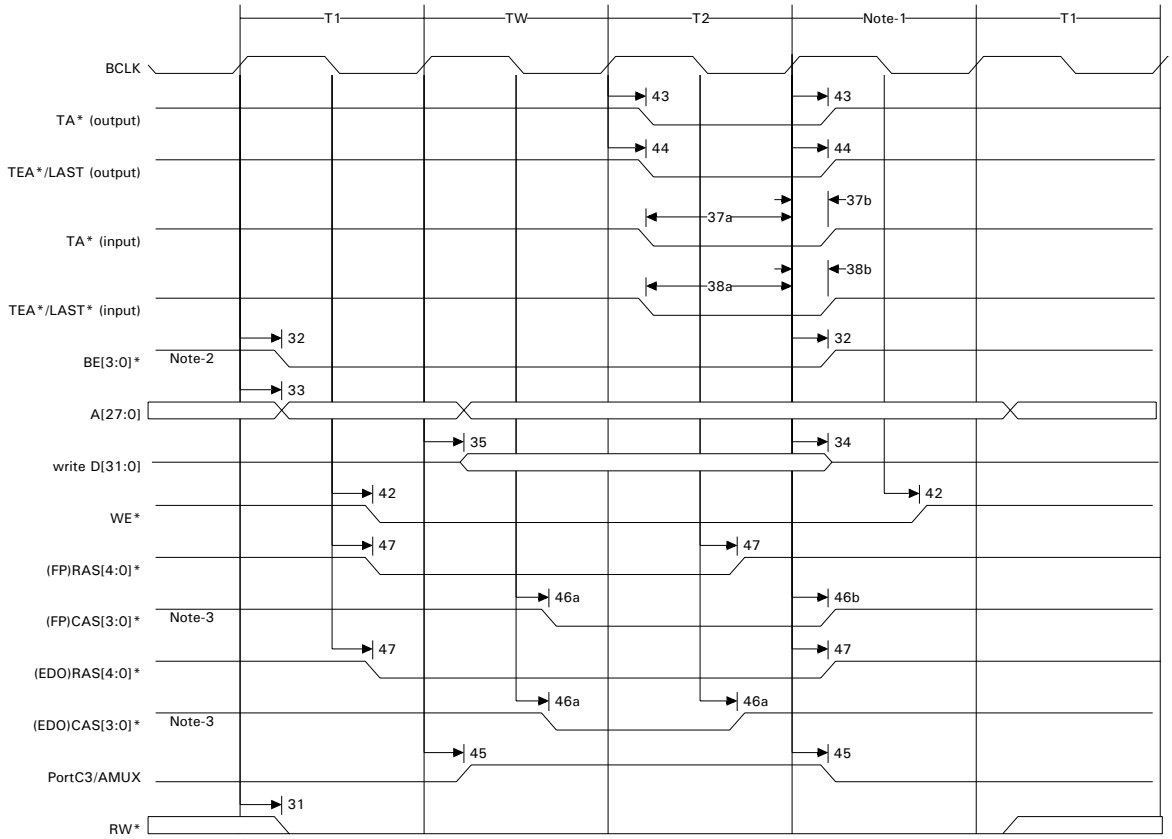
1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 The TW cycles are present when the WAIT field is set to 2 or more.

Fast Page and EDO DRAM Write



Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

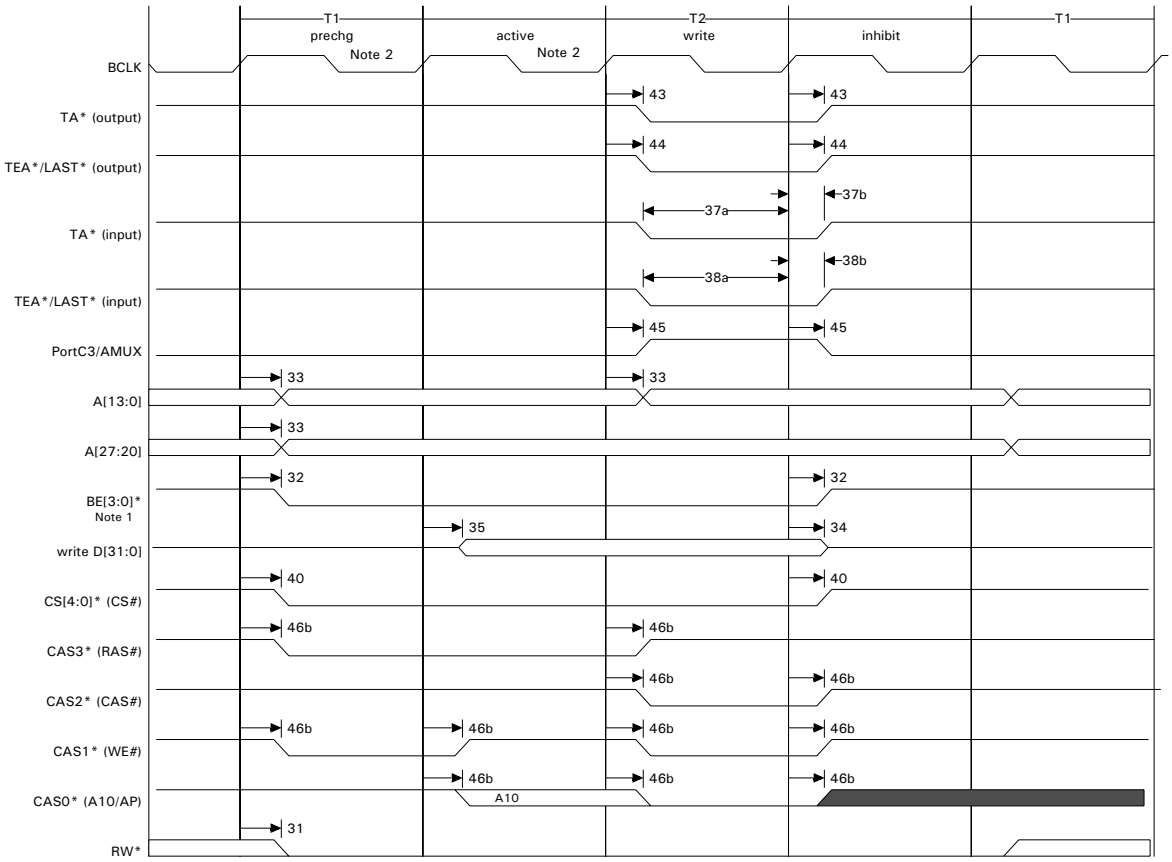
2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 Port size determines which CAS* signals are active:

8-bit port = CAS3*
16-bit port = CAS[3:2]*
32-bit port = CAS[3:0]*

SDRAM Write



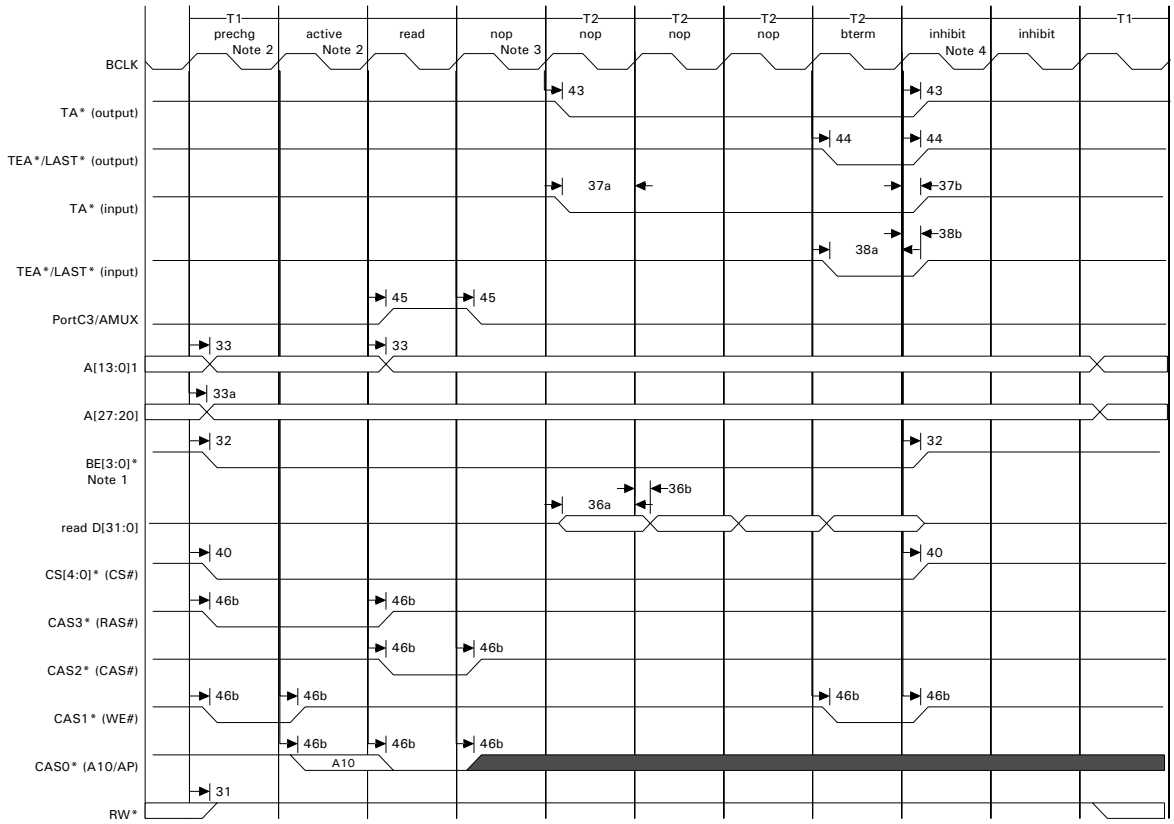
Notes:

1 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

2 The Precharge command or Active command or both are not always present. They depend on the address of the previous SDRAM access.When the Active command is not present, parameter 35 (write D[31:0]) is not valid until the Write (T2) cycle.

SDRAM Burst Read (CAS Latency = 2)



Notes:

1 Port size determines which byte enable signals are active:

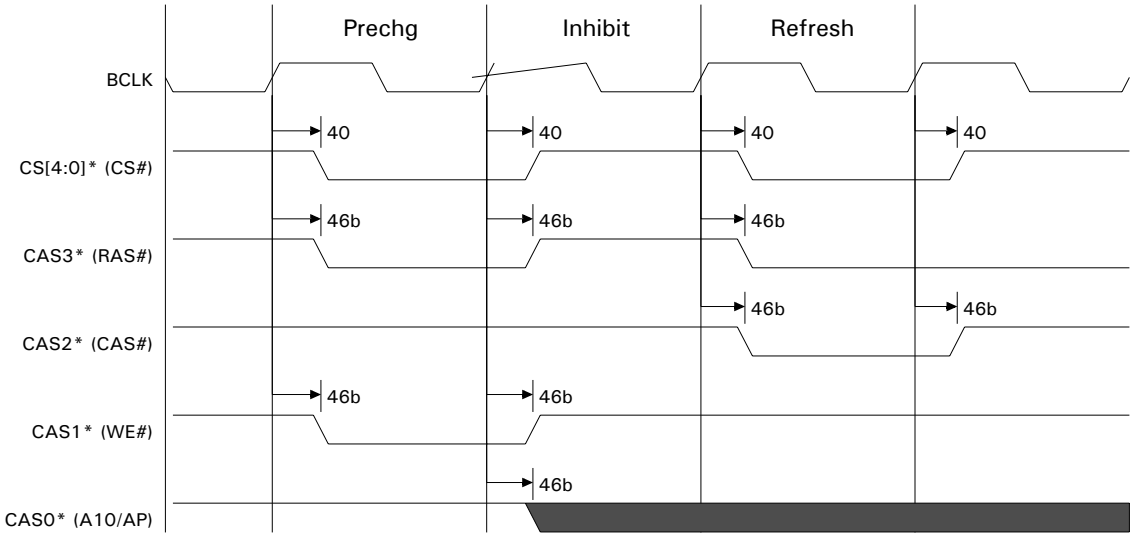
8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

2 The Precharge command or Active command or both are not always present. They depend on the address of the previous SDRAM access.

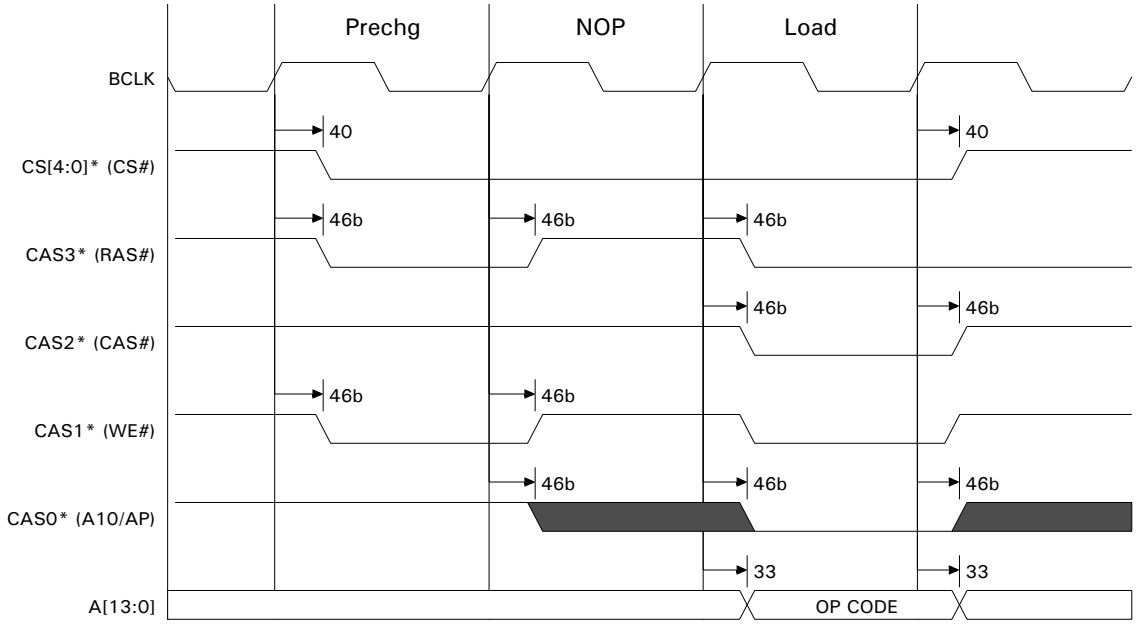
3 If CAS latency = 3, there are:

- 5 NOPs between the Read and Burst Terminate commands
- 3 Inhibit commands after the Burst Terminate command

SDRAM Refresh Command

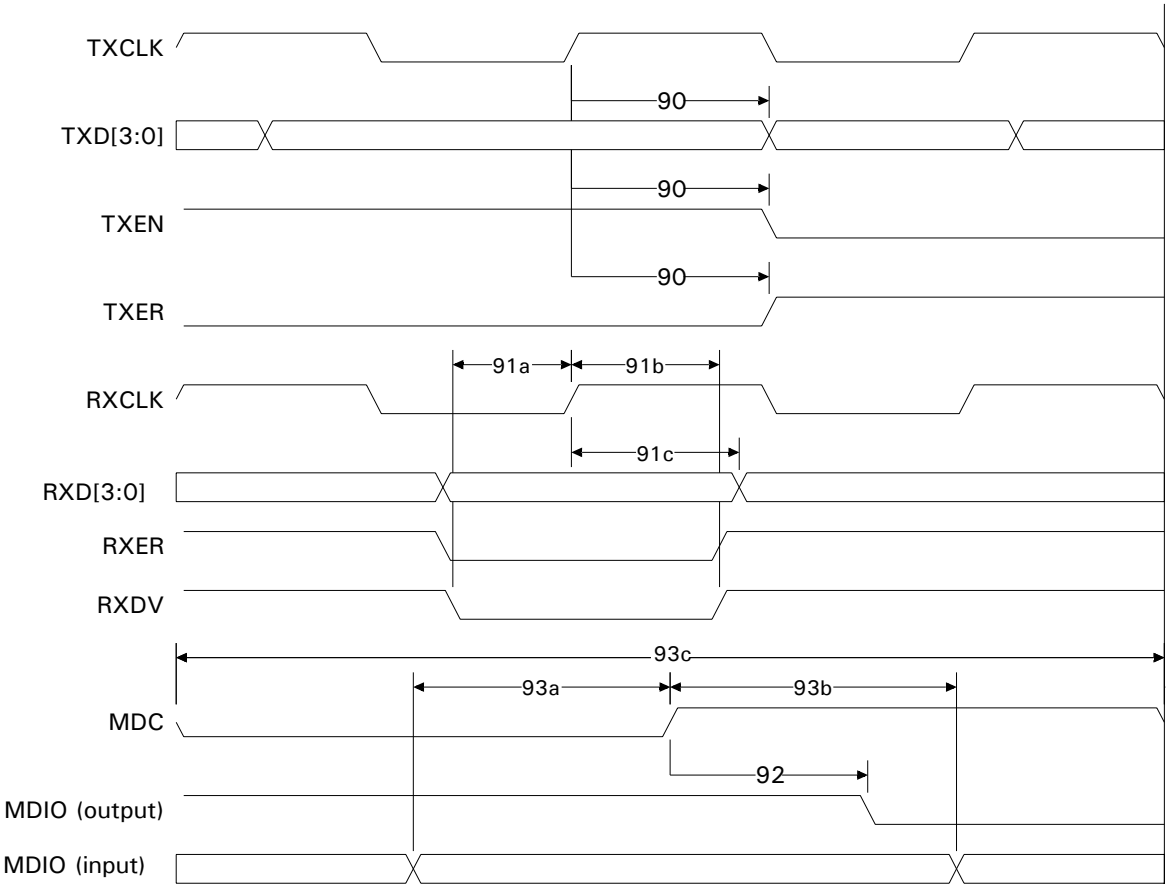


SDRAM Load Mode Command



Ethernet timing

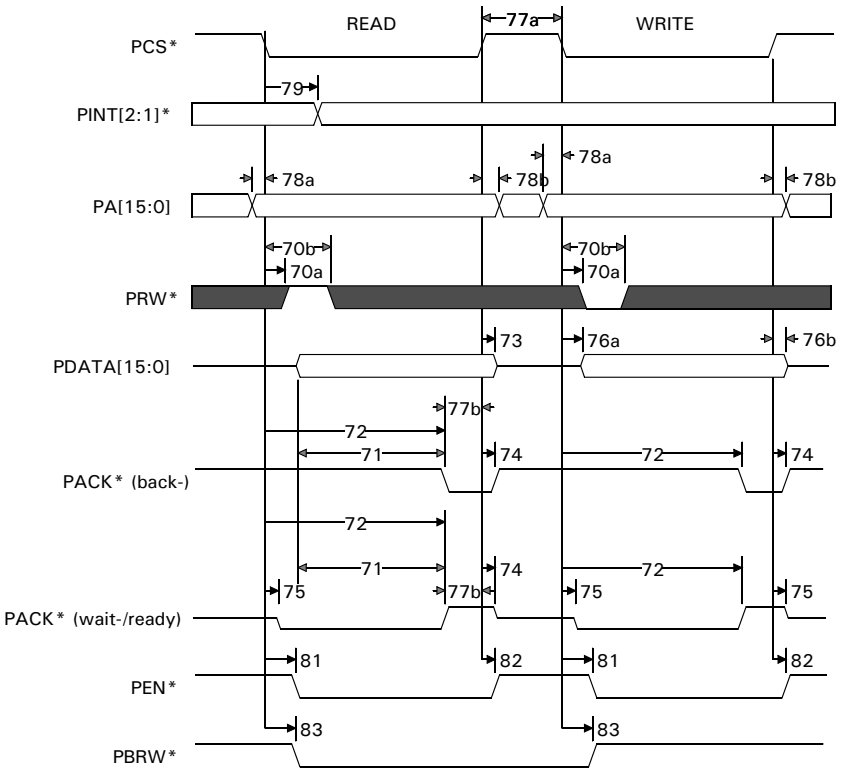
Number	Characteristic	Min.	Max.	Unit
90	TXCLK high to TXD, TXEN, TXER valid	5	17	ns
91a	RXD, RXER, RXDV valid to RXCLK high (setup)	8		ns
91b	RXCLK high to RXD, RXER, RXDV hold time	0		ns
91c	RXCLK high to RXD hold time	0		ns
92	MDC high to MDIO change	40	50	ns
93a	MDIO valid to MDC high (setup)	10		ns
93b	MDC high to MDIO hold time	0		ns
93c	MDC cycle time		SYSCLK/10	
94	RXCLK high to RPSF* change		6.5	ns
95a	REJECT* valid to RXCLK high (setup)	2.6		ns
95b	REJECT* valid from RXCLK high (hold)	0		ns
96	CRS low to RXCLK idle	27		Bit-Time



Notes:

1. Parameters 70a and 70b apply only when the ENI FAST bit is set to 0. When ENI FAST is set to 1, parameters 84a and 84b apply.
2. The PEN* and PBRW* signals control an external bi-directional data bus transceiver for the PDATA bus that can drive only 2 mA.
3. Parameter 72 applies only to ENI registers when FAST is set to 0. This does *not* apply to shared RAM access.
4. Parameter 72a applies to all shared RAM accesses when FAST is set to 0. The max specification for PCS* to PACK* valid is larger for shared RAM accesses. The additional delay depends on the speed of the external RAM assigned to provide the physical shared RAM. Consequently, the maximum specification for shared RAM accesses is system-dependent.
5. Parameter 72b applies to ENI register accesses when FAST is set to 1.
6. Parameter 72c applies to ENI shared RAM accesses when FAST is set to 1.
7. Parameter 85 applies when FAST is set to 0. Parameter 85a applies when FAST is set to 1.
8. Parameter 77c can be reduced to $3*T_{SYS}$ when FAST is set to 1.

ENI Shared RAM and Register Cycle timing



ENI Dual Direction DMA timing