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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Network Processor
Core Processor	ARM7®
Program Memory Type	External Program Memory
Controller Series	NET+50
RAM Size	16K x 8
Interface	EBI/EMI, Ethernet, DMA, HDLC, IEEE1284/ENI, SPI, UART
Number of I/O	40
Voltage - Supply	2.25V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/digi-international/net-50-qin-3

Operating frequency

- 44-MHz maximum system clock, requiring only a simple external 18.432-MHz crystal
- Supports external oscillators

ENI/P1284 Interface

- ENI host interface
- Four IEEE 1284 parallel ports
- 64 KB shared RAM ENI interface — 8- or 16-bit
- Full-duplex FIFO mode interface — 8- or 16-bit
- 32-byte transmit/receive FIFO mode FIFOs

Programmable timers

- Two independent, 27-bit timers (2 μs–20.7 hours)
- Watchdog timer (interrupt or reset on expiration)
- Bus timer

Serial port

- Two fully independent serial ports (UART, HDLC, SPI)
- Digital phase locked loop (DPLL) for receive clock extractions
- 32 byte transmit/receive FIFOs
- Internal programmable bit-rate generators
- Bit rates 75–230400 in 16X mode, 1200 bps – 4 Mbps in 1X mode. (Higher rates may be possible depending on the board design.)

10-channel DMA controller

- Two channels dedicated to Ethernet transmit and receive
- Four channels dedicated to serial transmit and receive
- Four channels (two at a time) configurable for external peripherals
- Flexible buffer management

Bus interface

- Five independent, programmable chip selects with 256 Mb addressing per chip select
- All chip selects support SRAM, EDO DRAM, SDRAM, and devices such as flash and EEPROM with SRAM interfaces
- Supports 8-, 16-, and 32-bit peripherals
- Dynamic bus sizing support
- Supports ASYNC and SYNC peripheral timing
- Internal DRAM address multiplexing
- Internal refresh controller (CAS before RAS)
- Burst-mode support
- 0–15 wait states per chip select
- Bootstrap support

Power and operating voltages

- 552 mW maximum (typically, 484 mW), outputs switching
- 3.3 V — I/O
- 2.5 V — core

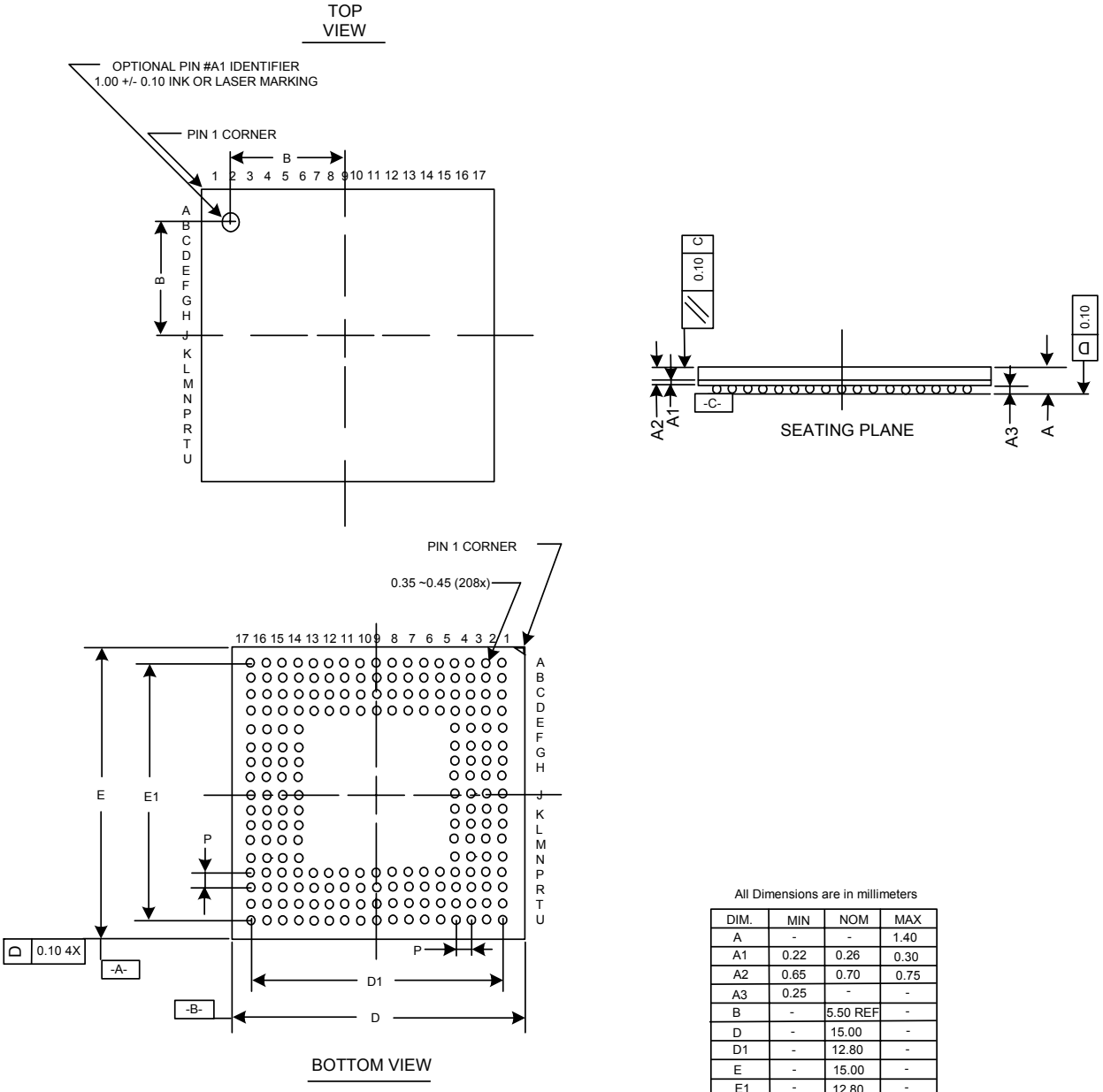
Serial port (cont)

- Odd, even, or no parity
- 5, 6, 7, or 8 bits
- 1 or 2 stop bits
- Internal and external clock support
- Receive-side character and buffer gap timers
- Four receive-side data match detectors

Packaging dimensions and pinout

The NET+50 is available in two package options — a ball-grid array (BGA) or a plastic quad flat pack (PQFP).

BGA packaging and pinout diagram

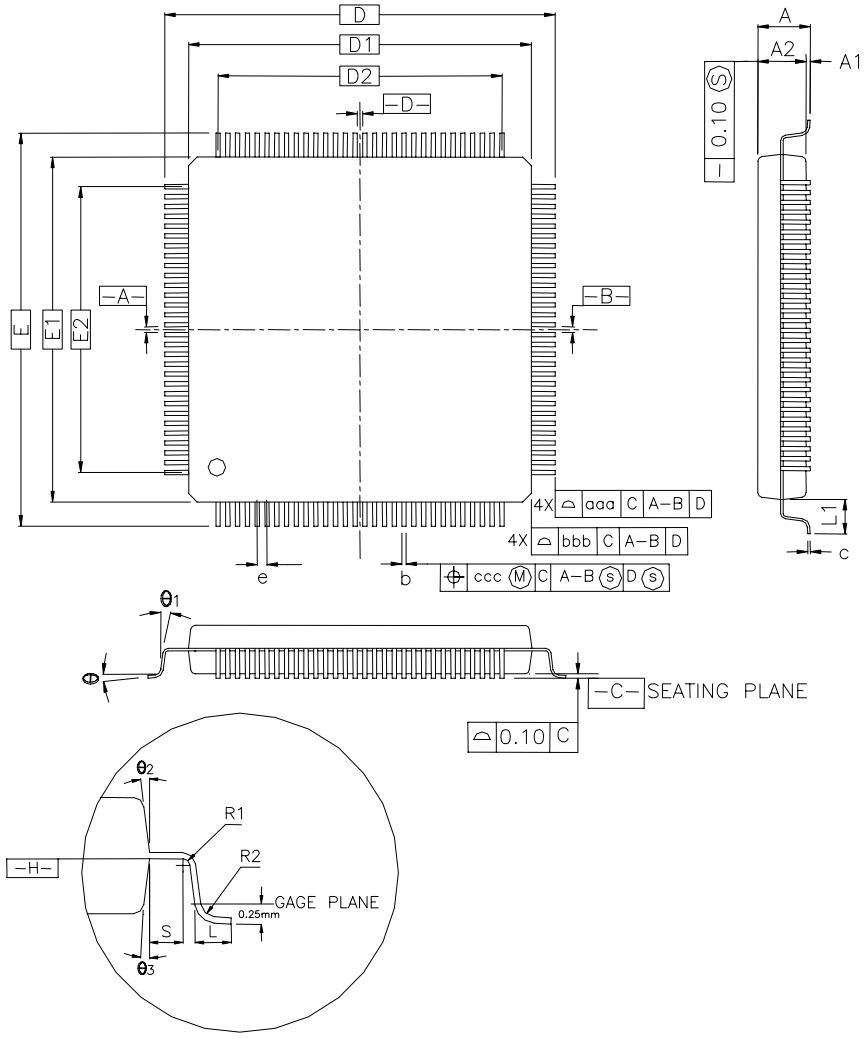


All Dimensions are in millimeters

DIM.	MIN	NOM	MAX
A	-	-	1.40
A1	0.22	0.26	0.30
A2	0.65	0.70	0.75
A3	0.25	-	-
B	-	5.50 REF	-
D	-	15.00	-
D1	-	12.80	-
E	-	15.00	-
E1	-	12.80	-
P	-	0.80	-

PQFP packaging and pinout diagrams

PQFP packaging



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	4.10	—	—	0.161
A_1	0.25	—	—	0.010	—	—
A_2	3.20	3.32	3.60	0.126	0.131	0.142
D	31.20 BASIC			1.228 BASIC		
D_1	28.00 BASIC			1.102 BASIC		
E	31.20 BASIC			1.228 BASIC		
E_1	28.00 BASIC			1.102 BASIC		
R_2	0.13	—	0.30	0.005	—	0.012
R_1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ_1	0°	—	—	0°	—	—
θ_2	8° REF			8° REF		
θ_3	8° REF			8° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L_1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	25.50			1.004		
E2	25.50			1.004		
TOLERANCES OF FORM AND POSITION						
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	0.08			0.003		

System bus interface (cont.)

Signal	BGA	PQFP	I/O	OD	Description
DATA11	L4	137	I/O	4	
DATA10	L3	136	I/O	4	
DATA9	K2	135	I/O	4	
DATA8	J1	134	I/O	4	
DATA7	K4	133	I/O	4	
DATA6	K3	132	I/O	4	
DATA5	J4	129	I/O	4	
DATA4	J3	128	I/O	4	
DATA3	H2	127	I/O	4	
DATA2	G1	126	I/O	4	
DATA1	H4	125	I/O	4	
DATA0	H3	124	I/O	4	
TS*	no connect				
BE3*	G2	123	I/O	2	Byte enable D31:D24
BE2*	F1	122	I/O	2	Byte enable D23:D16
BE1*	G4	121	I/O	2	Byte enable D15:D08
BE0*	G3	120	I/O	2	Byte enable D07:D00
RW*	U4	163	I/O	2	Transfer direction
TA*	R5 †	165	I/O	8	Data transfer acknowledge
TEA*	T4 †	166	I/O	8	Transfer error/last acknowledge
BR*	no connect				
BG*	no connect				
BUSY*	no connect				

ENI/Parallel 1284 Interface (cont.)

IEEE1284	ENI	GPIO	BGA	PFQP	I/O	OD	Description
PSELECT1	PA12	GPIG4	J14	25	I		
PSELECT2	PA13	GPIOF3	H15	28	I/O	2	Or ENI DMA output PDRQI*
PSELECT3	PA14	GPIOF2	H14	29	I/O	2	Or ENI DMA output PDRQO*
PSELECT4	PA15	GPIG5	J17	30	I		Or ENI DMA input PDACK*
FAULT1*	PA16	GPIG6	H16	31	I		
FAULT2*	PCS*	GPIG7	H17	34	I		
FAULT3*	PRW*	GPIOF0	G14	33	I/O	2	
FAULT4*	PBRW*	GPIOF1	G15	32	I/O	2	

Clock generation

Signal	BGA	PQFP	I/O	OD	Description
XTAL1	U7	178	I		2.5 V crystal oscillator circuit
XTAL2	T8	179	O		
PLLVDD	U8	182			2.5 V PLL clean power
PLLLPF	P9	181			PLL loop filter capacitor
PLLVSS	R9	180			PLL clean ground
PLLTST*	P8 †	177	I		2.5 V PLL test mode
BISTEN*	R10 †	184	I		Enable internal BIST operation
SCANEN*	P10 †	185	I		Enable internal SCAN testing

System reset

Signal	BGA	PQFP	I/O	OD	Description
RESET*	T2 †	158	I		System reset *

Debug support for ARM core

Signal	BGA	PQFP	I/O	OD	Description
TDI	T6 †	171	I		Test data in
TDO	U5	170	O	2	Test data out
TMS	R7 †	172	I		Test mode select
TRST*	R8	174	I		Test mode reset (input current sink)
TCK	P7	173	I		Test mode clock

Registers and addresses

General control module

Address	Register	Address	Register
0xFFB0 0000	System control register	0xFFB0 0024	Port B register
0xFFB0 0004	System status register	0xFFB0 0028	Port C register
0xFFB0 0008	PLL control register	0xFFB0 0030	Interrupt enable register
0xFFB0 000C	Software service register	0xFFB0 0034	Interrupt enable register — Set
0xFFB0 0010	Timer 1 control register	0xFFB0 0038	Interrupt enable register — Clear
0xFFB0 0014	Timer 1 status register	0xFFB0 0034	Interrupt status register — Enabled
0xFFB0 0018	Timer 2 control register	0xFFB0 0038	Interrupt status register — Raw
0xFFB0 001C	Timer 2 status register	0xFFB0 0040	Cache control register 0
0xFFB0 0020	Port A register	0xFFB0 0044	Cache control register 1

Memory module controller

Address	Register	Address	Register
0xFFC0 0000	Memory module configuration register (MMCR)	0xFFC0 0034	Chip select 2 option register (OR2)
0xFFC0 0010	Chip select 0 base address register (BAR0)	0xFFC0 0038	Chip select 2 option register B (OR2B)
0xFFC0 0014	Chip select 0 option register (OR0)	0xFFC0 0040	Chip select 3 base address register (BAR3)
0xFFC0 0018	Chip select 0 option register B (OR0B)	0xFFC0 0044	Chip select 3 option register (OR3)
0xFFC0 0020	Chip select 1 base address register (BAR1)	0xFFC0 0048	Chip select 3 option register B (OR3B)
0xFFC0 0024	Chip select 1 option register (OR1)	0xFFC0 0050	Chip select 4 base address register (BAR4)
0xFFC0 0028	Chip select 1 option register B (OR1B)	0xFFC0 0054	Chip select 4 option register (OR4)
0xFFC0 0030	Chip select 2 base address register (BAR2)	0xFFC0 0058	Chip select 4 option register B (OR4B)

ENI controller module

Address	Register	Address	Register
0xFFA0 0000	General control register	0xFFA0 0030	ENI control register
0xFFA0 0004	General status register	0xFFA0 0034	ENI pulsed interrupt register
0xFFA0 0008	FIFO mode data register	0xFFA0 0038	ENI shared RAM address register
0xFFA0 0010 – 001C	IEEE1284 ports 1–4 control registers	0xFFA0 003C	ENI shared register
0xFFA0 0020 – 002C	IEEE 1284 ports 1–4 data registers	0xFFA0 0040 – 0050	GPIO ports D, F, G, H, and F registers

Test modes and PLL usage

The PLLTST*, BISTEN*, and SCANEN* primary inputs control test modes for test operations (in manufacturing) and for using an external oscillator instead of a crystal, as follows:

PLLTST*	BISTEN*	SCANEN*	Mode
1	1	1	Normal with PLL operational
0	1	1	Normal with PLL bypass
1	1	0	HiZ / Tri-state (manufacturing testing)

Note: All other combinations of these inputs are reserved.

PLL

When the PLLTST* signal is active low, the PLL is isolated, and the internal system clock is provided by the XTAL1 input (XTAL1 = SYSCLK). The PLL is not programmable. If you want to use the PLL (crystal) and get a system clock of 44.236 MHz, you must use an 18.432 MHz crystal.

HiZ/Tri-state

The NET+50 chip supports a way to tri-state all outputs. When both PLLTST* and BISTEN* are inactive (high) and SCANNEN* is active (low), all outputs are placed in a low current tri-state mode.

ARM debugging features

The ARM7TDMI core contains hardware extensions for advanced debugging. These extensions facilitate development and testing of application software, operating systems, and the hardware itself.

The debug extensions let you stop the core on a given instruction fetch (break-point) or data access (watchpoint), or asynchronously by a debug request. In such cases, the ARM processor is in *debug state* so you can examine the core's internal state and the system's external state. When the examination is complete, you can restore the core and system state, and resume program execution.

The ARM processor is put into debug state by an internal functional unit called *ICEBreaker*. In debug state, the core isolates itself from the memory system. You can examine the core while all other system activities — for example, DMA operations — continue normally.

You can examine the ARM processor's internal state through the 5-pin interface for debugging. This interface lets you serially insert instructions into the core's pipe-line without using the external data bus. Therefore, in debug state, you can insert a store-multiple into the instruction pipeline to dump the contents of the processor's registers. Data can be serially shifted out without affecting the rest of the system.

DC characteristics and other specifications

DC inputs

Symbol	Characteristic	Conditions	Min.	Typical	Max.	Unit
V_{DD}	DC supply voltage — core		2.25	2.5	2.75	V
V_{CC}	DC supply voltage — I/O		3.0	3.3	3.6	V
V_{IH}	Input high voltage		2.0		3.6	V
V_{IL}	Input low voltage		V_{SS} – 0.3		0.8	V
I_{IL}	Input buffer	$V_{IN} = V_{CC}$	-10		10	µA
	Input buffer with current sink		99		429	
I_{IH}	Input buffer	$V_{IN} = V_{SS}$	-10		10	µA
	Input buffer with current source		130		352	
C_{IN}	Input capacitance	Any input		7		pF
V_T	Switching threshold	Any input	1.4	2.0		V

DC outputs

Symbol	Characteristic	Conditions	Min.	Max.	Unit
V_{OL}	Output low voltage		0	0.4	V
V_{OH}	Output high voltage		2.4	V_{CC}	V
I_{OZ}	High-Z leakage current	$V_O = V_{SS}$	-10	10	µA
I_{OS}	Output short circuit current	V_{CC} = 3.6V, V_O (low) = V_{CC}		55	µA
		V_{CC} = 3.6V, V_O (high) = V_{SS}	-55		
C_{IO}	Input/output capacitance	Any input, output, or I/O		7	pF

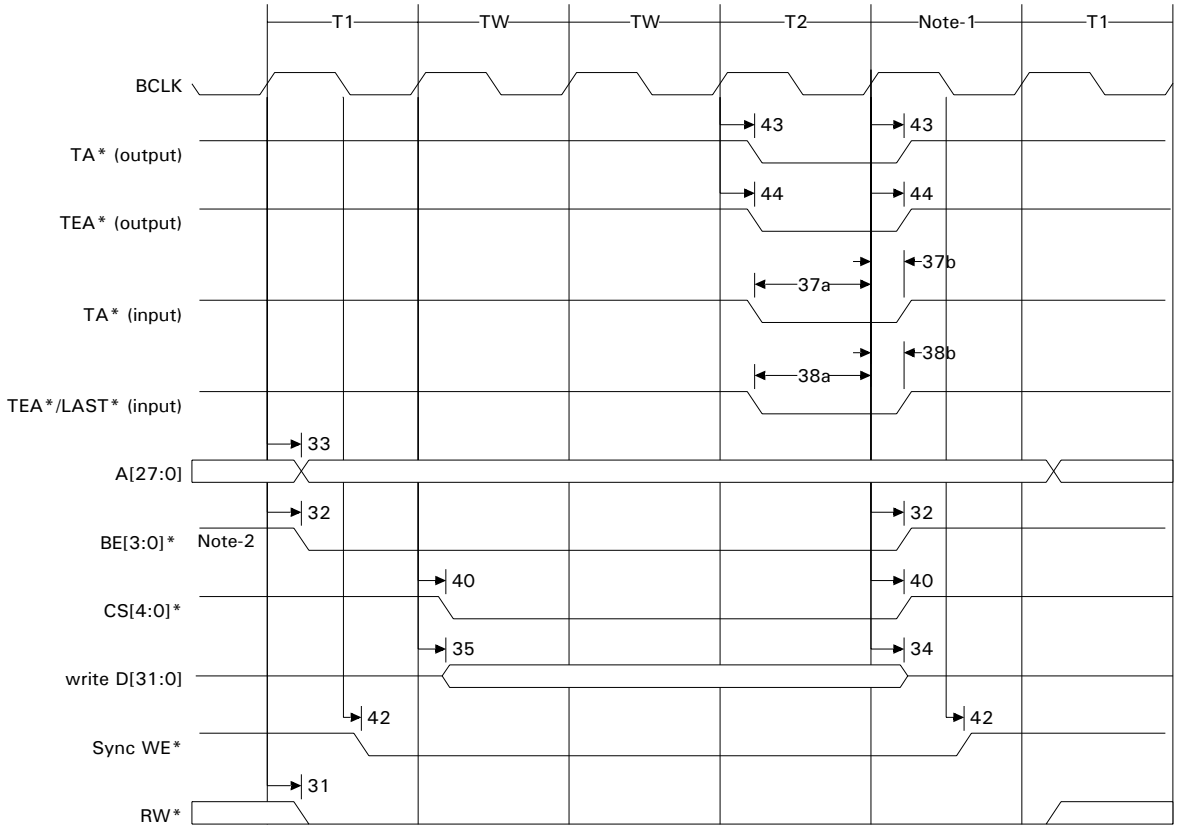
DC absolute maximum voltages

Characteristic	Min.	Max.
Supply voltage 2.5 V — core	-0.3	3.15
Supply voltage 3.3 V — I/O	-0.3	4.00
Input voltage	-0.3	4.50
Output voltage	-0.3	4.50

Temperature considerations

Characteristic	Min.	Max.
Thermal resistance — junction to ambient	37°C/W	
Operating junction temperature (°C)	-40°	100°
Operating ambient temperature (°C)	-40°	85°
Storage temperature (°C)	-60°	150°

SRAM Sync Write (Wait = 2)



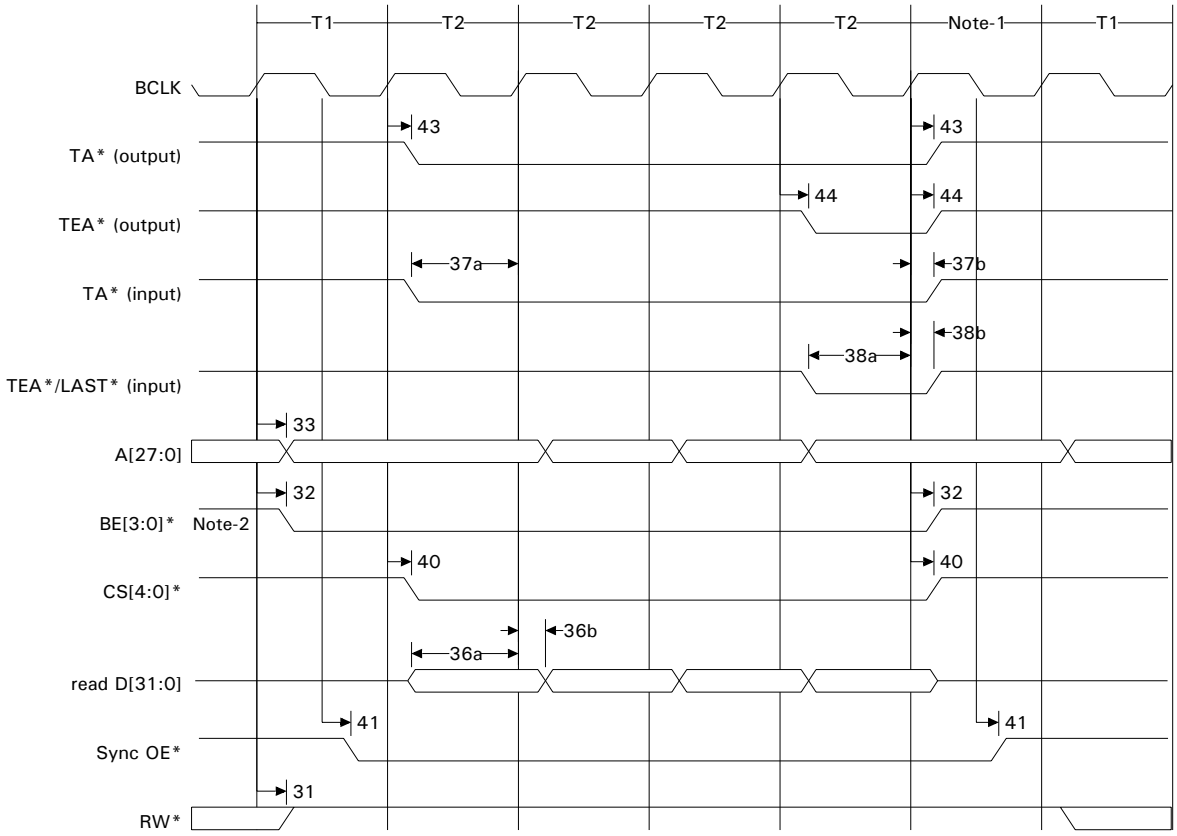
Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

SRAM Sync Burst Read (2-111, Wait = 0, BCYC = 00)



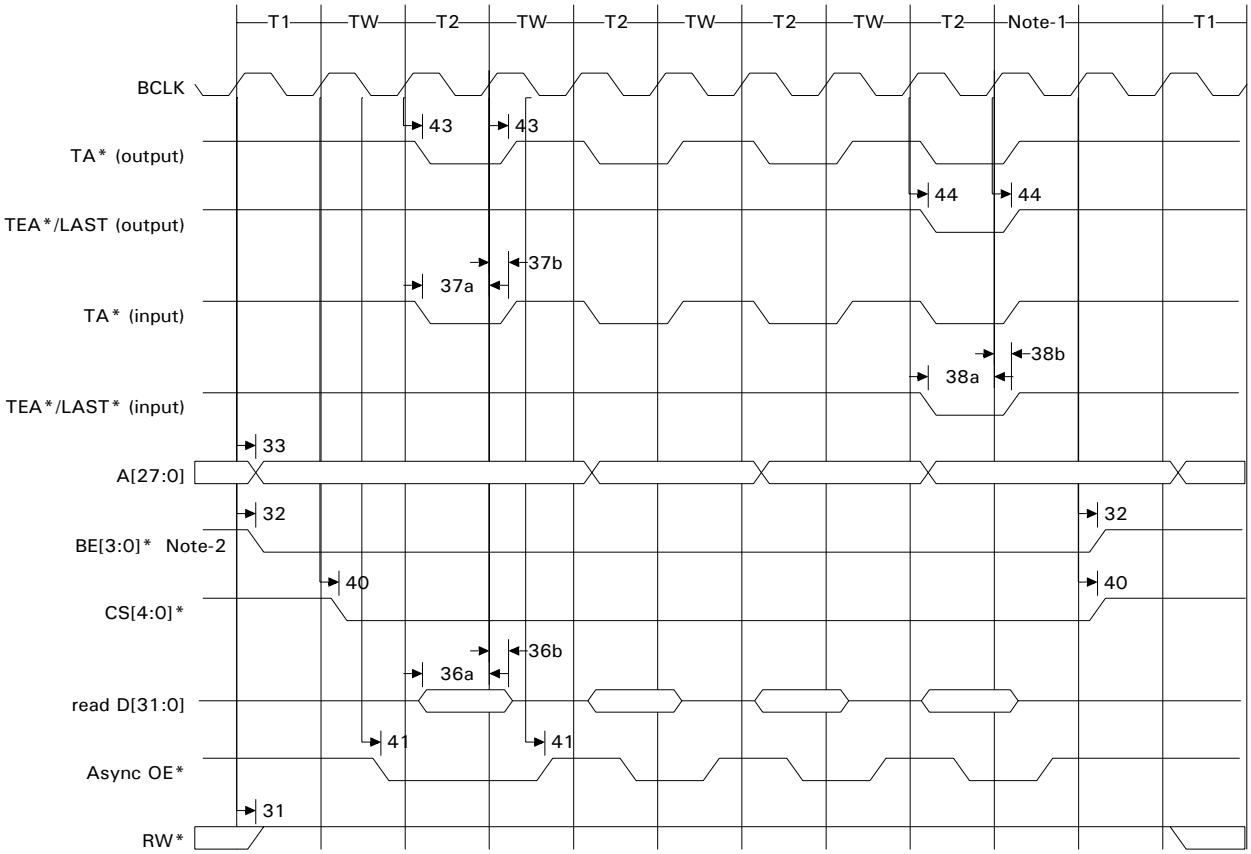
Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

SRAM Async Burst Read (Wait = 2, BCYC = 01)



Notes:

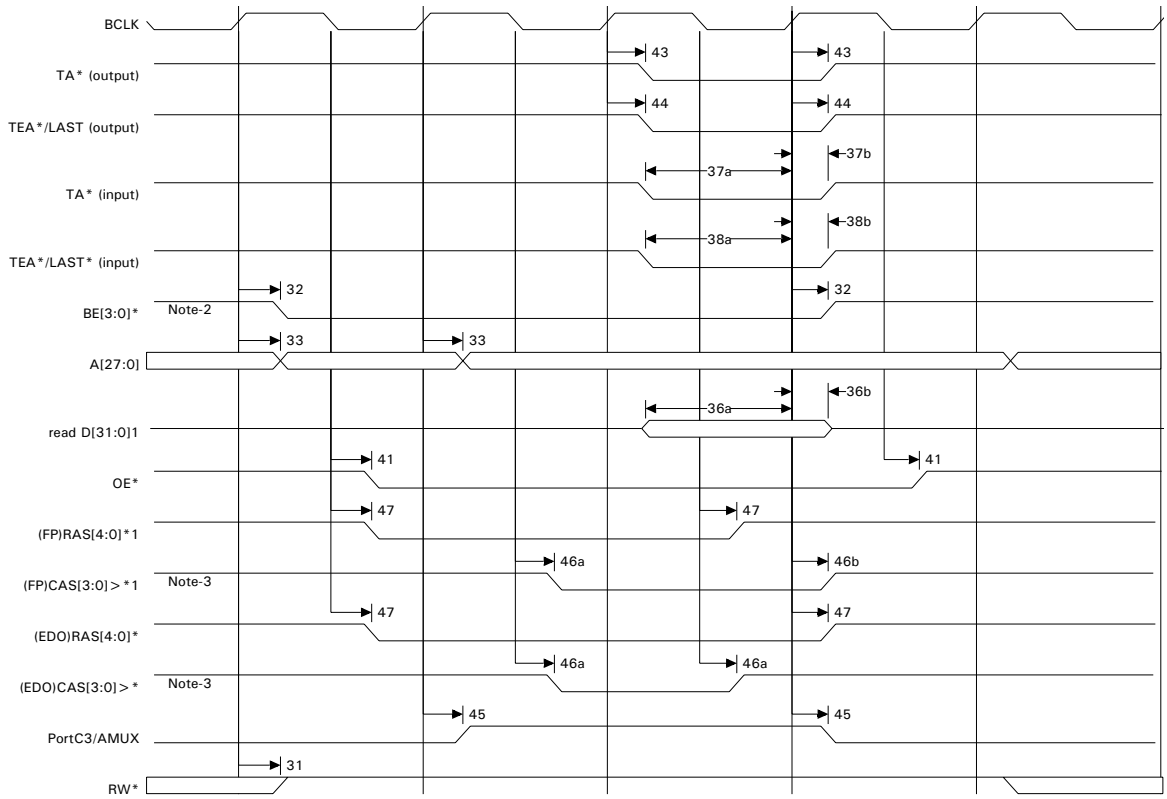
1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 The TW cycles are present when the WAIT field is set to 2 or more.

Fast Page and EDO DRAM Read



Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

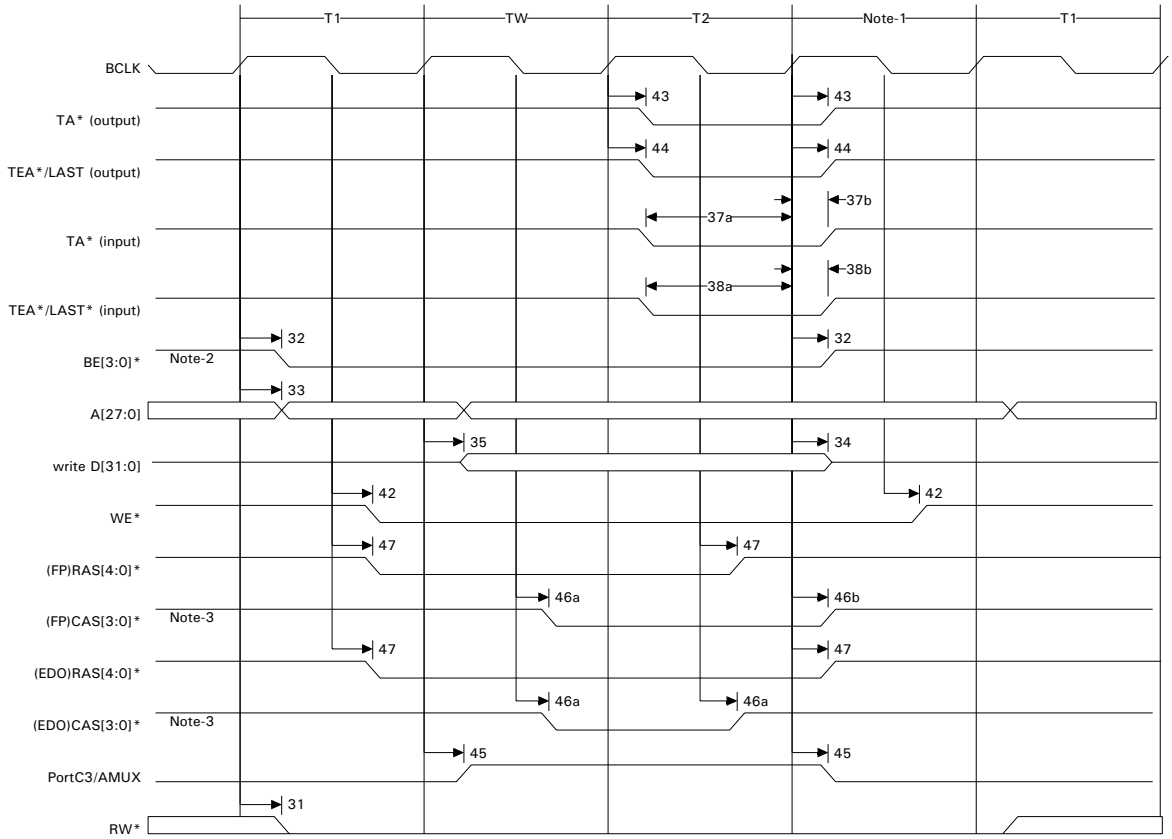
2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 Port size determines which CAS* signals are active:

8-bit port = CAS3*
16-bit port = CAS[3:2]*
32-bit port = CAS[3:0]*

Fast Page and EDO DRAM Write



Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

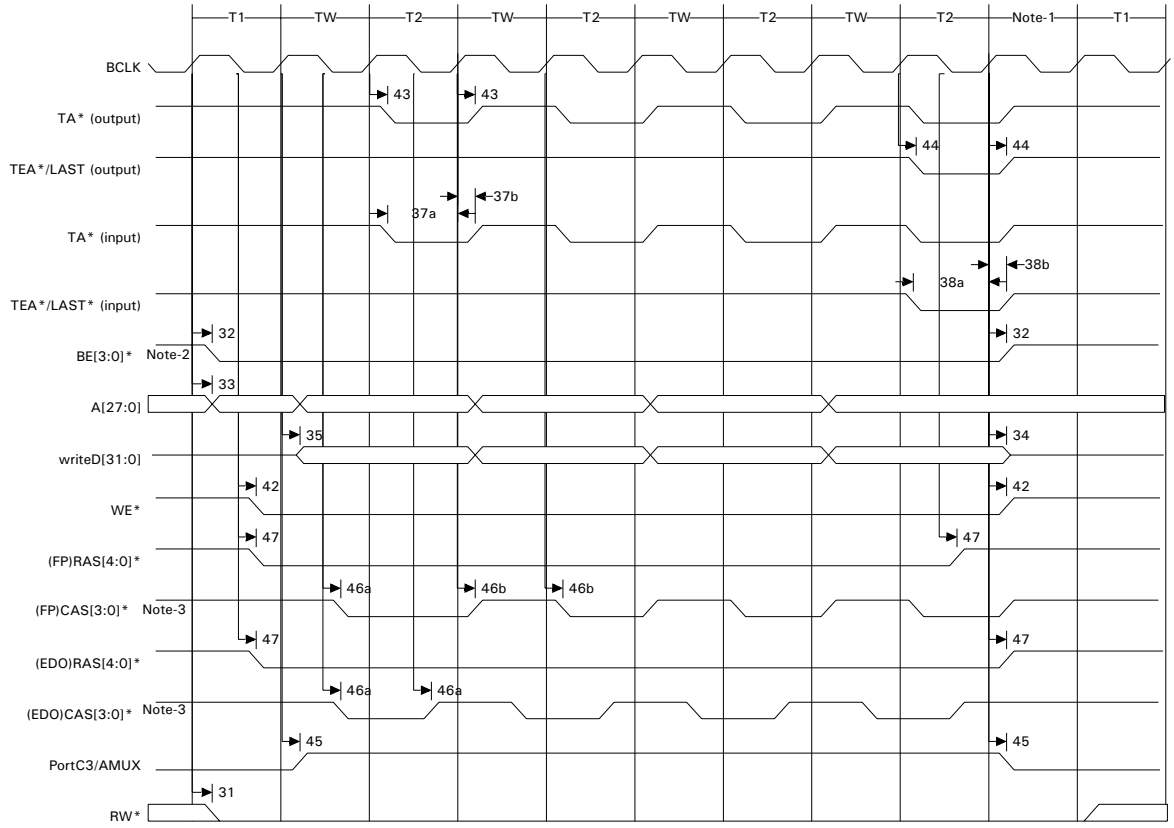
2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 Port size determines which CAS* signals are active:

8-bit port = CAS3*
16-bit port = CAS[3:2]*
32-bit port = CAS[3:0]*

Fast Page and EDO DRAM Burst Write



Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

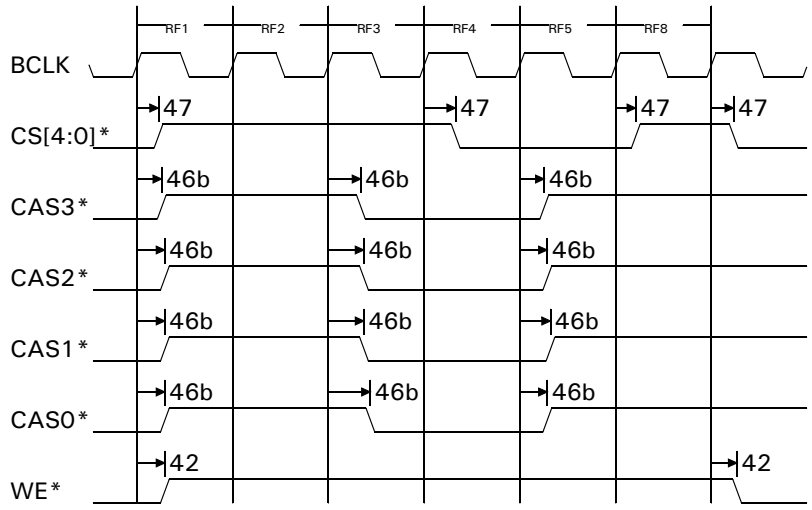
8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 Port size determines which CAS* signals are active:

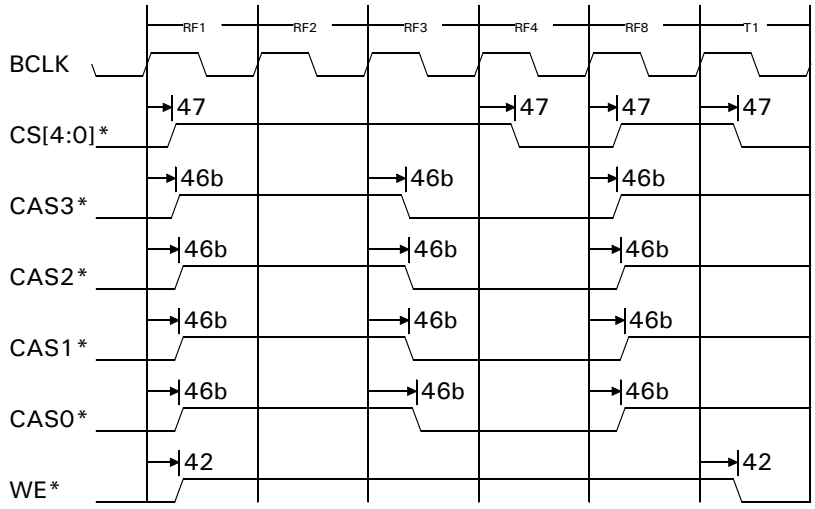
8-bit port = CAS3*
16-bit port = CAS[3:2]*
32-bit port = CAS[3:0]*

4 The BCYC field in the Chip Select Option register should never be set to 00 for Fast Page and EDO DRAM.

Fast Page and EDO DRAM Refresh (RCYC = 2)

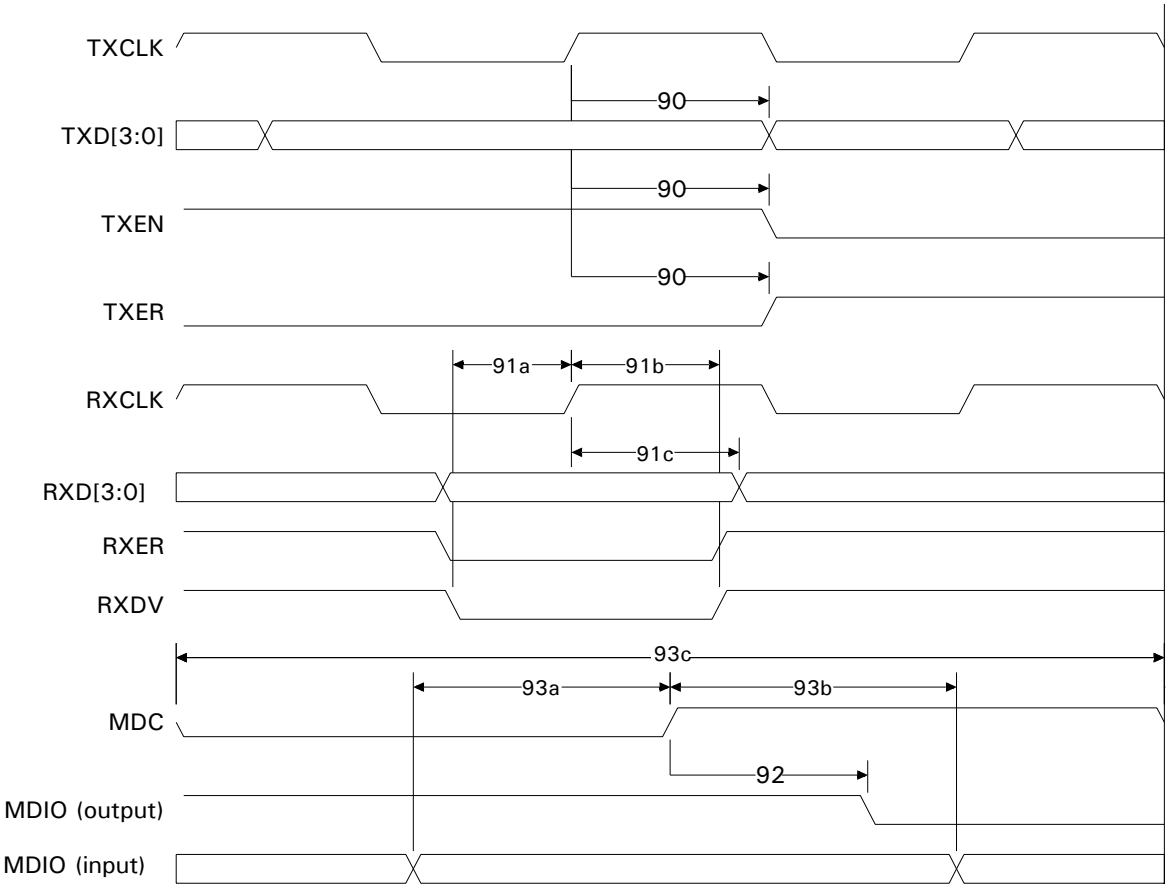


Fast Page and EDO DRAM Refresh (RCYC = 3)



Ethernet timing

Number	Characteristic	Min.	Max.	Unit
90	TXCLK high to TXD, TXEN, TXER valid	5	17	ns
91a	RXD, RXER, RXDV valid to RXCLK high (setup)	8		ns
91b	RXCLK high to RXD, RXER, RXDV hold time	0		ns
91c	RXCLK high to RXD hold time	0		ns
92	MDC high to MDIO change	40	50	ns
93a	MDIO valid to MDC high (setup)	10		ns
93b	MDC high to MDIO hold time	0		ns
93c	MDC cycle time		SYSCLK/10	
94	RXCLK high to RPSF* change		6.5	ns
95a	REJECT* valid to RXCLK high (setup)	2.6		ns
95b	REJECT* valid from RXCLK high (hold)	0		ns
96	CRS low to RXCLK idle	27		Bit-Time



ENI timing

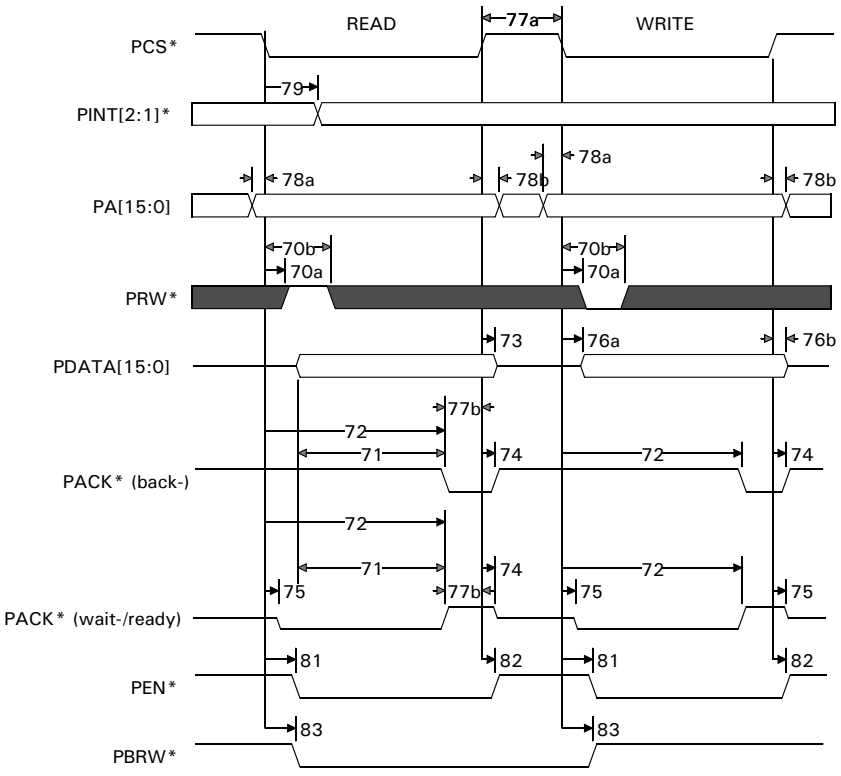
The data shown is independent of SYS_CLK and BCLK settings. Units are nanoseconds (ns).

Num	Characteristic	Note	Min	Max
70a	PCS*/PDACK* low to PRW* sampled	1		T_{SYS} - 2.5
70b	PCS*/PDACK* low to PRW* hold time	1	$4*T_{SYS}$	
71	Read Data Valid to PACK* valid		T_{SYS}	
72	PCS*/PDACK* low to PACK* low	3	T_{SYS}	$6*T_{SYS}$
72a	PCS* low to PACK* low	4	$7*T_{SYS}$	Determined by shared RAM access time
72b	PCS*/PACK* low to PACK* low	5	$2*T_{SYS}$	$4*T_{SYS}$
72c	PCS* low to PACK* valid (shared RAM only)	6	$7*T_{SYS}$	Determined by shared RAM access time
73	PCS*/PDACK* high to PDATA high impedance		0	7.84
74	PCS*/PDACK* high to PACK* high		0	13
75	PCS*/PDACK* low to PACK* (wait-) low		0	14
76a	PCS*/PDACK* low to Write Data valid			$2*T_{SYS}$
76b	PCS*/PDACK* high to Write Data hold time		0	
77a	PCS*/PDACK* width high (recovery)		16	
77b	PACK* low to PCS*/PDACK* high (hold)	8	0	
77c	PDACK* minimum low		120	
78a	Address valid to PCS* low		0	
78b	PCS* high to Address hold time		0	
79	PCS* low to PINT1/2 change (write)		$3*T_{SYS}$	$5*T_{SYS}$
80a	PDACK* low to PDRQI*, PDRQO* high			$5*T_{SYS}$
80b	PDRQO* high width		$5*T_{SYS}$	
80c	PDRQI* high width		$4*T_{SYS}$	
80d	PDACK* low to PINT2 low			14
80e	PDACK* high to PINT2 high		15	
81	PCS*/PDACK* low to PEN* low	2	$1*T_{SYS}$	$3*T_{SYS}$
82	PCS*/PDACK* high to PEN* high	2	0	13
83	PCS*/PDACK* low to PBRW* low	2	$1*T_{SYS}$	$2*T_{SYS}$
84a	PRW* valid to PDACK* low (setup)	1	0	
84b	PDACK* high to PRW* hold time	1	0	
85	PDACK* low to PDATA valid	7	$3*T_{SYS}$	$5*T_{SYS}$
85a	PDACK* low to PDATA valid	7	$1*T_{SYS}$	$2*T_{SYS}$

Notes:

1. Parameters 70a and 70b apply only when the ENI FAST bit is set to 0. When ENI FAST is set to 1, parameters 84a and 84b apply.
2. The PEN* and PBRW* signals control an external bi-directional data bus transceiver for the PDATA bus that can drive only 2 mA.
3. Parameter 72 applies only to ENI registers when FAST is set to 0. This does *not* apply to shared RAM access.
4. Parameter 72a applies to all shared RAM accesses when FAST is set to 0. The max specification for PCS* to PACK* valid is larger for shared RAM accesses. The additional delay depends on the speed of the external RAM assigned to provide the physical shared RAM. Consequently, the maximum specification for shared RAM accesses is system-dependent.
5. Parameter 72b applies to ENI register accesses when FAST is set to 1.
6. Parameter 72c applies to ENI shared RAM accesses when FAST is set to 1.
7. Parameter 85 applies when FAST is set to 0. Parameter 85a applies when FAST is set to 1.
8. Parameter 77c can be reduced to $3*T_{SYS}$ when FAST is set to 1.

ENI Shared RAM and Register Cycle timing



P/N: 91001374_B (formerly 8820002A)

Release date: March 2006

Digi International
11001 Bren Road East
Minnetonka, MN 55343 U.S.A.
United States: +1 877 912-3444
Other locations: +1 952 912-3444
Fax: +1 952 912-4960
www.digi.com/support
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