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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

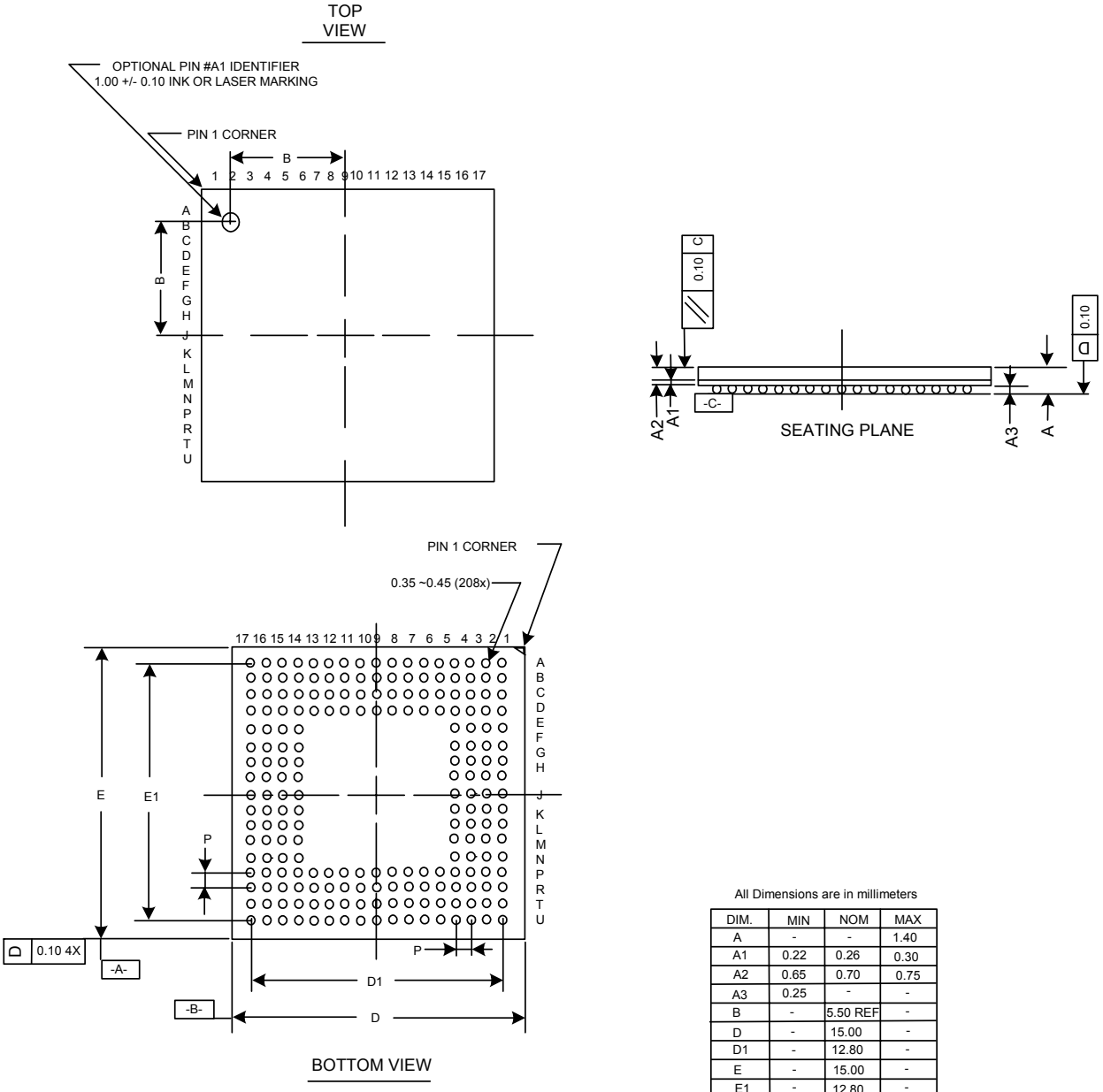
Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Network Processor
Core Processor	ARM7®
Program Memory Type	External Program Memory
Controller Series	NET+50
RAM Size	16K x 8
Interface	EBI/EMI, Ethernet, DMA, HDLC, IEEE1284/ENI, SPI, UART
Number of I/O	40
Voltage - Supply	2.25V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/digi-international/net-50-qinp-3

Packaging dimensions and pinout

The NET+50 is available in two package options — a ball-grid array (BGA) or a plastic quad flat pack (PQFP).

BGA packaging and pinout diagram

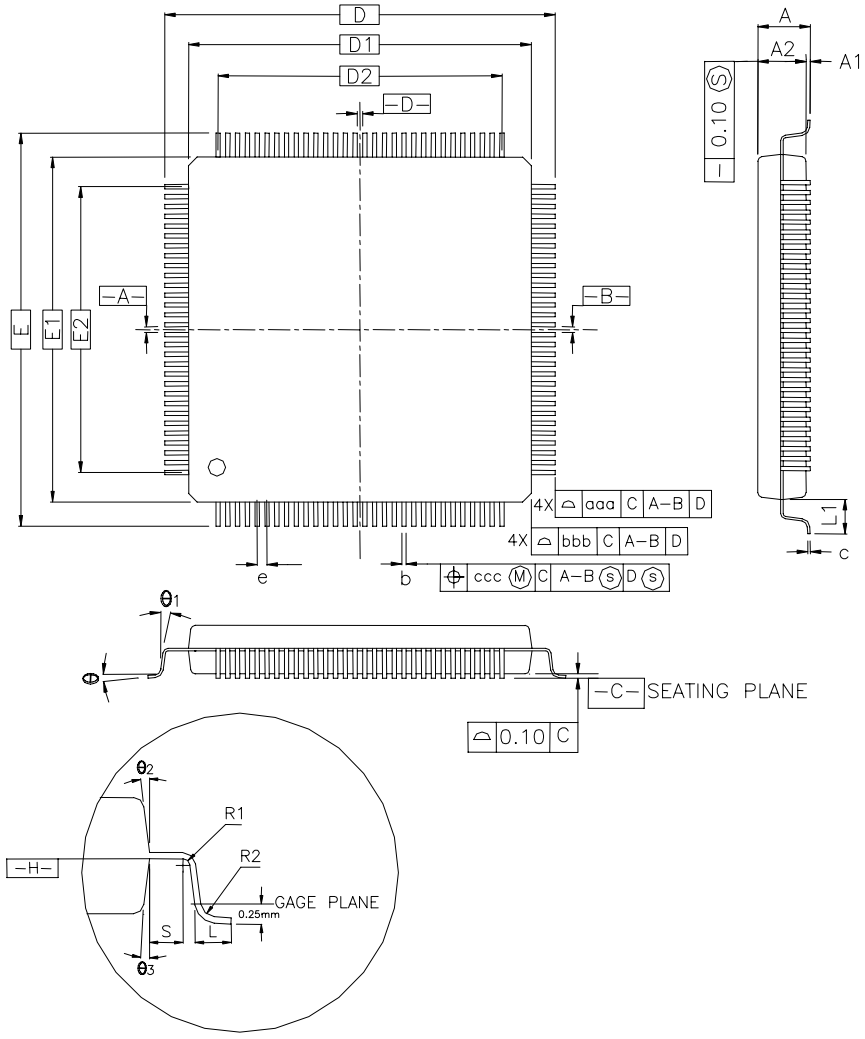


All Dimensions are in millimeters

DIM.	MIN	NOM	MAX
A	-	-	1.40
A1	0.22	0.26	0.30
A2	0.65	0.70	0.75
A3	0.25	-	-
B	-	5.50 REF	-
D	-	15.00	-
D1	-	12.80	-
E	-	15.00	-
E1	-	12.80	-
P	-	0.80	-

PQFP packaging and pinout diagrams

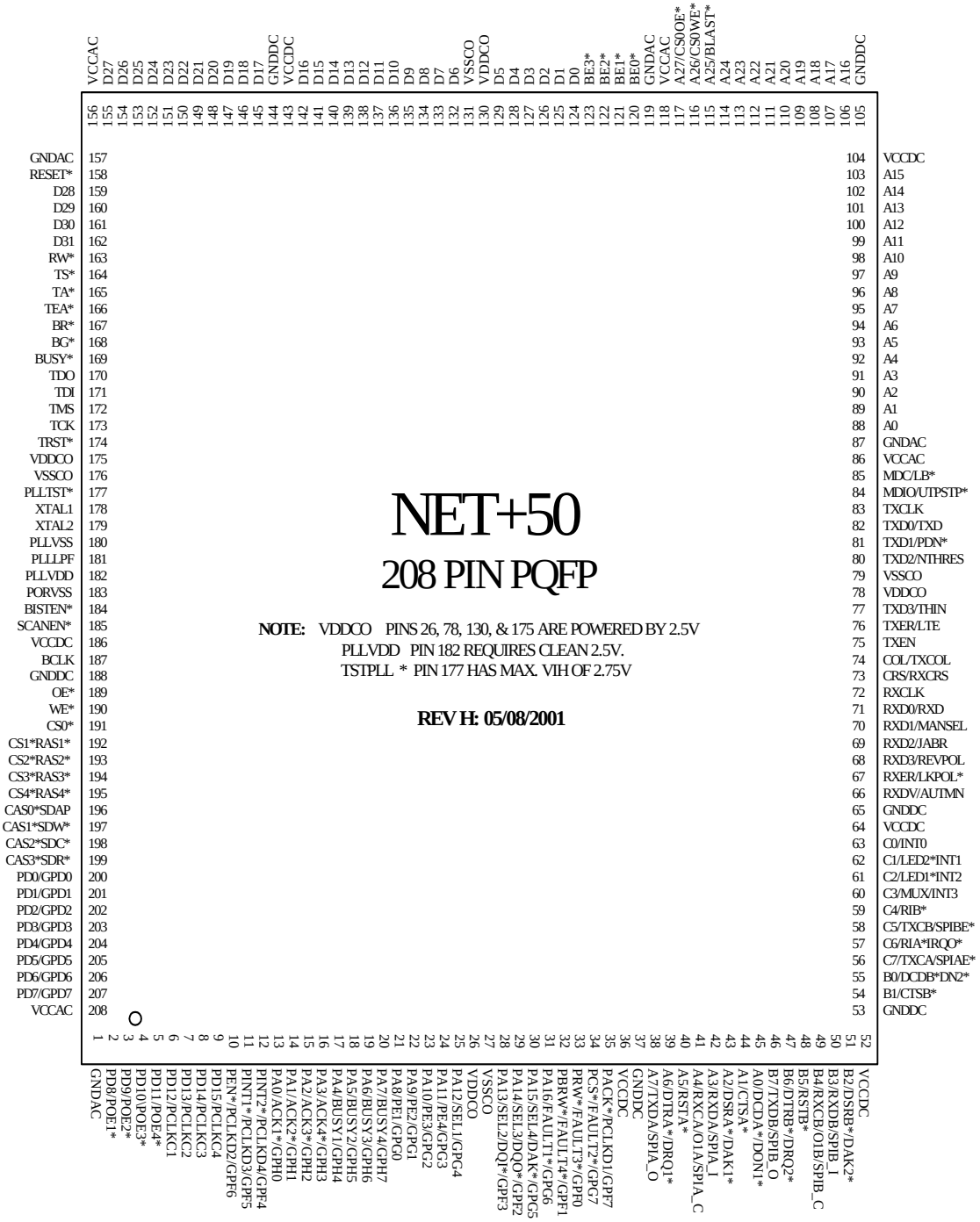
PQFP packaging



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	4.10	—	—	0.161
A_1	0.25	—	—	0.010	—	—
A_2	3.20	3.32	3.60	0.126	0.131	0.142
D	31.20 BASIC			1.228 BASIC		
D_1	28.00 BASIC			1.102 BASIC		
E	31.20 BASIC			1.228 BASIC		
E_1	28.00 BASIC			1.102 BASIC		
R_2	0.13	—	0.30	0.005	—	0.012
R_1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ_1	0°	—	—	0°	—	—
θ_2	8° REF			8° REF		
θ_3	8° REF			8° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L_1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	25.50			1.004		
E2	25.50			1.004		
TOLERANCES OF FORM AND POSITION						
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	0.08			0.003		

PQFP pinout


NET+50
208 PIN PQFP
NOTE: VDDCO PINS 26, 78, 130, & 175 ARE POWERED BY 2.5V
PLLVDD PIN 182 REQUIRES CLEAN 2.5V.
TSTPLL * PIN 177 HAS MAX. VIH OF 2.75V
REV H: 05/08/2001
1 GNDAC
2 PD8/POE1*
3 PD9/POE2*
4 PD10/POE3*
5 PD11/POF4*
6 PD12/PCLKC1
7 PD13/PCLKC2
8 PD14/PCLKC3
9 PD15/PCLKC4
10 PEN*/PCLKD2/GPF6
11 PINT1*/PCLKD3/GPF5
12 PINT2*/PCLKD4/GPF4
13 PA0/ACK1*/GPH0
14 PA1/ACK2*/GPH1
15 PA2/ACK3*/GPH2
16 PA3/ACK4*/GPH3
17 PA4/BUSY1/GPH4
18 PA5/BUSY2/GPH5
19 PA6/BUSY3/GPH6
20 PA7/BUSY4/GPH7
21 PA8/PE1/GPG0
22 PA9/PE2/GPG1
23 PA10/PE3/GPG2
24 PA11/PE4/GPG3
25 PA12/SEL1/GPG4
26 VDDCO
27 VSSCO
28 PA13/SEL2/DQI*/GPF3
29 PA14/SEL3/DQO*/GPF2
30 PA15/SEL4/DAK*/GPG5
31 PA16/FAULT1*/GPG6
32 PBRW*/FAULT4*/GPF1
33 PRW*/FAULT3*/GPF0
34 PCS*/FAULT2*/GPG7
35 PACK*/PCLKD1/GPF7
36 VCCDC
37 GNDDC
38 A7/TXDA/SPIA_O
39 A6/DTRA*/DRQ1*
40 A5/RSTA*
41 A4/RXCA/O1A/SPIA_C
42 A3/RXDA/SPIA_I
43 A2/DSRA*/DAK1*
44 A1/CTSA*
45 A0/DCDA*/DDN1*
46 B7/TXDB/SPIB_O
47 B6/DTRB*/DRQ2*
48 B5/RSTB*
49 B4/RXCB/O1B/SPIB_C
50 B3/RXDB/SPIB_I
51 B2/DSRB*/DAK2*
52 VCCDC
53 GNDDC
54 B1/CTSB*
55 B0/DCDB*DN2*
56 C7/TXCA/SPIAE*
57 C6/RIA*IRQO*
58 C5/TXCB/SPIBE*
59 C4/RIB*
60 C3/MUX/INT3
61 C2/LED1*INT2
62 C1/LED2*INT1
63 C0/INT0
64 VCCDC
65 GNDDC
66 RXDV/AUTMN
67 RXER/LKPOL*
68 RXD3/REVPOL
69 RXD2/JABR
70 RXD1/MANSEL
71 RXD0/RXD
72 RXCLK
73 CRS/RXCRS
74 COL/TXCOL
75 TXEN
76 TXER/LTE
77 TXD3/THIN
78 VDDCO
79 VSSCO
80 TXD2/NTHRES
81 TXD1/PDN*
82 TXD0/TXD
83 TXCLK
84 MDIO/UTPSTP*
85 MDC/LB*
86 VCCAC
87 GNDAC
88 A0
89 A1
90 A2
91 A3
92 A4
93 A5
94 A6
95 A7
96 A8
97 A9
98 A10
99 A11
100 A12
101 A13
102 A14
103 A15
104 VCCDC
105 GNDDC
106 A16
107 A17
108 A18
109 A19
110 A20
111 A21
112 A22
113 A23
114 A24
115 A25/BLAST*
116 A26/CS0WE*
117 A27/CS0OE*
118 VCCAC
119 GNDAC
120 BE0*
121 BE1*
122 BE2*
123 BE3*
124 D0
125 D1
126 D2
127 D3
128 D4
129 D5
130 VDDCO
131 VSSCO
132 D6
133 D7
134 D8
135 D9
136 D10
137 D11
138 D12
139 D13
140 D14
141 D15
142 D16
143 VCCDC
144 GNDDC
145 D17
146 D18
147 D19
148 D20
149 D21
150 D22
151 D23
152 D24
153 D25
154 D26
155 D27
156 VCCAC
157 GNDAC
158 RESET*
159 D28
160 D29
161 D30
162 D31
163 RW*
164 TS*
165 TA*
166 TEA*
167 BR*
168 BG*
169 BUSY*
170 TDO
171 TDI
172 TMS
173 TCK
174 TRST*
175 VDDCO
176 VSSCO
177 PLLTST*
178 XTAL1
179 XTAL2
180 PLLVSS
181 PLLLPF
182 PLLVDD
183 PORVSS
184 BISTEN*
185 SCANEN*
186 VCCDC
187 BCLK
188 GNDDC
189 OE*
190 WE*
191 CS0*
192 CS1*RAS1*
193 CS2*RAS2*
194 CS3*RAS3*
195 CS4*RAS4*
196 CAS0*SDAP
197 CAS1*SDW*
198 CAS2*SDC*
199 CAS3*SDR*
200 PD0/GPD0
201 PD1/GPD1
202 PD2/GPD2
203 PD3/GPD3
204 PD4/GPD4
205 PD5/GPD5
206 PD6/GPD6
207 PD7/GPD7
208 VCCAC

Pinout detail tables

The pinout tables in the following sections have the following columns:

Signal	The pin name for each I/O signal.Some signals have dual modes and are identified accordingly. The mode is configured through firmware using a configuration register. Some modes may require hardware configuration during a RESET condition
BGA	The BGA pin number for specific I/O signals.
PQFP	The PQFP pin number for specific I/O signals.
†	A dagger indicates a pin that is an input current source. (The daggers appear in the BGA column, but this applies in PQFP layout as well.)
*	An asterisk indicates a pin that is *active low*.
I/O	The type of signal — input, output, or input/output (I/O).
OD	The output drive strength of an output buffer. The NET+50 uses one of three drivers: ■ 2 mA ■ 4 mA ■ 8 mA

System bus interface

Signal		BGA	PQFP	I/O	OD	Description	
BCLK		T10	187	O	8	Synchronous bus clock	
ADDR27	CS0OE*	F4 †	117	I/O	4	Address bus	Chip select 0 output enable
ADDR26	CS0WE*	F3 †	116	I/O	4	Address bus	Chip select 0 write enable
ADDR25	BLAST*	E2 †	115	I/O	4	Address bus	Burst-terminated input
ADDR24		D2 †	114	I/O	4		
ADDR23		E3 †	113	I/O	4		
ADDR22		E4 †	112	I/O	4		
ADDR21		D1 †	111	I/O	4		
ADDR20		C2 †	110	I/O	4		
ADDR19		D3 †	109	I/O	4		
ADDR18		C1 †	108	I/O	4		
ADDR17		B1 †	107	I/O	4		
ADDR16		B2 †	106	I/O	4		
ADDR15		B3 †	103	I/O	4		
ADDR14		A3 †	102	I/O	4		
ADDR13		A4 †	101	I/O	4		
ADDR12		B4 †	100	I/O	4		

System bus interface (cont.)

Signal	BGA	PQFP	I/O	OD	Description
ADDR11	C3 †	99	I/O	4	
ADDR10	A5 †	98	I/O	4	
ADDR9	D4 †	97	I/O	4	
ADDR8	C4 †	96	I/O	4	
ADDR7	B5 †	95	I/O	4	
ADDR6	A6 †	94	I/O	4	
ADDR5	D5 †	93	I/O	4	
ADDR4	C5 †	92	I/O	4	
ADDR3	B6 †	91	I/O	4	
ADDR2	A7 †	90	I/O	4	
ADDR1	D6 †	89	I/O	4	
ADDR0	C6 †	88	I/O	4	
DATA31	T3	162	I/O	4	Data bus
DATA30	R4	161	I/O	4	
DATA29	U3	160	I/O	4	
DATA28	U2	159	I/O	4	
DATA27	R2	155	I/O	4	
DATA26	R1	154	I/O	4	
DATA25	P1	153	I/O	4	
DATA24	P2	152	I/O	4	
DATA23	R3	151	I/O	4	
DATA22	N1	150	I/O	4	
DATA21	P4	149	I/O	4	
DATA20	P3	148	I/O	4	
DATA19	N2	147	I/O	4	
DATA18	M1	146	I/O	4	
DATA17	N4	145	I/O	4	
DATA16	L1	142	I/O	4	
DATA15	M4	141	I/O	4	
DATA14	M3	140	I/O	4	
DATA13	L2	139	I/O	4	
DATA12	K1	138	I/O	4	

UARTs, SPI, and GPIO

GPIO	UART / HDLC	Special / DMA mode	BGA	PQFP	I/O	OD	SPI slave mode	SPI master mode
PORTA7	TXDA		G17 †	38	I/O	2	SPI-S-TXD-O-A	SPI-M-TXD-O-A
PORTA6	DTRA*	DRQ1*	F16 †	39	I/O	2		
PORTA5	RTSA*		E15 †	40	I/O	2		
PORTA4		RXCA	E14 †	41	I/O	2	SPI-S-CLK-I-A	SPI-M-CLK-O-A
PORTA3	RXDA		F17 †	42	I/O	2	SPI-S-RXD-I-A	SPI-M-RXD-I-A
PORTA2	DSRA*	DAK1*	E16 †	43	I/O	2		
PORTA1	CTSA*		D15 †	44	I/O	2		
PORTA0	DCDA*	DON1*	D14 †	45	I/O	2		
PORTB7	TXDB		E17 †	46	I/O	2	SPI-S-TXD-O-B	SPI-M-TXD-O-B
PORTB6	DTRB*	DRQ2*	C15 †	47	I/O	2		
PORTB5	RTSB*		D16 †	48	I/O	2	Reject* Ethernet packet	
PORTB4		RXCB	D17 †	49	I/O	2	SPI-S-CLK-I-B	SPI-M-CLK-O-B
PORTB3	RXDB		C17 †	50	I/O	2	SPI-S-RXD-I-B	SPI-M-RXD-O-B
PORTB2	DSRB*	DAK2*	C16 †	51	I/O	2		
PORTB1	CTSB*		B16 †	54	I/O	2	RPSF* Ethernet frame boundary	
PORTB0	DCDB*	DON2*	A16 †	55	I/O	2		
PORTC7		TXCA	A15 †	56	I/O	2	SPI-S-EN-I-A	SPI-M-EN-O-A
PORTC6	RIA*	IRQO*	C14 †	57	I/O	2		
PORTC5		TXCB	B15 †	58	I/O	2	SPI-S-EN-I-B	SPI-M-EN-O-B
PORTC4	RIB*		A14 †	59	I/O	2		
PORTC3		AMUX	D13 †	60	I/O	8	Interrupt 3	
PORTC2			C13 †	61	I/O	8	Interrupt 2	
PORTC1			B14 †	62	I/O	8	Interrupt 1	
PORTC0			B13 †	63	I/O	8	Interrupt 0	

DMA controller module

DMA register key: 0xFF90*nnnn* where *nnnn* = DMAx + Offset							
DMA*x*:						**Offset:**	
1A:	00	2:	80	6:	100	00	Buffer descriptor pointer
1B:	20	3:	A0	7:	120	10	Buffer control register
1C:	40	4:	C0	8:	140	14	Buffer status register
1D:	60	5:	E0	9:	160		
				10:	180		

Examples:	
0xFF90 0000	DMA 1A buffer descriptor pointer
0xFF90 0010	DMA 1A buffer control register
0xFF90 0014	DMA 1A buffer status register

Ethernet controller module

Address	Register	Address	Register
0xFF80 0000	General control register	0xFF80 0440 – 0478	Transmit control registers
0xFF80 0004	General status register	0xFF80 0480 – 0488	Receive control registers
0xFF80 0008	FIFO data register	0xFF80 040C0	Link fail counter
0xFF80 000C	FIFO last word data register	0xFFB0 0500	10 Mbit jabber counter
0xFF80 0010	TX status register	0xFFB0 0504	10 Mbit loss of carrier counter
0xFF80 0014	RX status register	0xFFB0 0540 – 0550	MII control registers
0xFF80 0400 – 0404	MAC configuration and test registers	0xFFB0 0580 – 059C	Status registers
0xFF80 0408 – 040C	PCS configuration and test registers	0xFFB0 05C0	SAL address filter register
0xFF80 0410 – 0414	STL configuration and test registers	0xFFB0 05C4 – 05DC	SAL hash table registers

Serial controller module

Address	Register	Address	Register
0xFFD0 0000 – 0030	Channel 1 registers	0xFFD0 0040 – 0070	Channel 2 registers

ENI controller module

Address	Register	Address	Register
0xFFA0 0000	General control register	0xFFA0 0030	ENI control register
0xFFA0 0004	General status register	0xFFA0 0034	ENI pulsed interrupt register
0xFFA0 0008	FIFO mode data register	0xFFA0 0038	ENI shared RAM address register
0xFFA0 0010 – 001C	IEEE1284 ports 1–4 control registers	0xFFA0 003C	ENI shared register
0xFFA0 0020 – 002C	IEEE 1284 ports 1–4 data registers	0xFFA0 0040 – 0050	GPIO ports D, F, G, H, and F registers

Test modes and PLL usage

The PLLTST*, BISTEN*, and SCANEN* primary inputs control test modes for test operations (in manufacturing) and for using an external oscillator instead of a crystal, as follows:

PLLTST*	BISTEN*	SCANEN*	Mode
1	1	1	Normal with PLL operational
0	1	1	Normal with PLL bypass
1	1	0	HiZ / Tri-state (manufacturing testing)

Note: All other combinations of these inputs are reserved.

PLL

When the PLLTST* signal is active low, the PLL is isolated, and the internal system clock is provided by the XTAL1 input (XTAL1 = SYSCLK). The PLL is not programmable. If you want to use the PLL (crystal) and get a system clock of 44.236 MHz, you must use an 18.432 MHz crystal.

HiZ/Tri-state

The NET+50 chip supports a way to tri-state all outputs. When both PLLTST* and BISTEN* are inactive (high) and SCANNEN* is active (low), all outputs are placed in a low current tri-state mode.

ARM debugging features

The ARM7TDMI core contains hardware extensions for advanced debugging. These extensions facilitate development and testing of application software, operating systems, and the hardware itself.

The debug extensions let you stop the core on a given instruction fetch (break-point) or data access (watchpoint), or asynchronously by a debug request. In such cases, the ARM processor is in *debug state* so you can examine the core's internal state and the system's external state. When the examination is complete, you can restore the core and system state, and resume program execution.

The ARM processor is put into debug state by an internal functional unit called *ICEBreaker*. In debug state, the core isolates itself from the memory system. You can examine the core while all other system activities — for example, DMA operations — continue normally.

You can examine the ARM processor's internal state through the 5-pin interface for debugging. This interface lets you serially insert instructions into the core's pipe-line without using the external data bus. Therefore, in debug state, you can insert a store-multiple into the instruction pipeline to dump the contents of the processor's registers. Data can be serially shifted out without affecting the rest of the system.

DC characteristics and other specifications

DC inputs

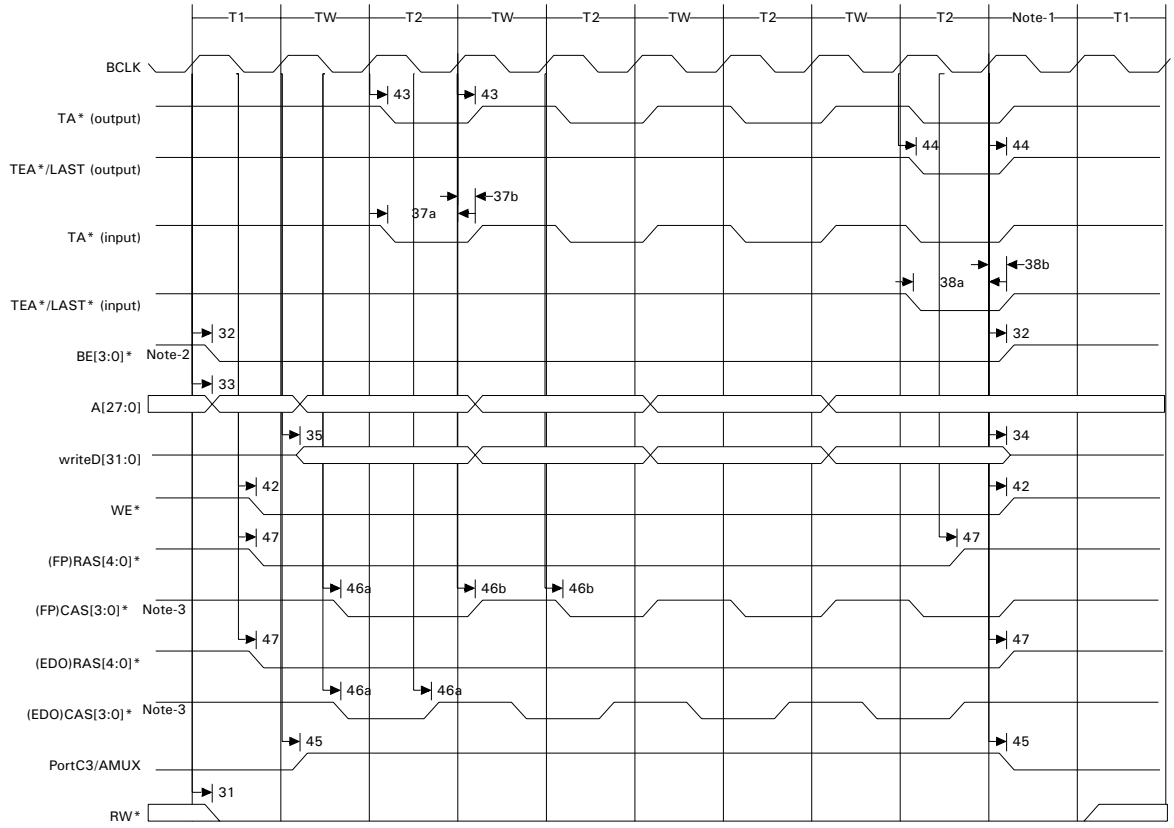
Symbol	Characteristic	Conditions	Min.	Typical	Max.	Unit
V_{DD}	DC supply voltage — core		2.25	2.5	2.75	V
V_{CC}	DC supply voltage — I/O		3.0	3.3	3.6	V
V_{IH}	Input high voltage		2.0		3.6	V
V_{IL}	Input low voltage		V_{SS} – 0.3		0.8	V
I_{IL}	Input buffer	$V_{IN} = V_{CC}$	-10		10	µA
	Input buffer with current sink		99		429	
I_{IH}	Input buffer	$V_{IN} = V_{SS}$	-10		10	µA
	Input buffer with current source		130		352	
C_{IN}	Input capacitance	Any input		7		pF
V_T	Switching threshold	Any input	1.4	2.0		V

SRAM timing

Number	Characteristic	Min.	Max.
31	BCLK high to RW* valid		19
32	BCLK high to BE* valid		16
33	BCLK high to Address valid	4	15
34	BCLK high to Data Out high impedance		17
35	BCLK high to Data Out valid		18
36a	Data In valid to BCLK high (setup)	8	
36b	BCLK high to Data In invalid (hold)	0	
37a	TA* valid to BCLK high (setup)	8	
37b	BCLK high to TA* invalid (hold)	0	
38a	TEA* valid to BCLK high (setup)	8.5	
38b	BCLK high to TEA* invalid (hold)	0	
40	BCLK high to CS* valid		16
41	BCLK low to OE* valid		14
42	BCLK low to WE* valid		16
43	BCLK high to TA* valid		11
44	BCLK high to TEA* valid		14

Minimum and maximum are in nanoseconds (ns).

Fast Page and EDO DRAM Burst Write



Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

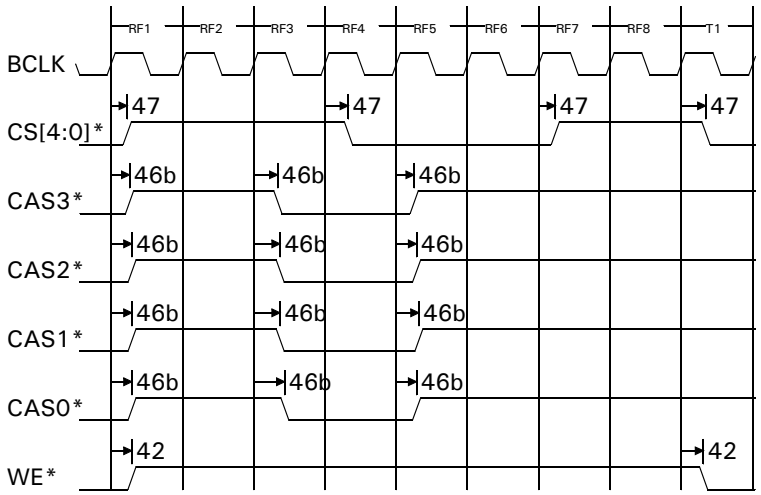
8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 Port size determines which CAS* signals are active:

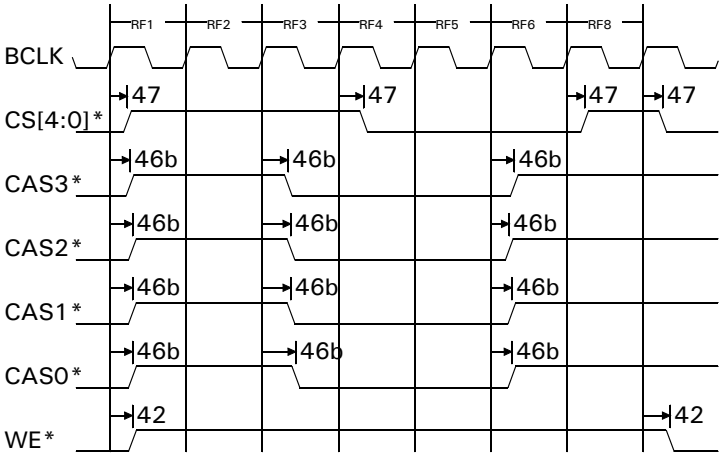
8-bit port = CAS3*
16-bit port = CAS[3:2]*
32-bit port = CAS[3:0]*

4 The BCYC field in the Chip Select Option register should never be set to 00 for Fast Page and EDO DRAM.

Fast Page and EDO DRAM Refresh (RCYC = 0)



Fast Page and EDO DRAM Refresh (RCYC = 1)

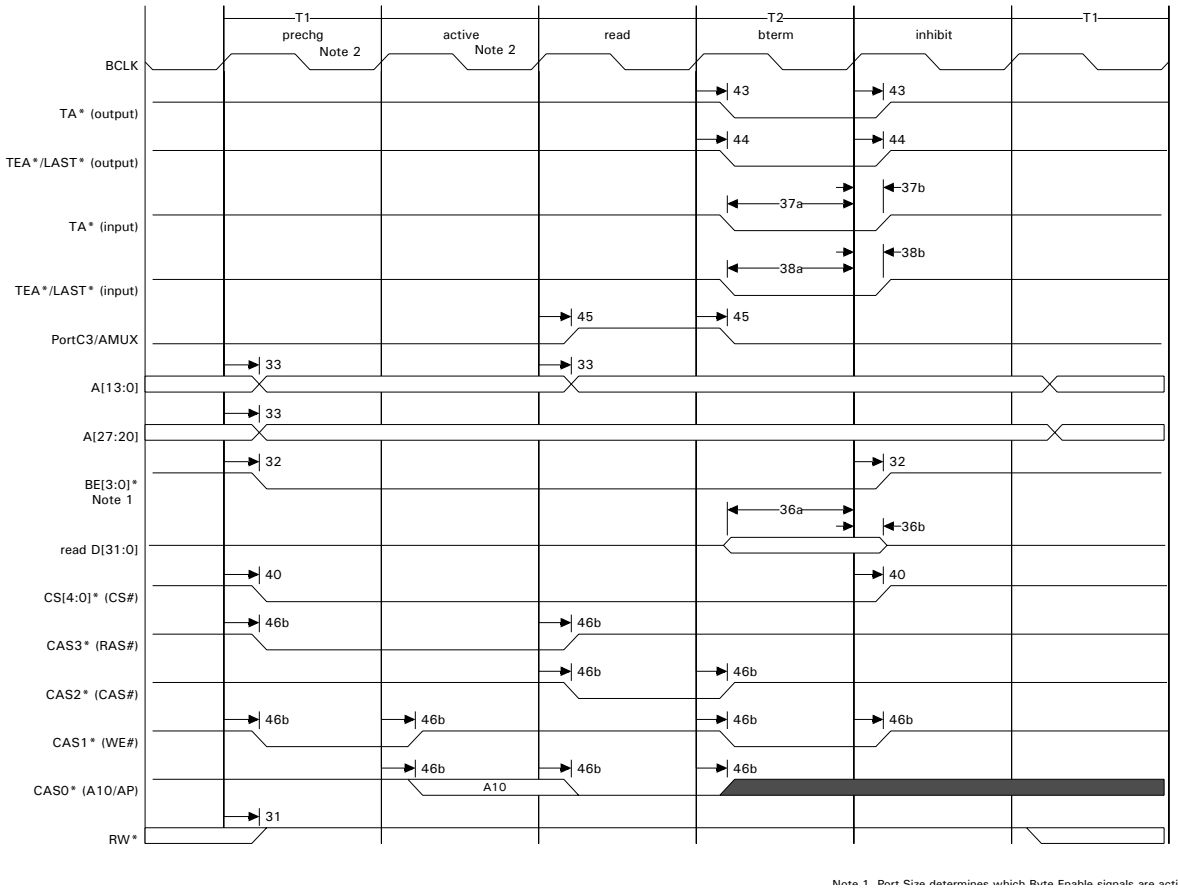


SDRAM timing

Number	Characteristic	Min.	Max.
31	BCLK high to RW* valid		19
32	BCLK high to BE* valid		16
33	BCLK high to Address valid	4	15
34	BCLK high to Data Out high impedance		17
35	BCLK high to Data Out valid		18
36a	Data In valid to BCLK high (setup)	8	
36b	BCLK high to Data In invalid (hold)	0	
37a	TA* valid to BCLK high (setup)	8	
37b	BCLK high to TA* invalid (hold)	0	
38a	TEA* valid to BCLK high (setup)	8.5	
38b	BCLK high to TEA* invalid (hold)	0	
40	BCLK high to CS* valid		16
41	BCLK low to OE* valid		14
42	BCLK low to WE* valid		16
43	BCLK high to TA* valid		11
44	BCLK high to TEA* valid		14

Minimum and maximum are in nanoseconds (ns).

SDRAM Read (CAS Latency = 1)



Note 1. Port Size determines which Byte Enable signals are active

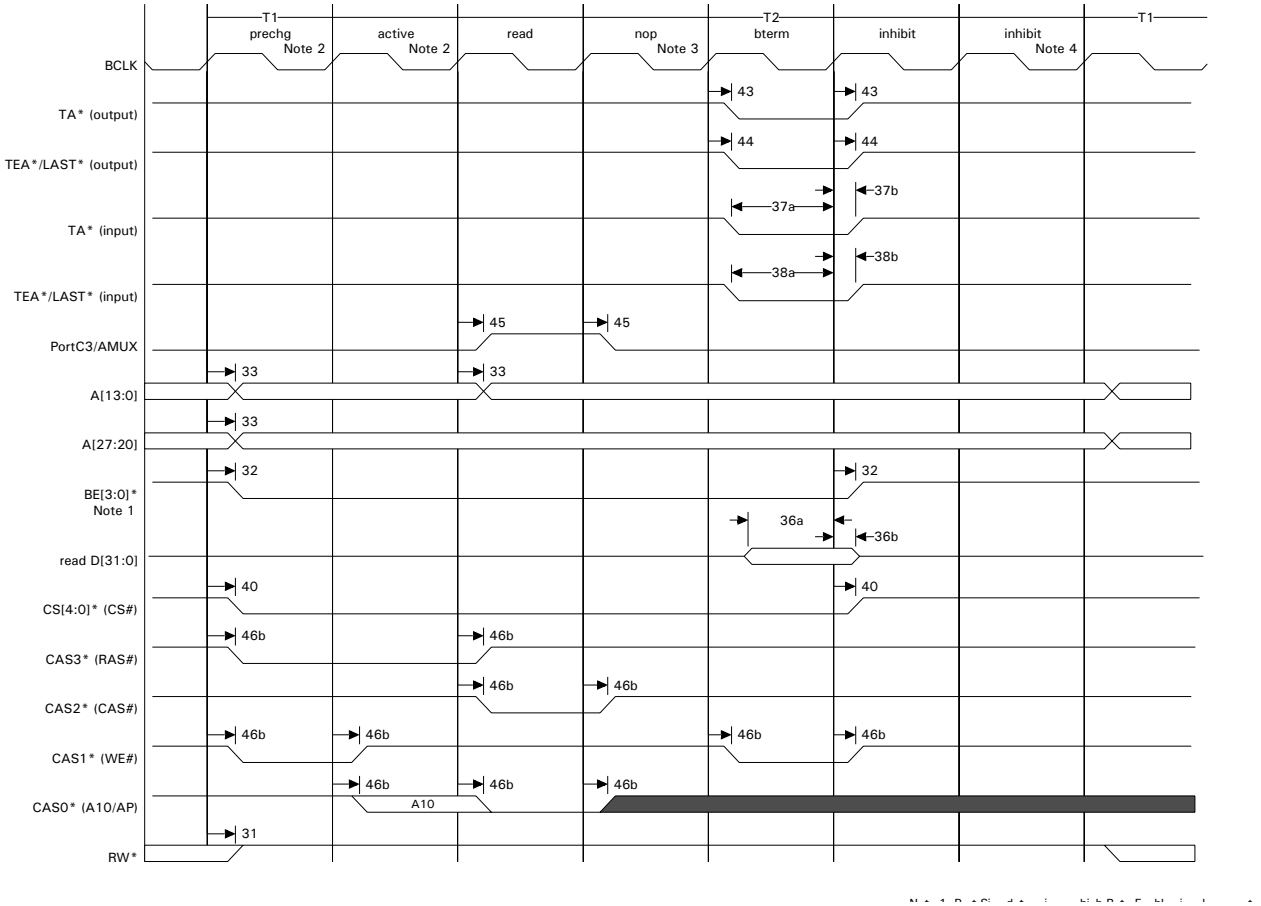
Notes:

1 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

2 The Precharge command or Active command or both are not always present. They depend on the address of the previous SDRAM access.

SDRAM Read (CAS Latency = 2)



Notes:

1 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

2 The Precharge command or Active command or both are not always present. They depend on the address of the previous SDRAM access.

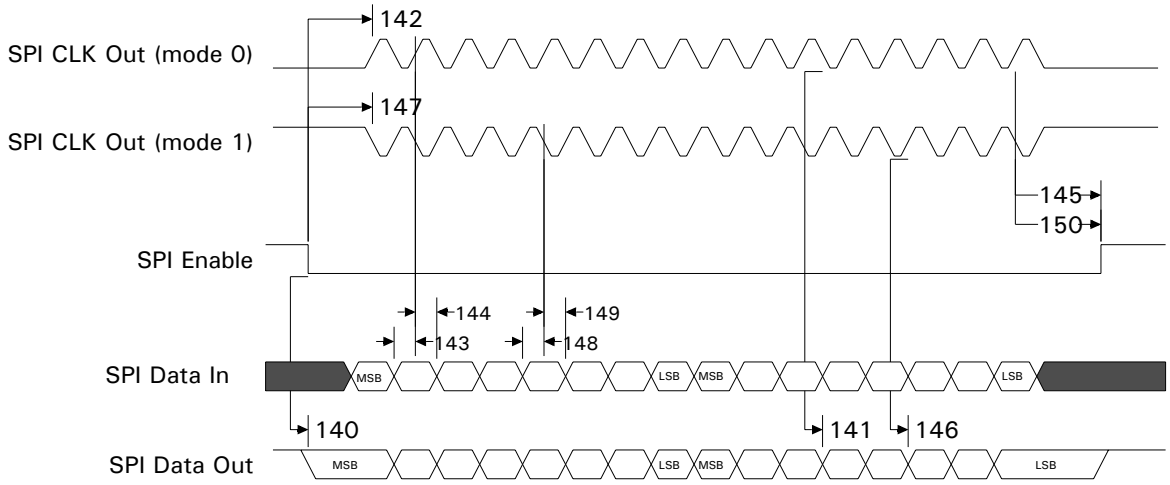
3 If CAS latency = 3, there are:

- Two NOPs between the Read and Burst Terminate commands
- Three Inhibit commands after the Burst Terminate command

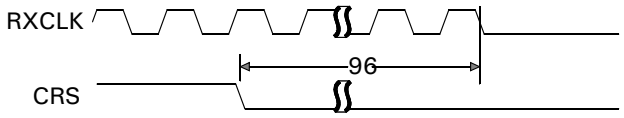
SPI Slave Mode 0 and 1 (Two-Byte Transfer)

Number	Characteristic	Min.	Max.
141	Mode 0 SPI Clock high to TXD valid	3 * T_{SYS}	4 * T_{SYS}
142	Mode 0 SPI Enable low to SPI Clock high (setup)	0	
143	Mode 0 RXD Input valid to SPI Clock high (setup)	3.4	
144	Mode 0 SPI Clock high to RXD input change (hold)	4 * T_{SYS}	
145	Mode 0 SPI Clock high to SPI Enable high (hold)	4 * T_{SYS}	
146	Mode 1 SPI Clock low to TXD valid	3 * T_{SYS}	4 * T_{SYS}
147	Mode 1 SPI Enable low to SPI Clock low (setup)	0	
148	Mode 1 RXD Input valid to SPI Clock low (setup)	3.4	
149	Mode 1 SPI Clock low to RXD input change (hold)	4 * T_{SYS}	
150	Mode 1 SPI Clock low to SPI Enable high (hold)	4 * T_{SYS}	

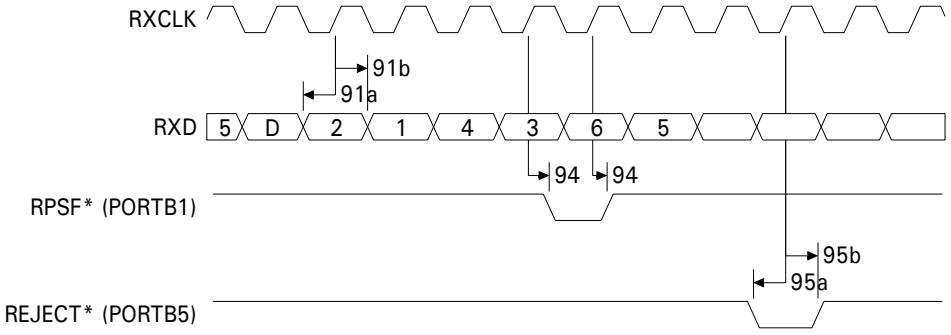
Minimum and maximum are in nanoseconds (ns).



Ethernet Receive Clock Idle



External Ethernet CAM Filtering



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