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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

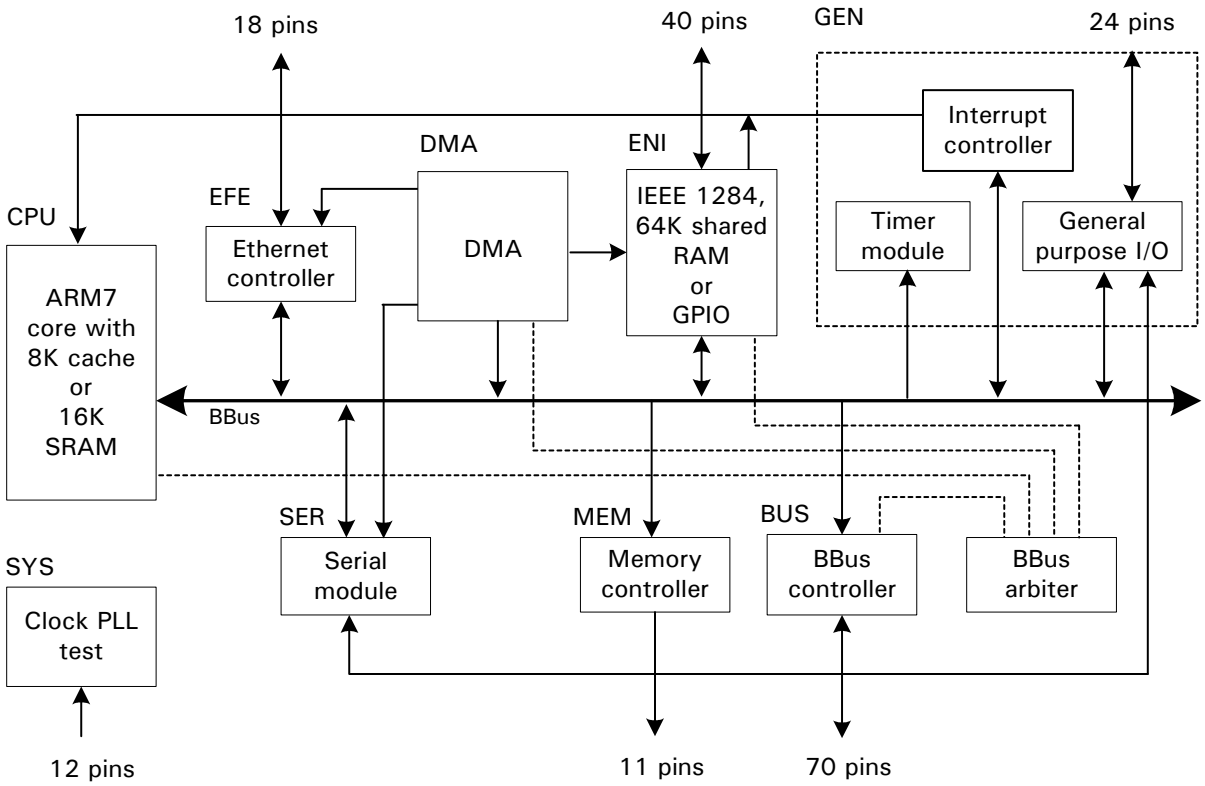
Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Network Processor
Core Processor	ARM7®
Program Memory Type	External Program Memory
Controller Series	NET+50
RAM Size	16K x 8
Interface	EBI/EMI, Ethernet, DMA, HDLC, IEEE1284/ENI, SPI, UART
Number of I/O	40
Voltage - Supply	2.25V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/digi-international/net-50-qit-3

Contents

NET+50 block diagram

The following diagram provides an overview of the modules that make up the NET+50 device:



Key features

CPU core

- Full 32-bit ARM7TDMI RISC processor
- 32-bit internal bus
- 16-bit Thumb mode
- 8 KB cache, configurable as 16 KB RAM
- 15 general-purpose 32-bit registers
- 32-bit program counter and status register
- Five supervisor modes, one user mode

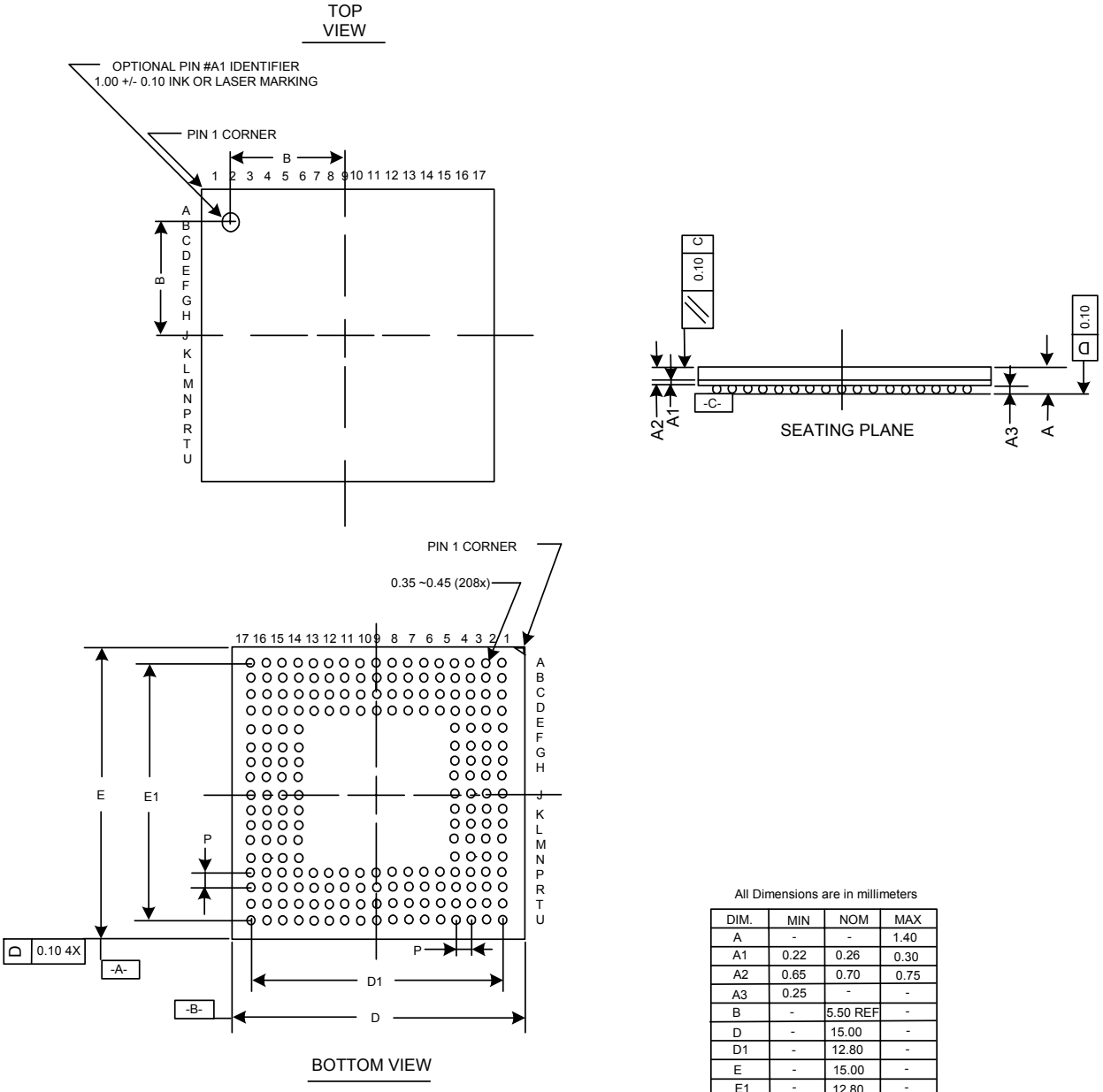
Integrated 10/100 Ethernet MAC

- 10/100 MII-based PHY interface
- 10 Mbit ENDEC interface
- Supports TP-PMD and fiber-PMD devices
- Full-duplex and half-duplex modes
- Optional 4B/5B coding
- Full statistics gathering (SNMP and RMON)
- Station, broadcast, and multicast address detection and filtering
- 128-byte transmit FIFO, 2 KB receive FIFO
- Intelligent receive-side buffer selection

Packaging dimensions and pinout

The NET+50 is available in two package options — a ball-grid array (BGA) or a plastic quad flat pack (PQFP).

BGA packaging and pinout diagram



All Dimensions are in millimeters

DIM.	MIN	NOM	MAX
A	-	-	1.40
A1	0.22	0.26	0.30
A2	0.65	0.70	0.75
A3	0.25	-	-
B	-	5.50 REF	-
D	-	15.00	-
D1	-	12.80	-
E	-	15.00	-
E1	-	12.80	-
P	-	0.80	-

Pinout detail tables

The pinout tables in the following sections have the following columns:

Signal	The pin name for each I/O signal.Some signals have dual modes and are identified accordingly. The mode is configured through firmware using a configuration register. Some modes may require hardware configuration during a RESET condition
BGA	The BGA pin number for specific I/O signals.
PQFP	The PQFP pin number for specific I/O signals.
†	A dagger indicates a pin that is an input current source. (The daggers appear in the BGA column, but this applies in PQFP layout as well.)
*	An asterisk indicates a pin that is *active low*.
I/O	The type of signal — input, output, or input/output (I/O).
OD	The output drive strength of an output buffer. The NET+50 uses one of three drivers: ■ 2 mA ■ 4 mA ■ 8 mA

System bus interface

Signal		BGA	PQFP	I/O	OD	Description	
BCLK		T10	187	O	8	Synchronous bus clock	
ADDR27	CS0OE*	F4 †	117	I/O	4	Address bus	Chip select 0 output enable
ADDR26	CS0WE*	F3 †	116	I/O	4	Address bus	Chip select 0 write enable
ADDR25	BLAST*	E2 †	115	I/O	4	Address bus	Burst-terminated input
ADDR24		D2 †	114	I/O	4		
ADDR23		E3 †	113	I/O	4		
ADDR22		E4 †	112	I/O	4		
ADDR21		D1 †	111	I/O	4		
ADDR20		C2 †	110	I/O	4		
ADDR19		D3 †	109	I/O	4		
ADDR18		C1 †	108	I/O	4		
ADDR17		B1 †	107	I/O	4		
ADDR16		B2 †	106	I/O	4		
ADDR15		B3 †	103	I/O	4		
ADDR14		A3 †	102	I/O	4		
ADDR13		A4 †	101	I/O	4		
ADDR12		B4 †	100	I/O	4		

Chip select controller

Signal		BGA	PQFP	I/O	OD	Description	
CS0*		T11	191	O	4	Chip select (boot select)	
CS1*	RAS1*	R12	192	O	4	Chip select	DRAM RAS*
CS2*	RAS2*	P12	193	O	4	Chip select	DRAM RAS*
CS3*	RAS3*	U11	194	O	4	Chip select	DRAM RAS*
CS4*	RAS4*	T12	195	O	4	Chip select	DRAM RAS*
CAS3*	SDRAS*	T13	199	O	4	DRAM column strobe D31:24	SDRAM RAS*
CAS2*	SDCAS*	U12	198	O	4	DRAM column strobe D23:16	SDRAM CAS*
CAS1*	SDWE*	P13	197	O	4	DRAM column strobe D15:08	SDRAM WE*
CAS0*	SD(AP)	R13	196	O	4	DRAM column strobe D07:00	SDRAM (AP)
WE*		R11	190	O	4	Write enable	
OE*		P11	189	O	4	Output enable	

Ethernet interface

MII	10BaseT	BGA	PQFP	I/O	OD	MII	10BaseT
MDC	LB*	D7	85	O	2	MII clock	Loopback enable
MDIO	UTPSTP*	C7 †	84	I/O	2	MII data	Cable type
TXCLK	TXCLK	B8	83	I		TX clock	
TXD0	TXD	A9	82	O	2	TX data 0	TX data
TXD1	PDN* (OD)	D8	81	O	2	TX data 1	Power down
TXD2	NTHRES	C8	80	O	2	TX data 2	Normal threshold
TXD3	THIN	D9	77	O	2	TX data 3	Enable Thinnet
TXER	LTE	C9	76	O	2	TX code error	Link test enable
TXEN	TXEN	B10	75	O	2	TX enable	
COL	TXCOL	A11	74	I		Collision	
CRS	RXCRS	D10	73	I		Carrier sense	
RXCLK	RXCLK	C10	72	I		RX clock	
RXD0	RXD	B11	71	I		RX data 0	RX data
RXD1	MANSENSE	A12	70	I		RX data 1	Sense jumper
RXD2	JABBER	D11	69	I		RX data 2	Jabber
RXD3	REVPOL	C11	68	I		RX data 3	Reverse polarity
RXER	LINKPUL*	B12	67	I		RX error	Link pulse detection
RXDV	AUTOMAN	A13	66	I		RX data valid	10B2 selected

ENI/Parallel 1284 Interface (cont.)

IEEE1284	ENI	GPIO	BGA	PFQP	I/O	OD	Description
PSELECT1	PA12	GPIG4	J14	25	I		
PSELECT2	PA13	GPIOF3	H15	28	I/O	2	Or ENI DMA output PDRQI*
PSELECT3	PA14	GPIOF2	H14	29	I/O	2	Or ENI DMA output PDRQO*
PSELECT4	PA15	GPIG5	J17	30	I		Or ENI DMA input PDACK*
FAULT1*	PA16	GPIG6	H16	31	I		
FAULT2*	PCS*	GPIG7	H17	34	I		
FAULT3*	PRW*	GPIOF0	G14	33	I/O	2	
FAULT4*	PBRW*	GPIOF1	G15	32	I/O	2	

Clock generation

Signal	BGA	PQFP	I/O	OD	Description
XTAL1	U7	178	I		2.5 V crystal oscillator circuit
XTAL2	T8	179	O		
PLLVDD	U8	182			2.5 V PLL clean power
PLLLPF	P9	181			PLL loop filter capacitor
PLLVSS	R9	180			PLL clean ground
PLLTST*	P8 †	177	I		2.5 V PLL test mode
BISTEN*	R10 †	184	I		Enable internal BIST operation
SCANEN*	P10 †	185	I		Enable internal SCAN testing

System reset

Signal	BGA	PQFP	I/O	OD	Description
RESET*	T2 †	158	I		System reset *

Debug support for ARM core

Signal	BGA	PQFP	I/O	OD	Description
TDI	T6 †	171	I		Test data in
TDO	U5	170	O	2	Test data out
TMS	R7 †	172	I		Test mode select
TRST*	R8	174	I		Test mode reset (input current sink)
TCK	P7	173	I		Test mode clock

Power supply

Signal	BGA	PQFP	Description
V_{CC} DC 3.3 V DC	F15, B17, C12, A2, M2, U9	36, 52, 64, 104, 143, 186	I/O steady state (6 pairs)
V_{SS} DC Gnd Returns	F14, A17, D12, A1, N3, U10	37, 53, 65, 105, 144, 188	
V_{CC} AC 3.3 V	A8, E1, T1, U16	86, 118, 156, 208	I/O switching (4 pairs — see note below on 3.3 V power and GND pads)
V_{SS} AC Gnd Return	B7, F2, U1, U17	87, 119, 157, 1	
V_{DD} CO 2.5 V	K17, A10, H1, T7	26, 78, 130, 175	Core power (4 pairs)
V_{SS} CO Gnd Returns	J16, B9, J2, U6	27, 79, 131, 176	
PLL V_{DD} 2.5 V	U8	182	PLL bead filtered clean power
PLL V_{SS} Gnd Return	R9	180	Power-up reset ground reference
POR V_{SS} Gnd	T9	183	

Additional information about NET+50 pins

- All outputs drive TTL levels. Outputs drive to 0.4 V maximum on low, 2.4 V minimum on high.
- The following pins require a 2.5 V input level:

Signal	BGA	PQFP
XTAL1	U7	178
PLLTST	P8	177
PLLVDD	U8	182

- TRST* (R8, 174) is the only pin that is an input current sink.
- Remaining inputs are TTL levels and are 3.3 V tolerant, allowing integration with 3.3 V devices.
- Regarding 3.3 V power and GND pads: In general, you should use separate power pairs for AC and DC power to prevent the noise in the AC power buses from reaching the DC power buses. Digi recommends (and uses) a ferrite bead to filter the AC power pins.

Registers and addresses

General control module

Address	Register	Address	Register
0xFFB0 0000	System control register	0xFFB0 0024	Port B register
0xFFB0 0004	System status register	0xFFB0 0028	Port C register
0xFFB0 0008	PLL control register	0xFFB0 0030	Interrupt enable register
0xFFB0 000C	Software service register	0xFFB0 0034	Interrupt enable register — Set
0xFFB0 0010	Timer 1 control register	0xFFB0 0038	Interrupt enable register — Clear
0xFFB0 0014	Timer 1 status register	0xFFB0 0034	Interrupt status register — Enabled
0xFFB0 0018	Timer 2 control register	0xFFB0 0038	Interrupt status register — Raw
0xFFB0 001C	Timer 2 status register	0xFFB0 0040	Cache control register 0
0xFFB0 0020	Port A register	0xFFB0 0044	Cache control register 1

Memory module controller

Address	Register	Address	Register
0xFFC0 0000	Memory module configuration register (MMCR)	0xFFC0 0034	Chip select 2 option register (OR2)
0xFFC0 0010	Chip select 0 base address register (BAR0)	0xFFC0 0038	Chip select 2 option register B (OR2B)
0xFFC0 0014	Chip select 0 option register (OR0)	0xFFC0 0040	Chip select 3 base address register (BAR3)
0xFFC0 0018	Chip select 0 option register B (OR0B)	0xFFC0 0044	Chip select 3 option register (OR3)
0xFFC0 0020	Chip select 1 base address register (BAR1)	0xFFC0 0048	Chip select 3 option register B (OR3B)
0xFFC0 0024	Chip select 1 option register (OR1)	0xFFC0 0050	Chip select 4 base address register (BAR4)
0xFFC0 0028	Chip select 1 option register B (OR1B)	0xFFC0 0054	Chip select 4 option register (OR4)
0xFFC0 0030	Chip select 2 base address register (BAR2)	0xFFC0 0058	Chip select 4 option register B (OR4B)

DMA controller module

DMA register key: 0xFF90*nnnn* where *nnnn* = DMAx + Offset							
DMA*x*:						**Offset:**	
1A:	00	2:	80	6:	100	00	Buffer descriptor pointer
1B:	20	3:	A0	7:	120	10	Buffer control register
1C:	40	4:	C0	8:	140	14	Buffer status register
1D:	60	5:	E0	9:	160		
				10:	180		

Examples:	
0xFF90 0000	DMA 1A buffer descriptor pointer
0xFF90 0010	DMA 1A buffer control register
0xFF90 0014	DMA 1A buffer status register

Ethernet controller module

Address	Register	Address	Register
0xFF80 0000	General control register	0xFF80 0440 – 0478	Transmit control registers
0xFF80 0004	General status register	0xFF80 0480 – 0488	Receive control registers
0xFF80 0008	FIFO data register	0xFF80 040C0	Link fail counter
0xFF80 000C	FIFO last word data register	0xFFB0 0500	10 Mbit jabber counter
0xFF80 0010	TX status register	0xFFB0 0504	10 Mbit loss of carrier counter
0xFF80 0014	RX status register	0xFFB0 0540 – 0550	MII control registers
0xFF80 0400 – 0404	MAC configuration and test registers	0xFFB0 0580 – 059C	Status registers
0xFF80 0408 – 040C	PCS configuration and test registers	0xFFB0 05C0	SAL address filter register
0xFF80 0410 – 0414	STL configuration and test registers	0xFFB0 05C4 – 05DC	SAL hash table registers

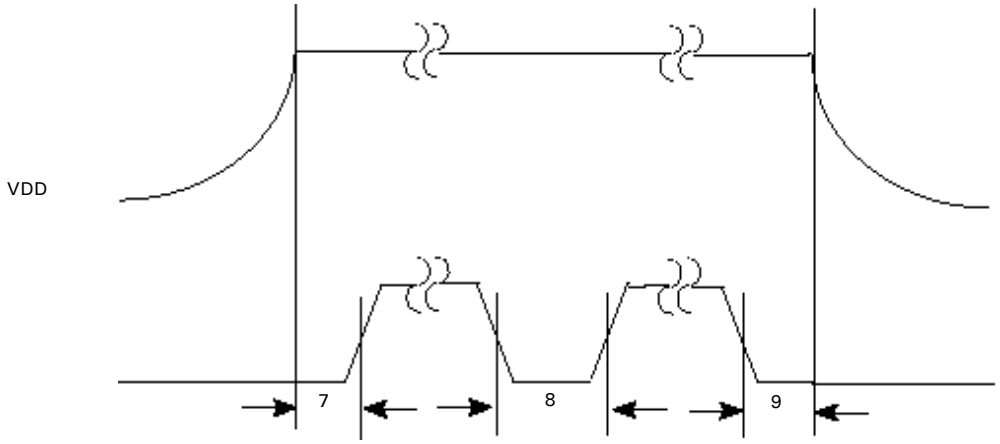
Serial controller module

Address	Register	Address	Register
0xFFD0 0000 – 0030	Channel 1 registers	0xFFD0 0040 – 0070	Channel 2 registers

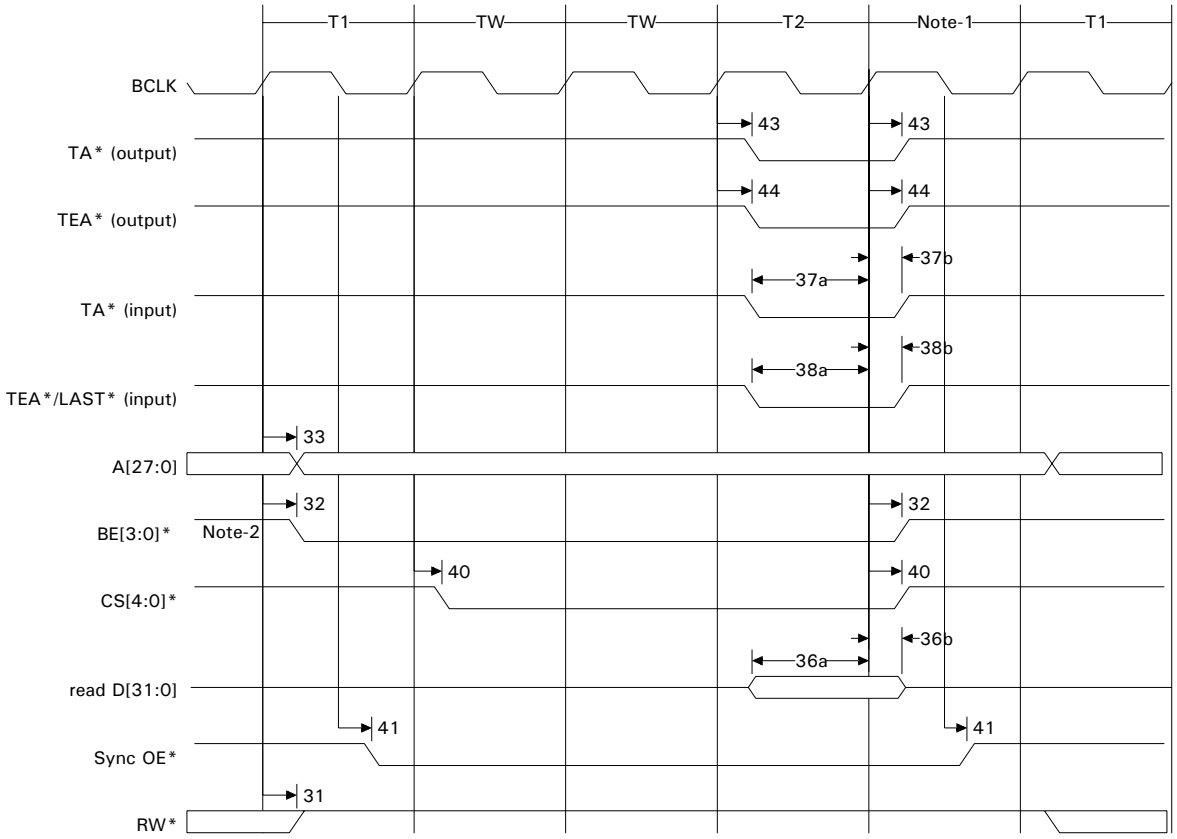
Timing data and diagrams

Reset timing

Number	Characteristic	Min.	Max.	Unit
7	V_{DD} at 3.0 V to RESET* high	40		ms
8	RESET* pulse width low	$10/F_{SYSCLK}$		µs
9	RESET* low to V_{DD} below 3.0 V	$8/F_{SYSCLK}$		µs



SRAM Sync Read (Wait = 2)



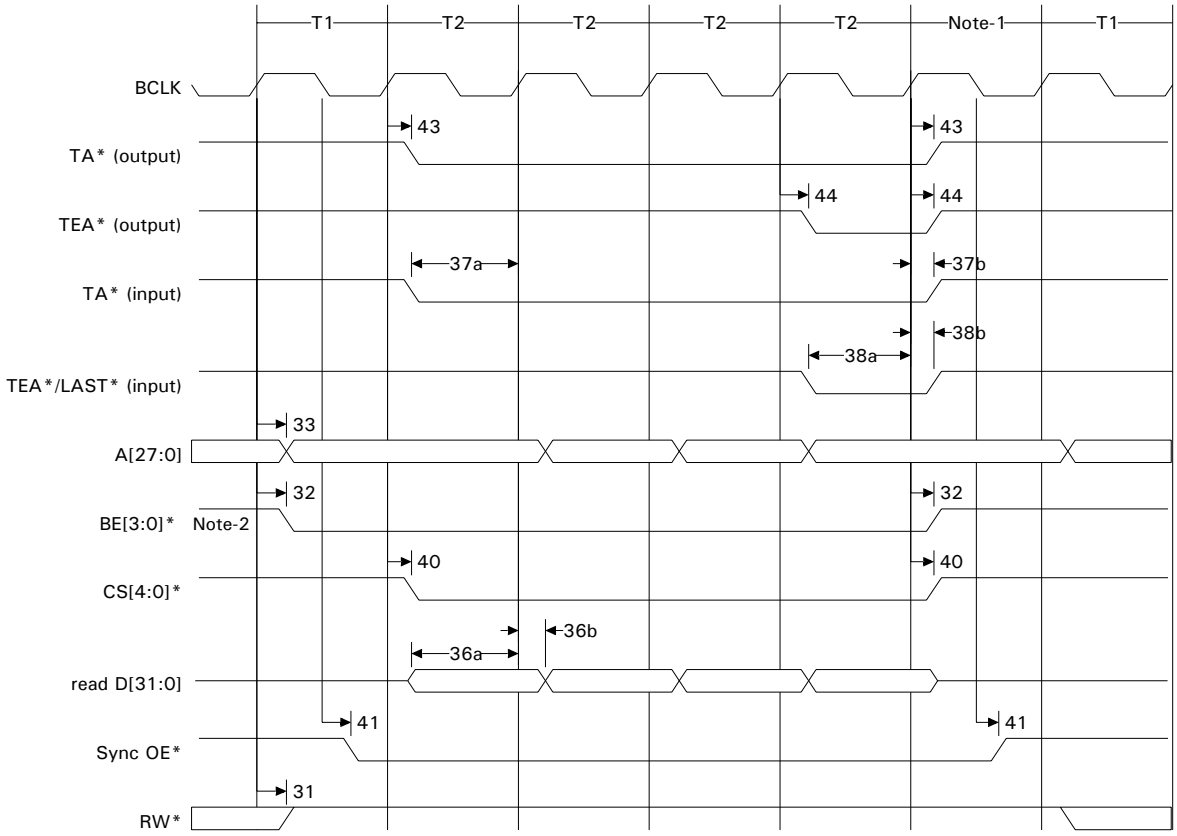
Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

SRAM Sync Burst Read (2-111, Wait = 0, BCYC = 00)



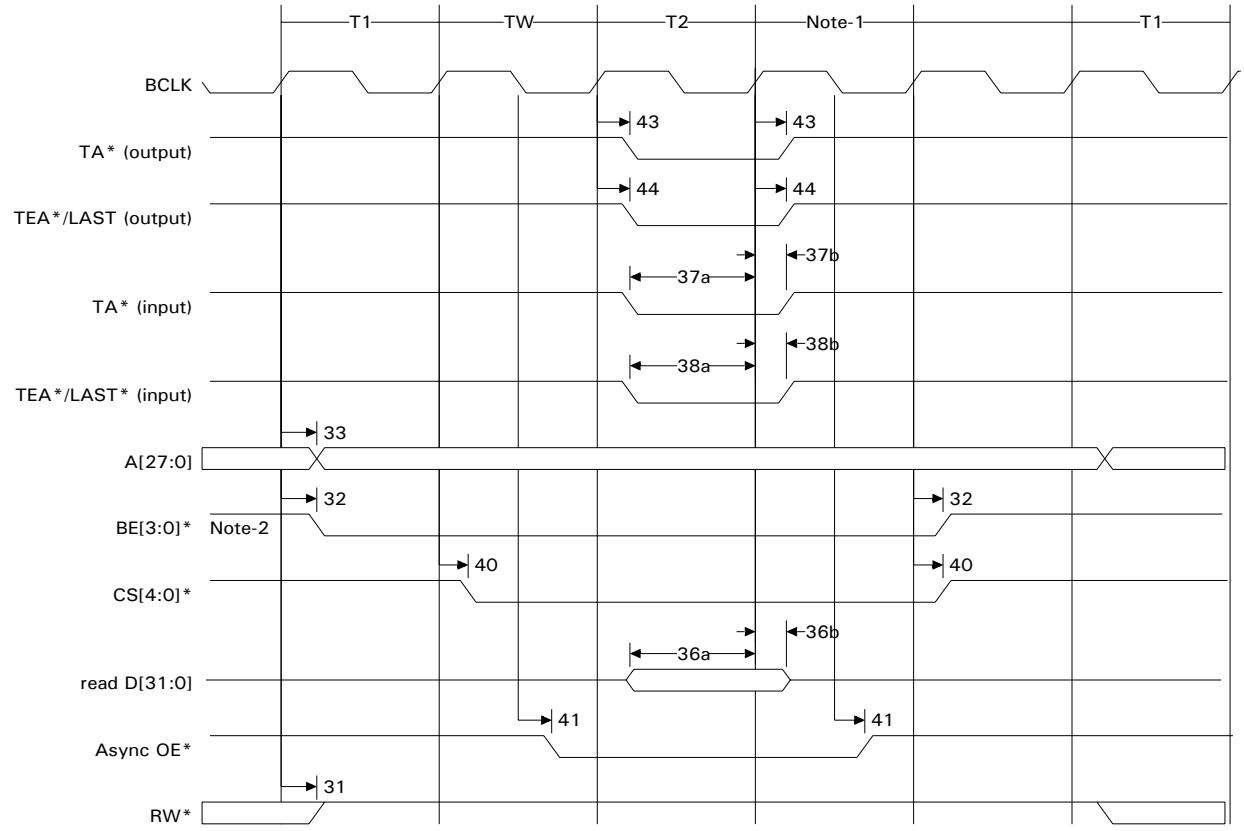
Notes:

1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

SRAM Async Read (Wait = 2)



Notes:

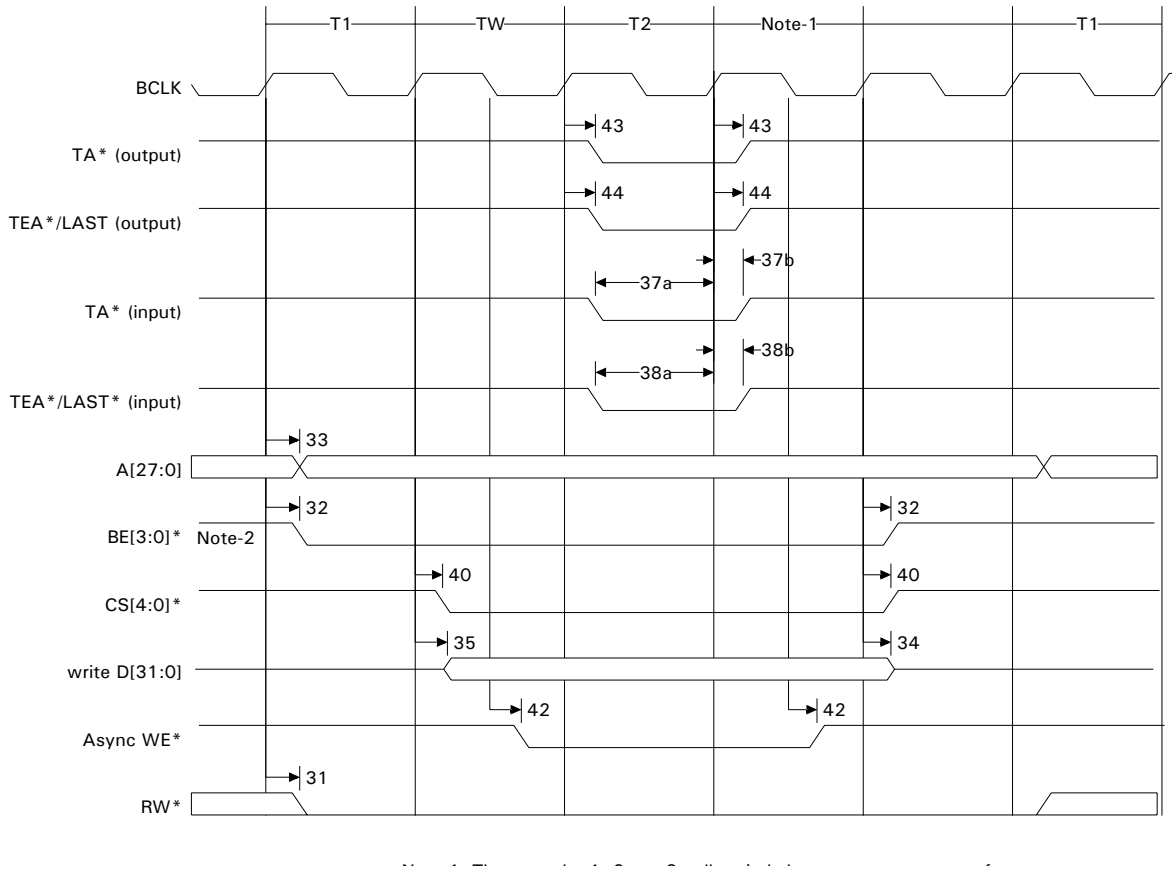
1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 The TW cycles are present when the WAIT field is set to 2 or more.

SRAM Async Write (Wait = 2)



Notes:

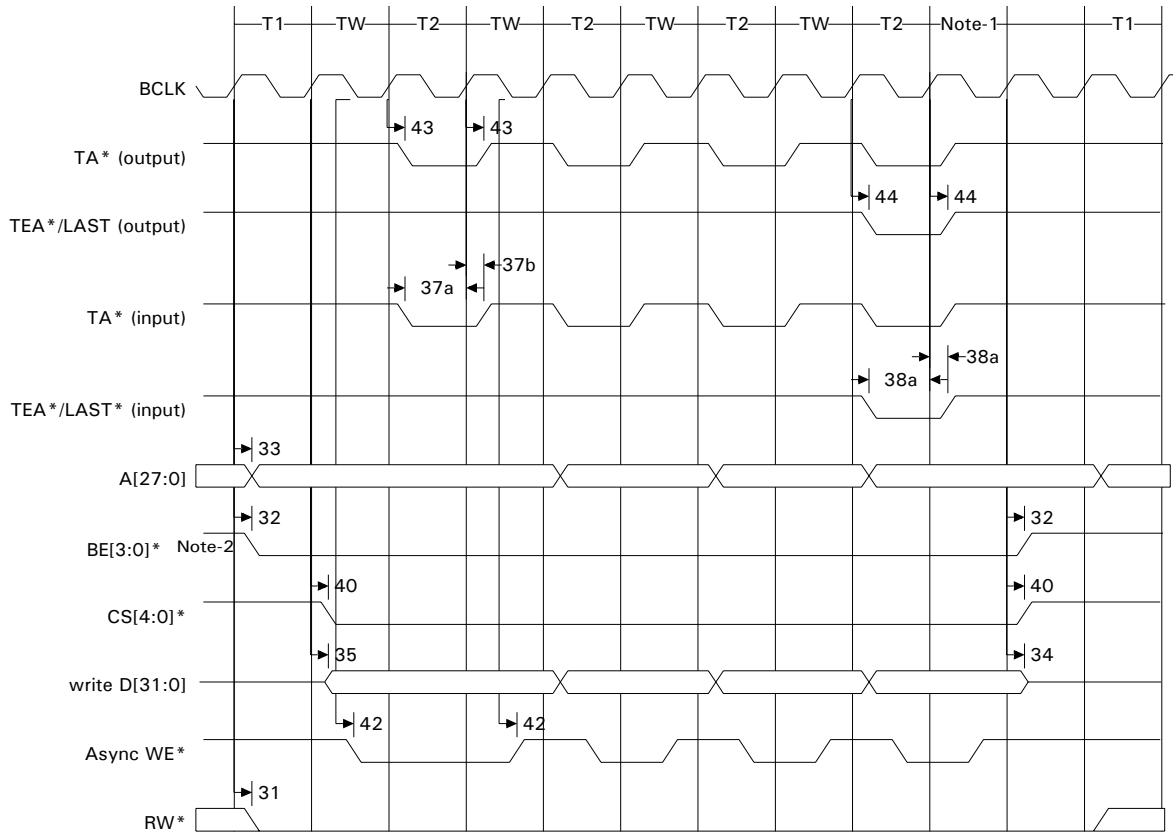
1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 The TW cycles are present when the WAIT field is set to 2 or more.

SRAM Async Burst Write (Wait = 2, BCYC = 01)



Notes:

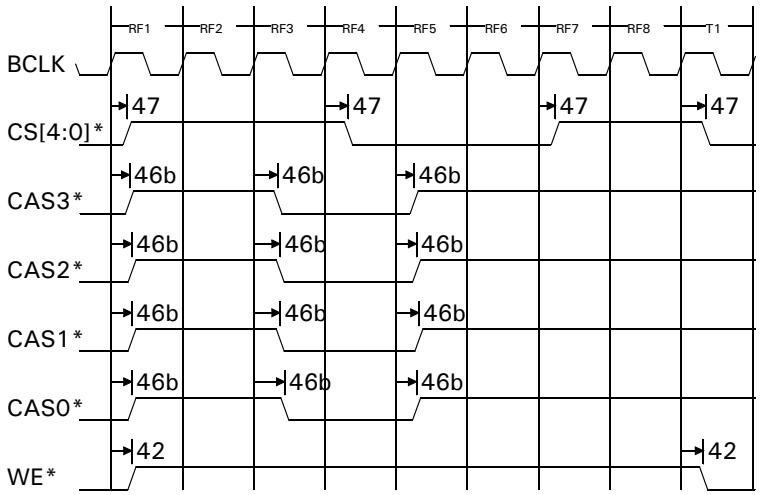
1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.

2 Port size determines which byte enable signals are active:

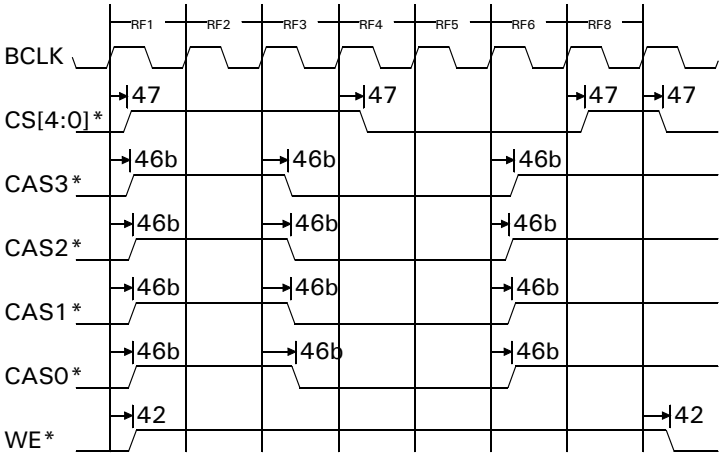
8-bit port = BE3*
16-bit port = BE[3:2]*
32-bit port = BE[3:0]*

3 The TW cycles are present when the WAIT field is set to 2 or more.

Fast Page and EDO DRAM Refresh (RCYC = 0)



Fast Page and EDO DRAM Refresh (RCYC = 1)



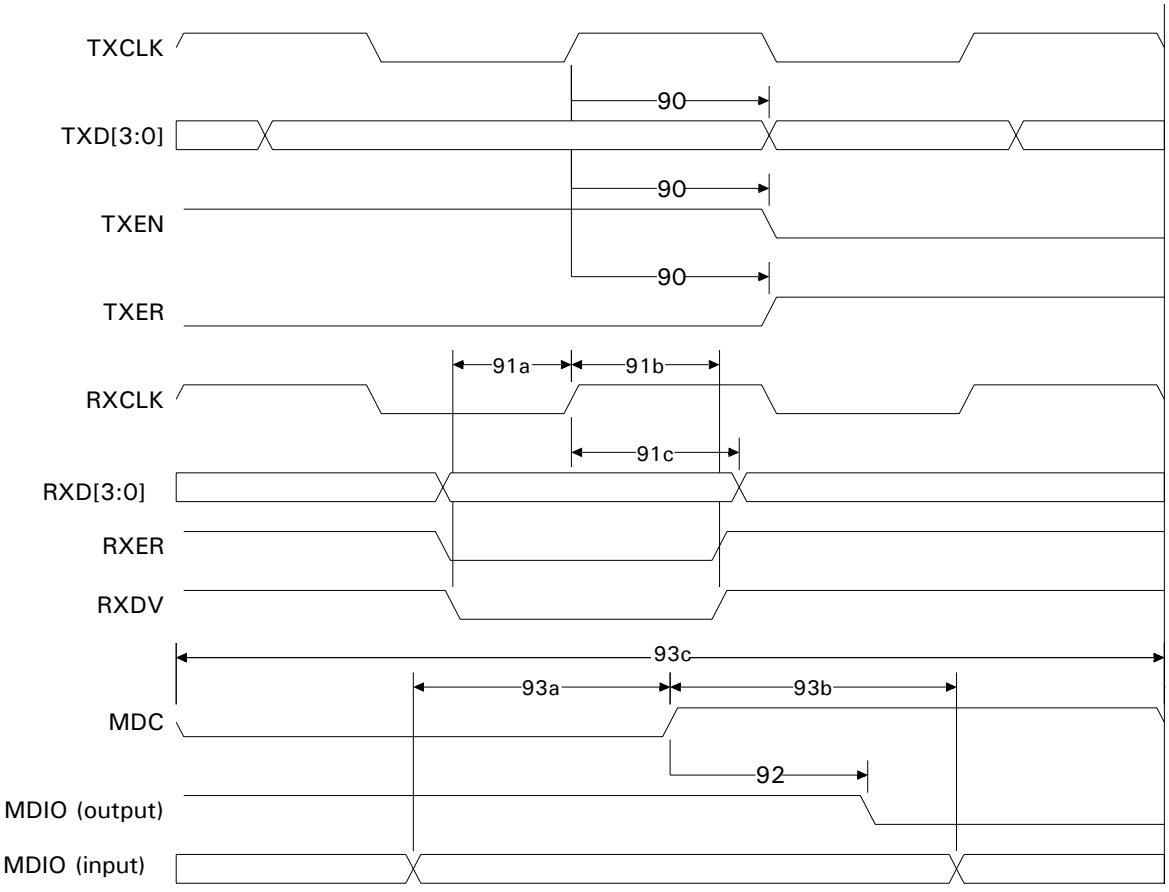
SDRAM timing

Number	Characteristic	Min.	Max.
31	BCLK high to RW* valid		19
32	BCLK high to BE* valid		16
33	BCLK high to Address valid	4	15
34	BCLK high to Data Out high impedance		17
35	BCLK high to Data Out valid		18
36a	Data In valid to BCLK high (setup)	8	
36b	BCLK high to Data In invalid (hold)	0	
37a	TA* valid to BCLK high (setup)	8	
37b	BCLK high to TA* invalid (hold)	0	
38a	TEA* valid to BCLK high (setup)	8.5	
38b	BCLK high to TEA* invalid (hold)	0	
40	BCLK high to CS* valid		16
41	BCLK low to OE* valid		14
42	BCLK low to WE* valid		16
43	BCLK high to TA* valid		11
44	BCLK high to TEA* valid		14

Minimum and maximum are in nanoseconds (ns).

Ethernet timing

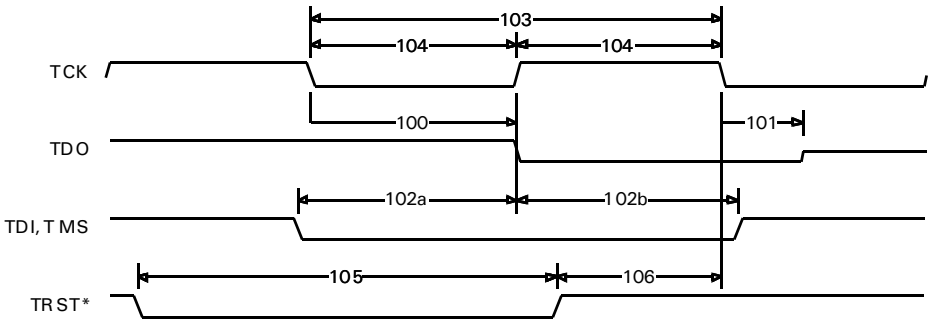
Number	Characteristic	Min.	Max.	Unit
90	TXCLK high to TXD, TXEN, TXER valid	5	17	ns
91a	RXD, RXER, RXDV valid to RXCLK high (setup)	8		ns
91b	RXCLK high to RXD, RXER, RXDV hold time	0		ns
91c	RXCLK high to RXD hold time	0		ns
92	MDC high to MDIO change	40	50	ns
93a	MDIO valid to MDC high (setup)	10		ns
93b	MDC high to MDIO hold time	0		ns
93c	MDC cycle time		SYSCLK/10	
94	RXCLK high to RPSF* change		6.5	ns
95a	REJECT* valid to RXCLK high (setup)	2.6		ns
95b	REJECT* valid from RXCLK high (hold)	0		ns
96	CRS low to RXCLK idle	27		Bit-Time



ARM core debug timing

Number	Characteristic	Min.	Max.
100	TCK low to TDO valid	0	33.5
101	TCK low to TDO high impedance	0	32.3
102a	TDI, TMS valid to TCK high (setup)	0.72	
102b	TCK high to TDI, TMS hold time	1.3	
103	TCK cycle time	31.2	
104	TCK pulse width	15.6	
105	TRST* low time	27	
	Minimum and maximum are in nanoseconds (ns).		

Note: TRST* has an internal current sink. On production units, do not leave TRST* pulled low. The noise margin on inputs at a logic 0 is only a few tenths of a volt. Digi recommends tying TRST* to RESET* on production units.



ENI Dual Direction DMA timing