Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	16MHz
Connectivity	I²C, IEBus, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	5K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 18x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30302fapfp-u5

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SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

REJ03B0088-0122
Rev.1.22
Mar 30, 2007

1. Overview

The M16C/30P Group of single-chip microcomputers is built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and is packaged in a 100-pin plastic molded QFP.

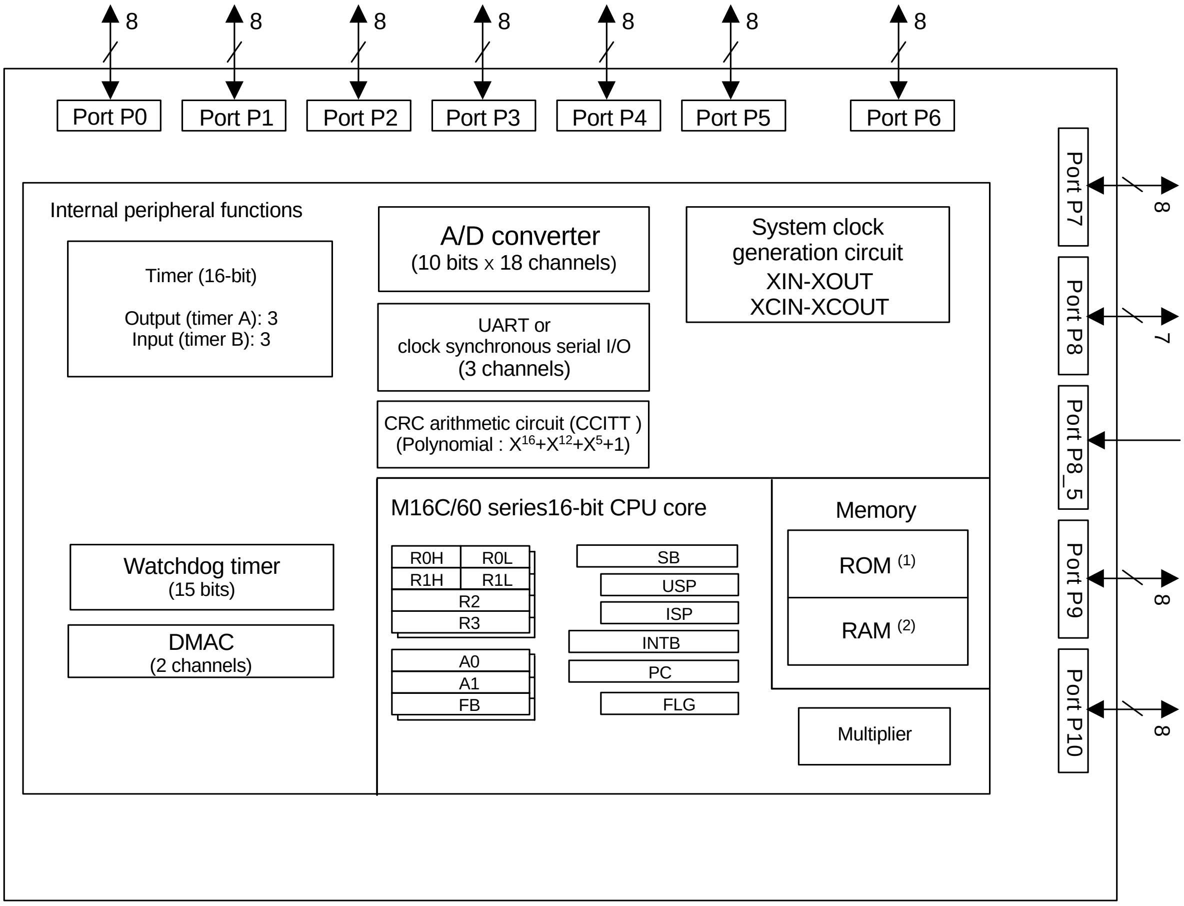
These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed. In addition, these microcomputers contain a multiplier and DMAC which combined with fast instruction processing capability, make it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/ logic operations.

1.1 Applications

Audio, cameras, TV, home appliance, office/communications/portable/industrial equipment, etc.

1.3 Block Diagram

Figure 1.1 is a M16C/30P Group Block Diagram.



NOTES :
1. ROM size depends on microcomputer type.
2. RAM size depends on microcomputer type.

Figure 1.1 M16C/30P Group Block Diagram

1.4 Product List

Table 1.2 lists the M16C/30P group products and Figure 1.2 shows the Part No., Memory Size, and Package. Table 1.4 lists Product Code of MASK ROM version for M16C/30P. Figure 1.3 shows the Marking Diagram of Mask ROM Version for M16C/30P (Top View). Table 1.5 lists Product Code of One Time Flash version, Flash Memory version, and ROM-less version for M16C/30P. Figure 1.4 shows the Marking Diagram of One Time Flash version, Flash Memory version, and ROM-less Version for M16C/30P (Top View). Please specify the marking for M16C30P (MASK ROM version) when placing an order for ROM.

Table 1.2 Product List (1) **As of March 2007**

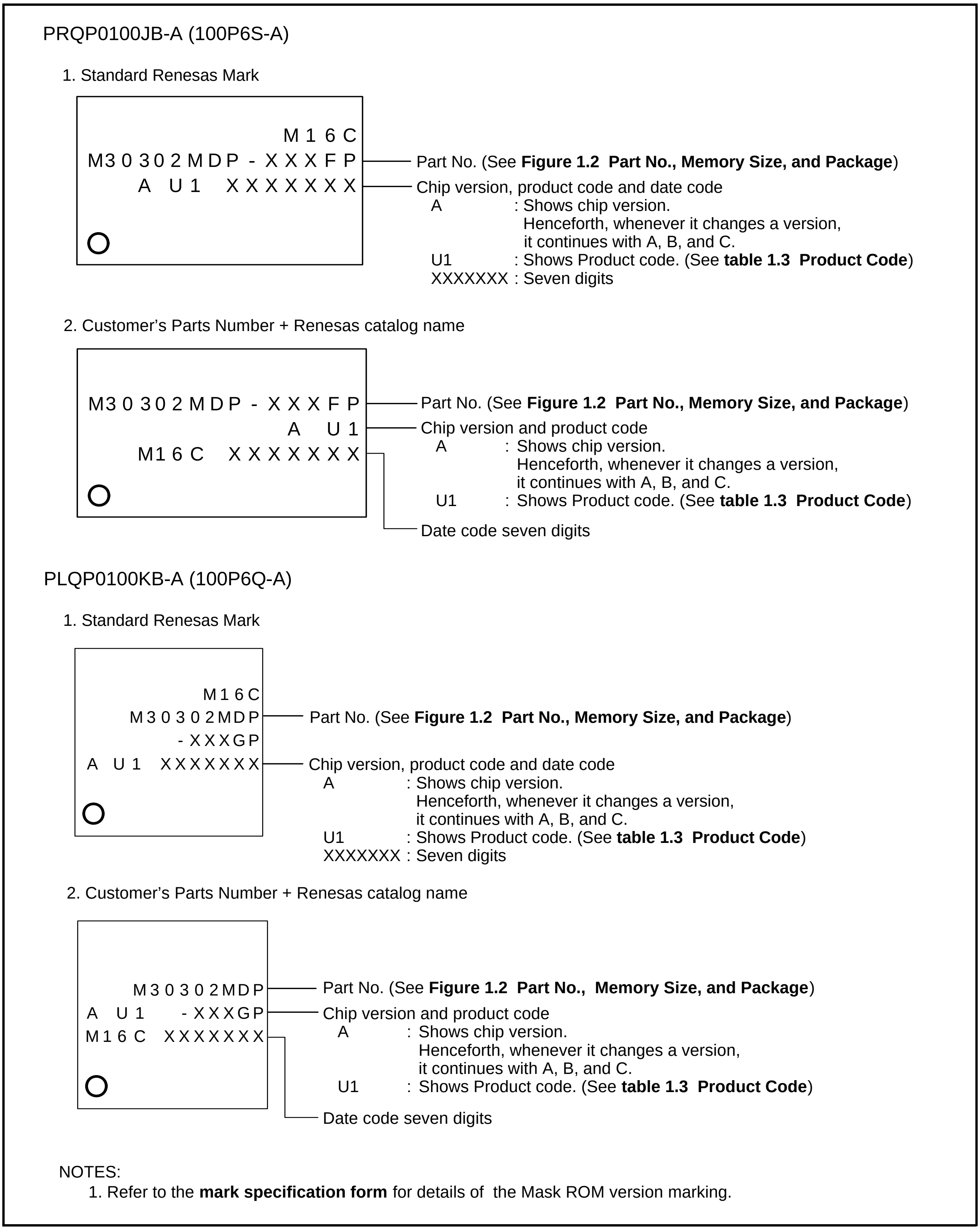
Part No.	ROM Capacity	RAM Capacity	package code (1)	Remarks
M30302MAP-XXXFP	96 Kbytes	5 Kbytes	PRQP0100JB-A	Mask ROM version
M30302MAP-XXXGP			PLQP0100KB-A	
M30302MCP-XXXFP	128 Kbytes		PRQP0100JB-A	
M30302MCP-XXXGP			PLQP0100KB-A	
M30302MDP-XXXFP	160 Kbytes	6 Kbytes	PRQP0100JB-A	
M30302MDP-XXXGP			PLQP0100KB-A	
M30302MEP-XXXFP	192 Kbytes		PRQP0100JB-A	
M30302MEP-XXXGP			PLQP0100KB-A	
M30302GAPFP	96 Kbytes	5 Kbytes	PRQP0100JB-A	One Time Flash version (blank product)
M30302GAPGP (D)			PLQP0100KB-A	
M30302GCPFP	128 Kbytes		PRQP0100JB-A	
M30302GCPGP (D)			PLQP0100KB-A	
M30302GDPFP	160 Kbytes	6 Kbytes	PRQP0100JB-A	
M30302GDPGP (D)			PLQP0100KB-A	
M30304GDPFP (D)		12 Kbytes	PRQP0100JB-A	
M30304GDPGP (D)			PLQP0100KB-A	
M30302GEPFP	192 Kbytes	6 Kbytes	PRQP0100JB-A	
M30302GEPGP (D)			PLQP0100KB-A	
M30304GEPFP (D)		12 Kbytes	PRQP0100JB-A	
M30304GEPGP (D)			PLQP0100KB-A	
M30302GGPFP (D)	256 Kbytes	12 Kbytes	PRQP0100JB-A	
M30302GGPGP (D)			PLQP0100KB-A	
M30302GAP-XXXFP	96 Kbytes	5 Kbytes	PRQP0100JB-A	One Time Flash version (factory programmed product)
M30302GAPvGP (D)			PLQP0100KB-A	
M30302GCP-XXXFP	128 Kbytes		PRQP0100JB-A	
M30302GCP-XXXGP (D)			PLQP0100KB-A	
M30302GDP-XXXFP	160 Kbytes	6 Kbytes	PRQP0100JB-A	
M30302GDP-XXXGP (D)			PLQP0100KB-A	
M30304GDP-XXXFP (D)		12 Kbytes	PRQP0100JB-A	
M30304GDP-XXXGP (D)			PLQP0100KB-A	
M30302GEP-XXXFP	192 Kbytes	6 Kbytes	PRQP0100JB-A	
M30302GEP-XXXGP (D)			PLQP0100KB-A	
M30304GEP-XXXFP (D)		12 Kbytes	PRQP0100JB-A	
M30304GEP-XXXGP (D)			PLQP0100KB-A	
M30302GGP-XXXFP (D)	256 Kbytes	12 Kbytes	PRQP0100JB-A	
M30302GGP-XXXGP (D)			PLQP0100KB-A	

(D): Under development
(P): Under planning
NOTES:

1. Previous package codes are as follows.
   PRQP0100JB-A : 100P6S-A,
   PLQP0100KB-A : 100P6Q-A
2. Block A (4-Kbytes space) is available in flash memory version.

Table 1.4 Product Code of MASK ROM version for M16C/30P

Product Code	Package	Operating Ambient Temperature
U1	Lead-free	-20°C to 85°C
U4		-40°C to 85°C



PRQP0100JB-A (100P6S-A)

1. Standard Renesas Mark

Part No. (See **Figure 1.2 Part No., Memory Size, and Package**)

Chip version, product code and date code
A : Shows chip version.
Henceforth, whenever it changes a version,
it continues with A, B, and C.
U1 : Shows Product code. (See **table 1.3 Product Code**)
XXXXXXX : Seven digits

2. Customer's Parts Number + Renesas catalog name

Part No. (See **Figure 1.2 Part No., Memory Size, and Package**)

Chip version and product code
A : Shows chip version.
Henceforth, whenever it changes a version,
it continues with A, B, and C.
U1 : Shows Product code. (See **table 1.3 Product Code**)

Date code seven digits

PLQP0100KB-A (100P6Q-A)

1. Standard Renesas Mark

Part No. (See **Figure 1.2 Part No., Memory Size, and Package**)

Chip version, product code and date code
A : Shows chip version.
Henceforth, whenever it changes a version,
it continues with A, B, and C.
U1 : Shows Product code. (See **table 1.3 Product Code**)
XXXXXXX : Seven digits

2. Customer's Parts Number + Renesas catalog name

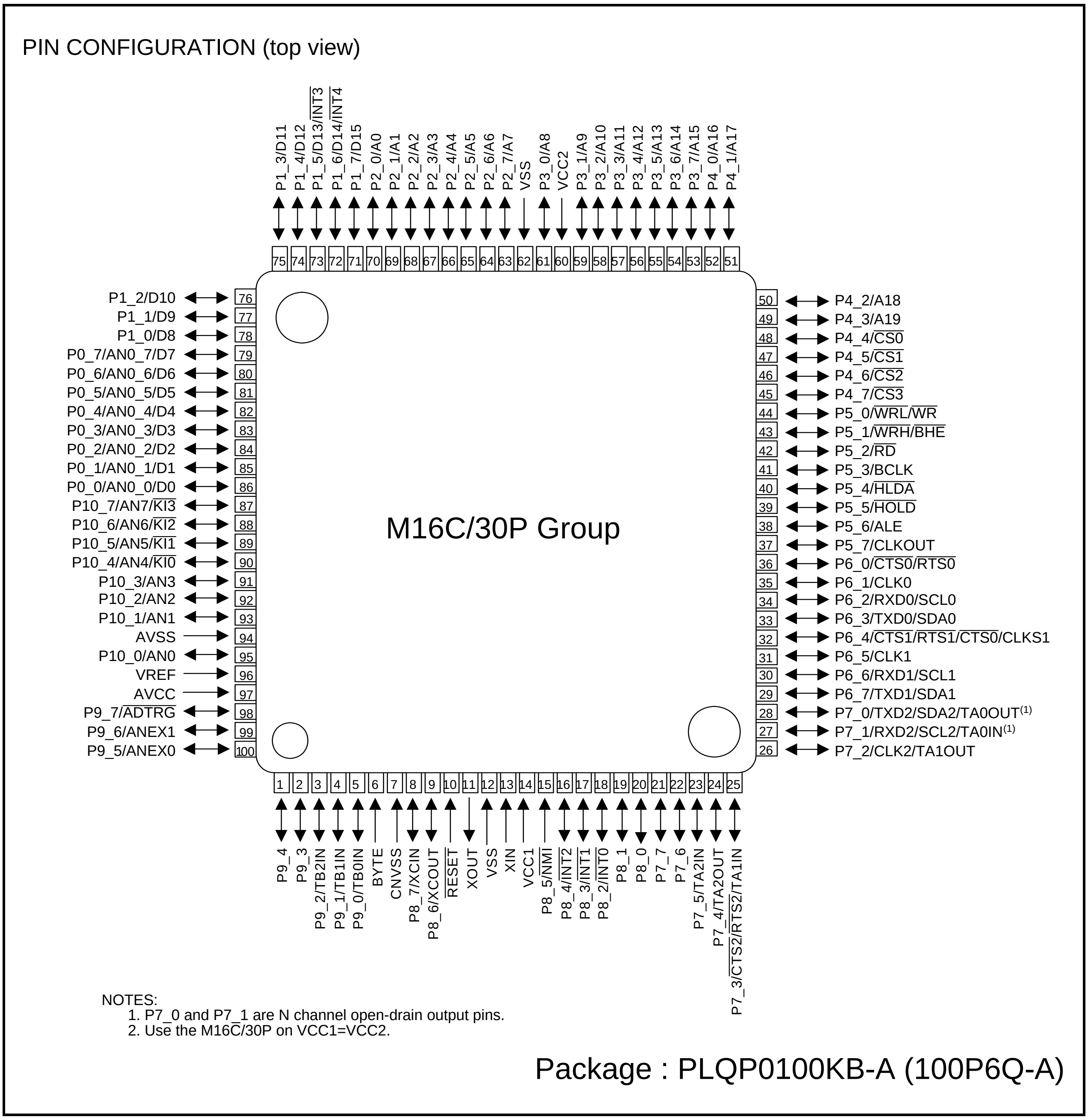
Part No. (See **Figure 1.2 Part No., Memory Size, and Package**)

Chip version and product code
A : Shows chip version.
Henceforth, whenever it changes a version,
it continues with A, B, and C.
U1 : Shows Product code. (See **table 1.3 Product Code**)

Date code seven digits

NOTES:
1. Refer to the **mark specification form** for details of the Mask ROM version marking.

Figure 1.3 Marking Diagram of Mask ROM Version for M16C/30P (Top View)



NOTES:
1. P7_0 and P7_1 are N channel open-drain output pins.
2. Use the M16C/30P on VCC1=VCC2.

Package : PLQP0100KB-A (100P6Q-A)

Figure 1.6 Pin Configuration (Top View)

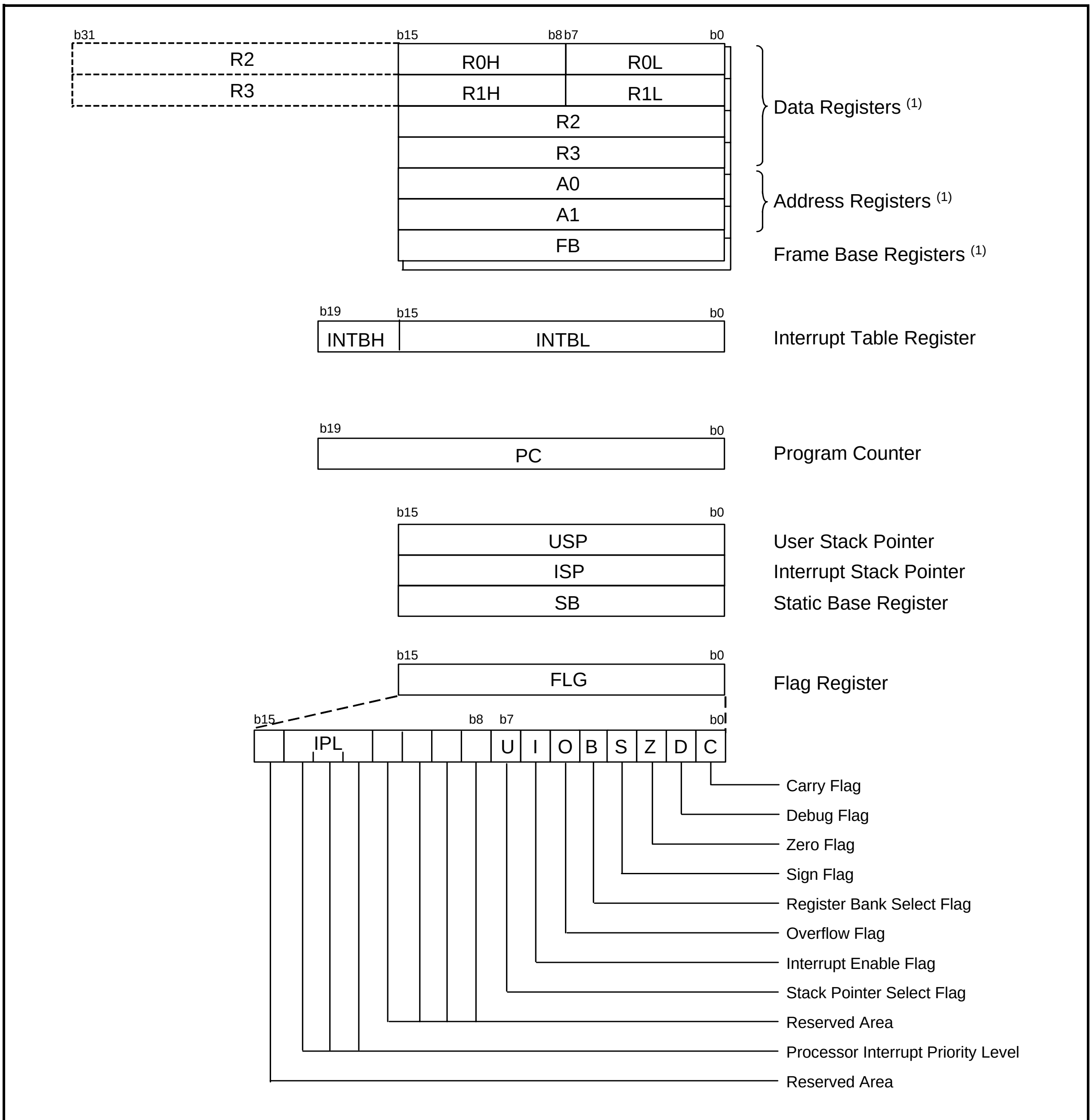
Table 1.9 Pin Description (2)

Signal Name	Pin Name	I/O Type	Description
Main clock input	XIN	I	I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To use the external clock, input the clock from XIN and leave XOUT open.
Main clock output	XOUT	O	
Sub clock input	XCIN	I	I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT. To use the external clock, input the clock from XCIN and leave XCOUT open.
Sub clock output	XCOUT	O	
Clock output	CLKOUT	O	The clock of the same cycle as fC, f8, or f32 is outputted.
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT4}}$	I	Input pins for the $\overline{\text{INT}}$ interrupt.
$\overline{\text{NMI}}$ interrupt input	$\overline{\text{NMI}}$	I	Input pin for the $\overline{\text{NMI}}$ interrupt.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Input pins for the key input interrupt.
Timer A	TA0OUT to TA2OUT	I/O	These are timer A0 to timer A2 I/O pins. (however, the output of TA0OUT for the N-channel open drain output.)
	TA0IN to TA2IN	I	These are timer A0 to timer A2 input pins.
Timer B	TB0IN to TB2IN	I	These are timer B0 to timer B2 input pins.
Serial interface	$\overline{\text{CTS0}}$ to $\overline{\text{CTS2}}$	I	These are send control input pins.
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS2}}$	O	These are receive control output pins.
	CLK0 to CLK2	I/O	These are transfer clock I/O pins.
	RXD0 to RXD2	I	These are serial data input pins.
	TXD0 to TXD2	O	These are serial data output pins. (however, TXD2 for the N-channel open drain output.)
	CLKS1	O	This is output pin for transfer clock output from multiple pins function.
I^2C mode	SDA0 to SDA2	I/O	These are serial data I/O pins. (however, SDA2 for the N-channel open drain output.)
	SCL0 to SCL2	I/O	These are transfer clock I/O pins. (however, SCL2 for the N-channel open drain output.)
Reference voltage input	VREF	I	Applies the reference voltage for the A/D converter.
A/D converter	AN0 to AN7, AN0_0 to AN0_7	I	Analog input pins for the A/D converter.
	$\overline{\text{ADTRG}}$	I	This is an A/D trigger input pin.
	ANEX0	I/O	This is the extended analog input pin for the A/D converter, and is the output in external op-amp connection mode.
	ANEX1	I	This is the extended analog input pin for the A/D converter.
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P9_0 to P9_7, P10_0 to P10_7	I/O	8-bit I/O ports in CMOS, having a direction register to select an input or output. Each pin is set as an input port or output port. An input port can be set for a pull-up or for no pull-up in 4-bit unit by program. (however, P7_0 and P7_1 for the N-channel open drain output.)
	P8_0 to P8_4, P8_6, P8_7	I/O	I/O ports having equivalent functions to P0.
Input port	P8_5	I	Input pin for the $\overline{\text{NMI}}$ interrupt. Pin states can be read by the P8_5 bit in the P8 register.

I : Input O : Output I/O : Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.



NOTES:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.
The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers.
R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

3. Memory

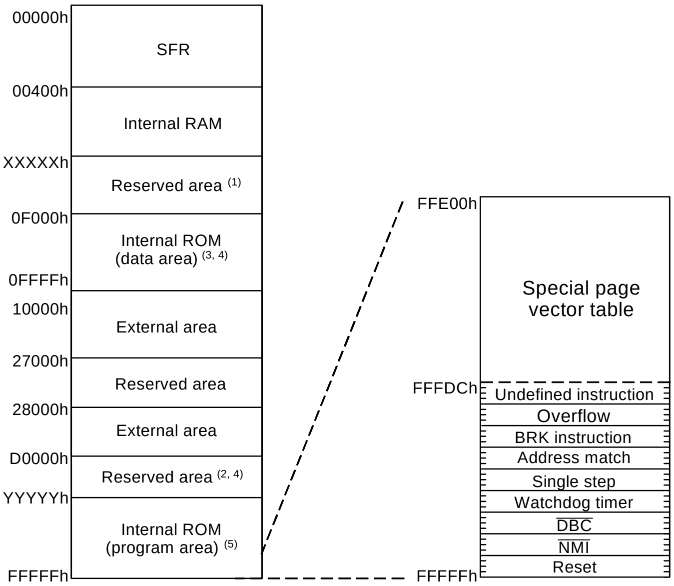
Figure 3.1 is a Memory Map of the M16C/30P group. The address space extends the 1 Mbyte from address 00000h to FFFFFh.

The internal ROM is allocated in a lower address direction beginning with address FFFFFh. For example, a 64-Kbyte internal ROM is allocated to the addresses from F0000h to FFFFFh.

The fixed interrupt vector table is allocated to the addresses from FFFDCh to FFFFFh. Therefore, store the start address of each interrupt routine here.

The internal RAM is allocated in an upper address direction beginning with address 00400h. For example, a 5-Kbyte internal RAM is allocated to the addresses from 00400h to 017FFh. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated. The SFR is allocated to the addresses from 00000h to 003FFh. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be used by users.

The special page vector table is allocated to the addresses from FFE00h to FFFDBh. This vector is used by the JMPS or JSRS instruction. For details, refer to the **M16C/60 and M16C/20 Series Software Manual**.



Internal RAM		Internal ROM [5]	
Size	Address XXXXXh	Size	Address YYYYYh
5 Kbytes	017FFh	96 Kbytes	E8000h
6 Kbytes	01BFFh	128 Kbytes	E0000h
12 Kbytes	033FFh	160 Kbytes	D8000h
		192 Kbytes	D0000h
		256 Kbytes	C0000h[6]

NOTES:
1. During memory expansion and microprocessor modes, can be used.
2. In memory expansion mode, can be used.
3. As for the flash memory version, 4-Kbyte space (block A) exists.
4. Shown here is a memory map for the case where the PM10 bit in the PM1 register is “1” .
5. When using the masked ROM version, write nothing to internal ROM area.
6. When the PM13 bit is set to "0", the address of Internal ROM becomes D0000h, and when the PM13 bit is set to "1", the address becomes C0000h.

Figure 3.1 Memory Map

Table 5.2 Recommended Operating Conditions (1)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply Voltage (V_{CC1}=V_{CC2})		2.7	5.0	5.5	V
AV_{CC}	Analog Supply Voltage			V_{CC}		V
V_{SS}	Supply Voltage			0		V
AV_{SS}	Analog Supply Voltage			0		V
V_{IH}	HIGH Input Voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7	0.8V_{CC}		V_{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode)	0.8V_{CC}		V_{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor mode)	0.5V_{CC}		V_{CC}	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, $\overline{\text{RESET}}$, CNVSS, BYTE	0.8V_{CC}		V_{CC}	V
		P7_0, P7_1	0.8V_{CC}		6.5	V
V_{IL}	LOW Input Voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7	0		0.2V_{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode)	0		0.2V_{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor mode)	0		0.16V_{CC}	V
		P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, XIN, $\overline{\text{RESET}}$, CNVSS, BYTE	0		0.2V_{CC}	V
$I_{OH(peak)}$	HIGH Peak Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7			−10.0	mA
$I_{OH(avg)}$	HIGH Average Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7			−5.0	mA
$I_{OL(peak)}$	LOW Peak Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7			10.0	mA
$I_{OL(avg)}$	LOW Average Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7			5.0	mA
f(XIN)	Main Clock Input Oscillation Frequency (4)	V_{CC}=3.0V to 5.5V	0		16	MHz
		V_{CC}=2.7V to 3.0V	0		20×V_{CC1}−44	MHz
f(XCIN)	Sub-Clock Oscillation Frequency			32.768	50	kHz
f(BCLK)	CPU Operation Clock		0		16	MHz

NOTES:

1. Referenced to V_{CC1} = V_{CC2} = 2.7 to 5.5V at T_{opr} = −20 to 85°C / −40 to 85°C unless otherwise specified.
2. The Average Output Current is the mean value within 100ms.
3. The total $I_{OL(peak)}$ for ports P0, P1, P2, P8_6, P8_7, P9 and P10 must be 80mA max. The total $I_{OL(peak)}$ for ports P3, P4, P5, P6, P7 and P8_0 to P8_4 must be 80mA max. The total $I_{OH(peak)}$ for ports P0, P1, and P2 must be −40mA max. The total $I_{OH(peak)}$ for ports P3, P4 and P5 must be −40mA max. The total $I_{OH(peak)}$ for ports P6, P7, and P8_0 to P8_4 must be −40mA max.
   The total $I_{OH(peak)}$ for ports P8_6, P8_7 and P9 must be −40mA max. Set Average Output Current to 1/2 of peak.
4. Relationship between main clock oscillation frequency, and supply voltage.

Main clock input oscillation frequency

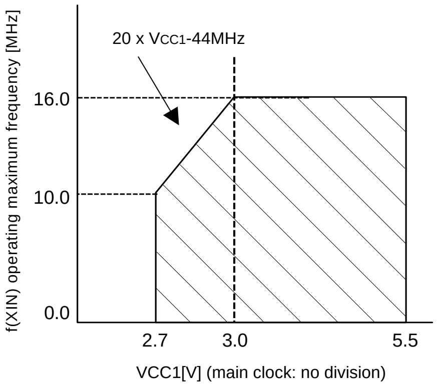


Table 5.8 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for Internal Power Supply Stabilization During Powering-On	V_{CC}=2.7V to 5.5V			2	ms
$t_{d(R-S)}$	STOP Release Time				1500	µs
$t_{d(W-S)}$	Low Power Dissipation Mode Wait Mode Release Time				1500	µs

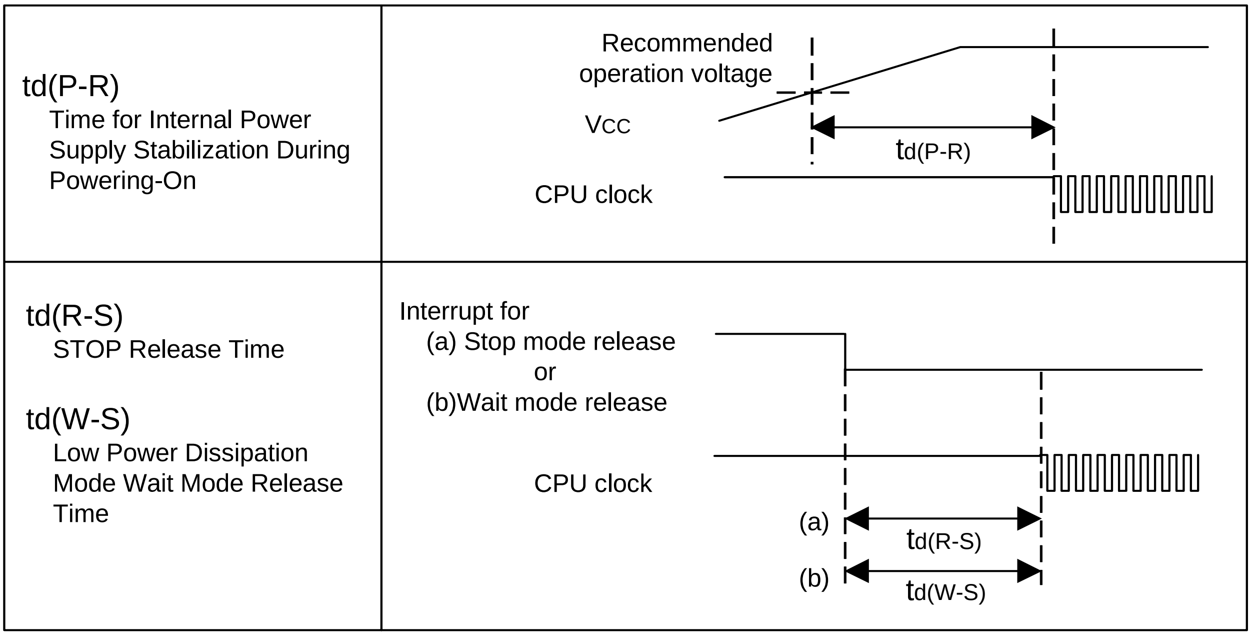


Figure 5.1 Power Supply Circuit Timing Diagram

Table 5.10 Electrical Characteristics (2) (1)

Symbol	Parameter	Measuring Condition			Standard			Unit
					Min.	Typ.	Max.	
I_{CC}	Power Supply Current (V_{CC1}=V_{CC2}=4.0V to 5.5V)	In single-chip mode, the output pins are open and other pins are V_{SS}	Mask ROM	f(XIN)=16MHz No division		10	15	mA
			One Time Flash	f(XIN)=16MHz, No division		10	18	mA
			Flash Memory	f(XIN)=16MHz, No division		12	18	mA
			One Time Flash	f(XIN)=10MHz, VCC1=5.0V		15		mA
			Flash Memory Program	f(XIN)=10MHz, VCC1=5.0V		15		mA
			Flash Memory Erase	f(XIN)=10MHz, VCC1=5.0V		25		mA
			Mask ROM	f(XCIN)=32kHz Low power dissipation mode, ROM (3)		25		µA
			One Time Flash	f(XCIN)=32kHz Low power dissipation mode, RAM (3)		25		µA
				f(XCIN)=32kHz Low power dissipation mode, Flash Memory (3)		350		µA
			Flash Memory	f(XCIN)=32kHz Low power dissipation mode, RAM (3)		25		µA
				f(XCIN)=32kHz Low power dissipation mode, Flash Memory (3)		420		µA
			Mask ROM One Time Flash Flash Memory	f(XCIN)=32kHz Wait mode (2), Oscillation capability High		7.5		µA
				f(XCIN)=32kHz Wait mode (2), Oscillation capability Low		2.0		µA
				Stop mode Topr =25°C		0.8	3.0	µA

NOTES:

1. Referenced to V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS} = 0V at T_{opr} = –20 to 85°C / –40 to 85°C, f(XIN)=16MHz unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.

$V_{CC1}=V_{CC2}=5V$

Timing Requirements
(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.19 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on both edges)	80		ns

Table 5.20 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	200		ns

Table 5.21 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	200		ns

Table 5.22 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{\text{ADTRG}}$ Input Cycle Time	1000		ns
$t_{w(ADL)}$	$\overline{\text{ADTRG}}$ input LOW Pulse Width	125		ns

Table 5.23 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input HIGH Pulse Width	100		ns
$t_{w(CKL)}$	CLKi Input LOW Pulse Width	100		ns
$t_{d(C-Q)}$	TXDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TXDi Hold Time	0		ns
$t_{su(D-C)}$	RXDi Input Setup Time	70		ns
$t_{h(C-D)}$	RXDi Input Hold Time	90		ns

Table 5.24 External Interrupt $\overline{\text{INTi}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{\text{INTi}}$ Input HIGH Pulse Width	250		ns
$t_{w(INL)}$	$\overline{\text{INTi}}$ Input LOW Pulse Width	250		ns

$V_{CC1}=V_{CC2}=5V$

Switching Characteristics
(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.26 Memory Expansion and Microprocessor Modes (for 1 wait setting and external area access)

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See **Figure 5.2**		25	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (in relation to BCLK)		–3		ns
$t_{h(RD-AD)}$	Address Output Hold Time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
$t_{d(BCLK-CS)}$	Chip Select Output Delay Time			25	ns
$t_{h(BCLK-CS)}$	Chip Select Output Hold Time (in relation to BCLK)		–3		ns
$t_{d(BCLK-ALE)}$	ALE Signal Output Delay Time			15	ns
$t_{h(BCLK-ALE)}$	ALE Signal Output Hold Time		–4		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			25	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		0		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			25	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(BCLK-DB)}$	Data Output Delay Time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data Output Hold Time (in relation to BCLK) (3)		4		ns
$t_{d(DB-WR)}$	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
th(WR-DB)	Data Output Hold Time (in relation to WR)(3)		(NOTE 2)		ns
$t_{d(BCLK-HLDA)}$	HLDA Output Delay Time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

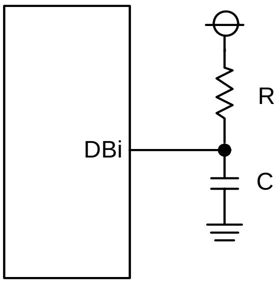
$$\frac{(n-0.5)x10^9}{f(BCLK)} - 40[ns]$$

n is “1” for 1-wait setting, f(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5x10^9}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = –CR \times \ln (1–V_{OL} / V_{CC1})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC1}$, C = 30pF, R = 1kΩ, hold time of output ”L” level is
$t = –30pF \times 1kΩ \times \ln(1–0.2V_{CC1} / V_{CC1})$
= 6.7ns.



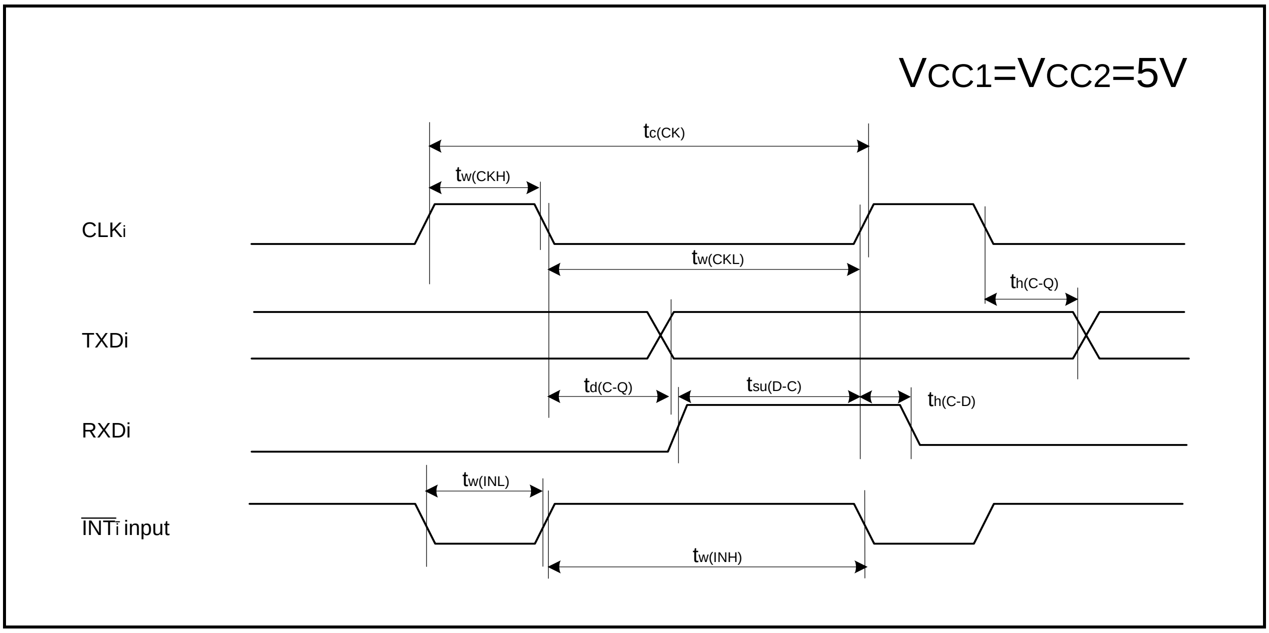
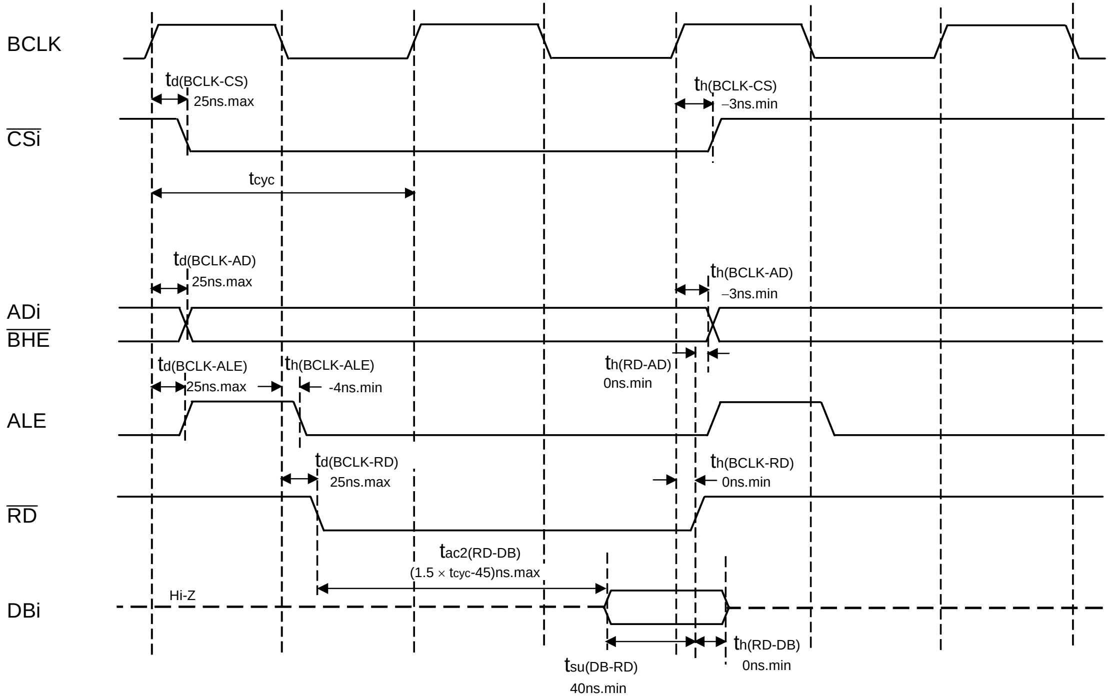


Figure 5.4 Timing Diagram (2)

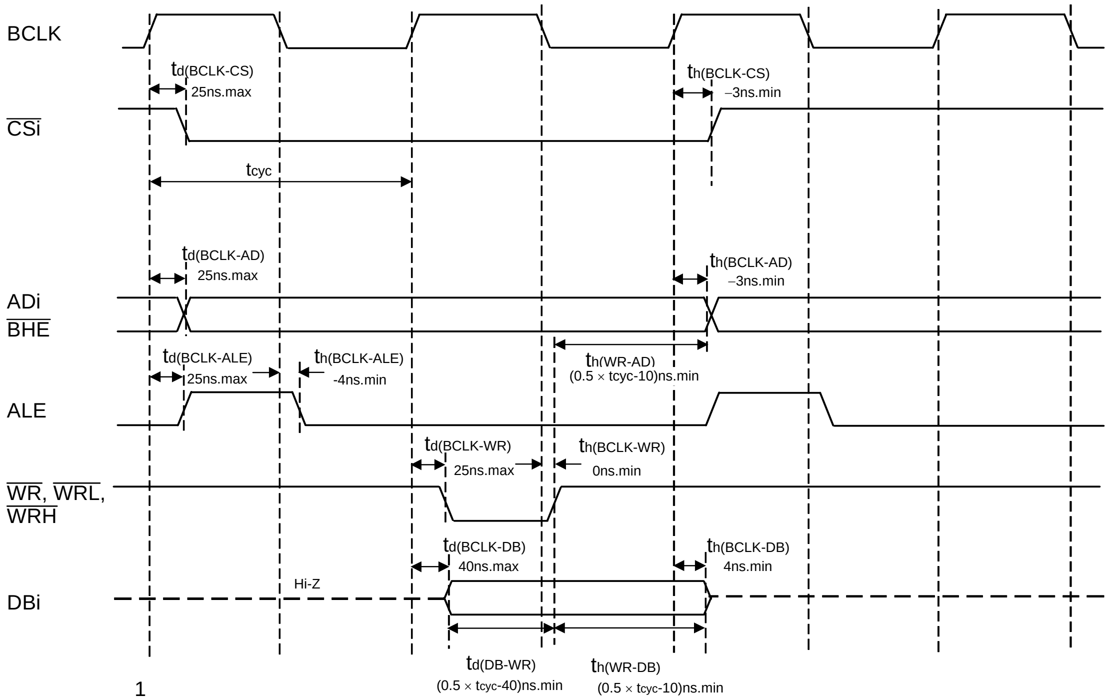
$V_{CC1}=V_{CC2}=5V$

Memory Expansion Mode, Microprocessor Mode
(for 1-wait setting and external area access**)**

Read timing



Write timing



$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
· Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

Figure 5.7 Timing Diagram (5)

VCC1=VCC2=3V

Timing Requirements
(VCC1 = VCC2 = 3V, VSS = 0V, at Topr = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.29 External Clock Input (XIN input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	(NOTE 2)		ns
$t_{w(H)}$	External Clock Input HIGH Pulse Width	(NOTE 3)		ns
$t_{w(L)}$	External Clock Input LOW Pulse Width	(NOTE 3)		ns
t_r	External Clock Rise Time		(NOTE 4)	ns
t_f	External Clock Fall Time		(NOTE 4)	ns

NOTES:
1. The condition is VCC1=VCC2=2.7 to 3.0V.
2. Calculated according to the VCC1 voltage as follows:

$$\frac{10^{-6}}{20 \times V_{CC1} - 44} \text{ [ns]}$$

3. Calculated according to the VCC1 voltage as follows:

$$\frac{10^{-6}}{20 \times V_{CC1} - 44} \times 0.4 \text{ [ns]}$$

4. Calculated according to the VCC1 voltage as follows:

$$-10 \times V_{CC1} + 45 \text{ [ns]}$$

Table 5.30 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (for setting with no wait)		(NOTE 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (for setting with wait)		(NOTE 2)	ns
$t_{su(DB-RD)}$	Data Input Setup Time	50		ns
$t_{su(RDY-BCLK)}$	$\overline{\text{RDY}}$ Input Setup Time	40		ns
$t_{su(HOLD-BCLK)}$	$\overline{\text{HOLD}}$ Input Setup Time	50		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{\text{RDY}}$ Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{\text{HOLD}}$ Input Hold Time	0		ns

NOTES:
1. Calculated according to the BCLK frequency as follows:

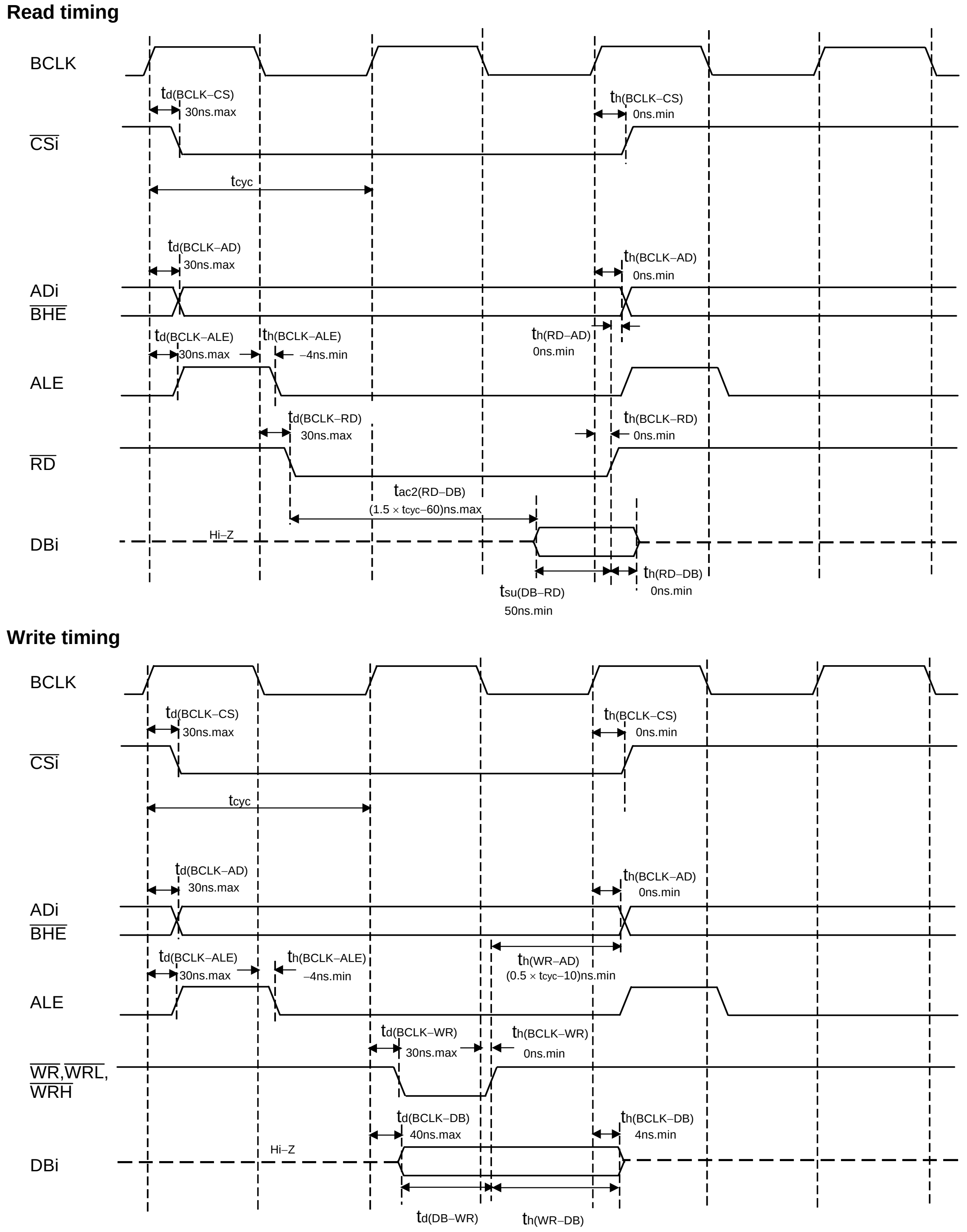
$$\frac{0.5 \times 10^{9}}{f(BCLK)} - 60 \text{[ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^{9}}{f(BCLK)} - 60 \text{[ns]}$$ n is ”2” for 1-wait setting.

$V_{CC1}=V_{CC2}=3V$

Memory Expansion Mode, Microprocessor Mode
(for 1-wait setting and external area access**)**



$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

Figure 5.13 Timing Diagram (5)

REVISION HISTORY	M16C/30P Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.20	Oct 17, 2006	1	Note is partly deleted.
		2	Table 1.1 Performance Outline of M16C/30P Group is partly added.
		4	Table 1.2 Product List is partly revised.
		5	Figure 1.2 Type No., Memory Size, and Package is added.
		7	Table 1.4 Product Code of One Time Flash version, Flash Memory version, and ROM-less version for M16C/30P is partly added.
		17	Figure 3.1 Memory Map is partly added.
		19	Table 4.2 SFR Information (2) is partly added.
		23	Table 5.1 Absolute Maximum Ratings is partly added.
		27	Table 5.6 One Time Flash Version Electrical Characteristics and Table 5.7 One Time Flash Version Program Voltage and Read Operation Voltage Characteristics is added.
		30	Table 5.10 Electrical Characteristics (2) is partly added.
		42	Table 5.28 Electrical Characteristics (2) is partly added.
1.21	Nov 02 2006	7	Table 1.4 Product Code of One Time Flash version, Flash Memory version, and ROM-less version for M16C/30P is partly revised.
1.22	Mar 30, 2007	4	Table 1.2 Product List (1) is partly revised.
		5	Table 1.3 Product List (2) is partly revised.
		19	Table 4.2 SFR Information (2) is partly revised.

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
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