Renesas Electronics America Inc - M30302FAPGP#U3 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M16C/60
Core Size	16-Bit
Speed	16MHz
Connectivity	I²C, IEBus, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	5K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 18x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30302fapgp-u3

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1.2 Performance Outline

Table 1.1 lists Performance Outline of M16C/30P Group.

Table 1.1 Performance Outline of M16C/30P Group

Item		Performance
CPU	Number of Basic Instructions	91 instructions
	Minimum Instruction Execution Time	62.5ns(f(XIN)=16MHz, VCC1=VCC2=3.0 to 5.5V, no wait) 100ns(f(XIN)=10MHz, VCC1=VCC2=2.7 to 5.5V, no wait)
	Operation Mode	Single-chip, memory expansion and microprocessor mode
	Memory Space	1 Mbyte
	Memory Capacity	See **Table 1.2 Product List**
Peripheral Function	Port	Input/Output : 87 pins, Input : 1 pin
	Multifunction Timer	Timer A : 16 bits x 3 channels, Timer B : 16 bits x 3 channels
	Serial Interface	1 channels Clock synchronous, UART, I^{2}CBus(1), IEBus(2) 2 channels Clock synchronous, UART, I^{2}CBus(1)
	A/D Converter	10-bit A/D converter: 1 circuit, 18 channels
	DMAC	2 channels
	CRC Calculation Circuit	CCITT-CRC
	Watchdog Timer	15 bits x 1 channel (with prescaler)
	Interrupt	Internal: 20 sources, External: 7 sources, Software: 4 sources, Priority level: 7 levels
	Clock Generating Circuit	2 circuits Main clock generation circuit (*), Subclock generation circuit (*), (*)Equipped with a built-in feedback resistor.
Electric Characteristics	Supply Voltage	VCC1=VCC2=3.0 to 5.5 V (f(XIN)=16MHz) VCC1=VCC2=2.7 to 5.5 V (f(XIN)=10MHz, no wait)
	Power Consumption	10 mA (VCC1=VCC2=5V, f(XIN)=16MHz) 8 mA (VCC1=VCC2=3V, f(XIN)=10MHz) 1.8 µA (VCC1=VCC2=3V, f(XCIN)=32kHz, wait mode) 0.7 µA(VCC1=VCC2=3V, stop mode)
One time flash version	Program Supply Voltage	3.3±0.3 V or 5.0±0.5 V
Flash memory version	Program/Erase Supply Voltage	3.3±0.3 V or 5.0±0.5 V
	Program and Erase Endurance	100 times (all area)
Operating Ambient Temperature		-20 to 85°C, -40 to 85°C
Package		100-pin plastic mold QFP, LQFP

NOTES:

1. I^{2}C bus is a registered trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a registered trademark of NEC Electronics Corporation.
3. Use the M16C/30P on VCC1 = VCC2.

Table 1.3 Product List (2) **As of March 2007**

Part No.	ROM Capacity	RAM Capacity	package code (1)	Remarks
M30302FAPFP	96 K + 4 Kbytes	5 Kbytes	PRQP0100JB-A	Flash memory version(2)
M30302FAPGP			PLQP0100KB-A	
M30302FCPFP	128 K + 4 Kbytes		PRQP0100JB-A	
M30302FCPGP			PLQP0100KB-A	
M30302FEPFP	192 K + 4 Kbytes	6 Kbytes	PRQP0100JB-A	
M30302FEPGP			PLQP0100KB-A	
M30302SPFP	-	6 Kbytes	PRQP0100JB-A	ROM-less version
M30302SPGP			PLQP0100KB-A	

(D): Under development
(P): Under planning
NOTES:

1. Previous package codes are as follows.
   PRQP0100JB-A : 100P6S-A,
   PLQP0100KB-A : 100P6Q-A
2. Block A (4-Kbytes space) is available in flash memory version.

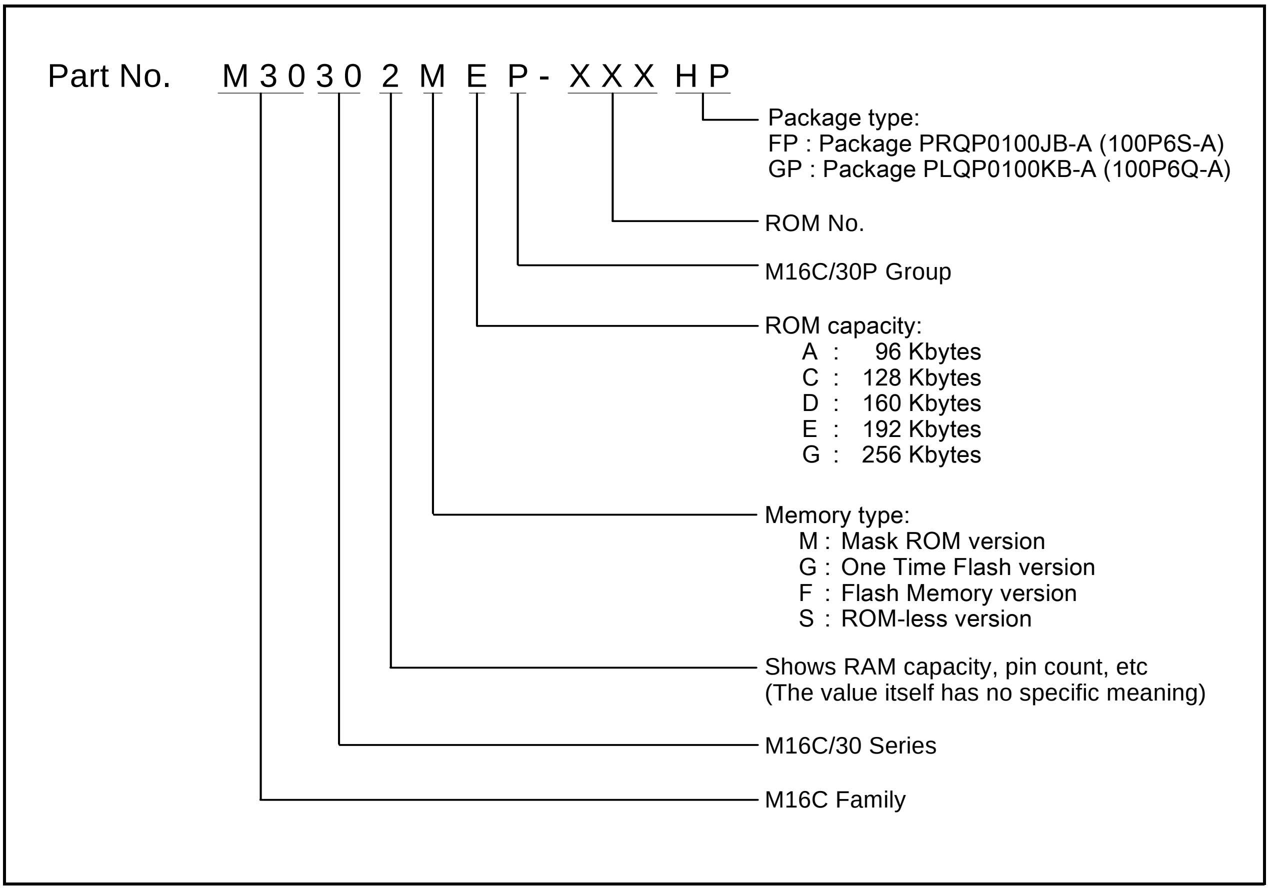
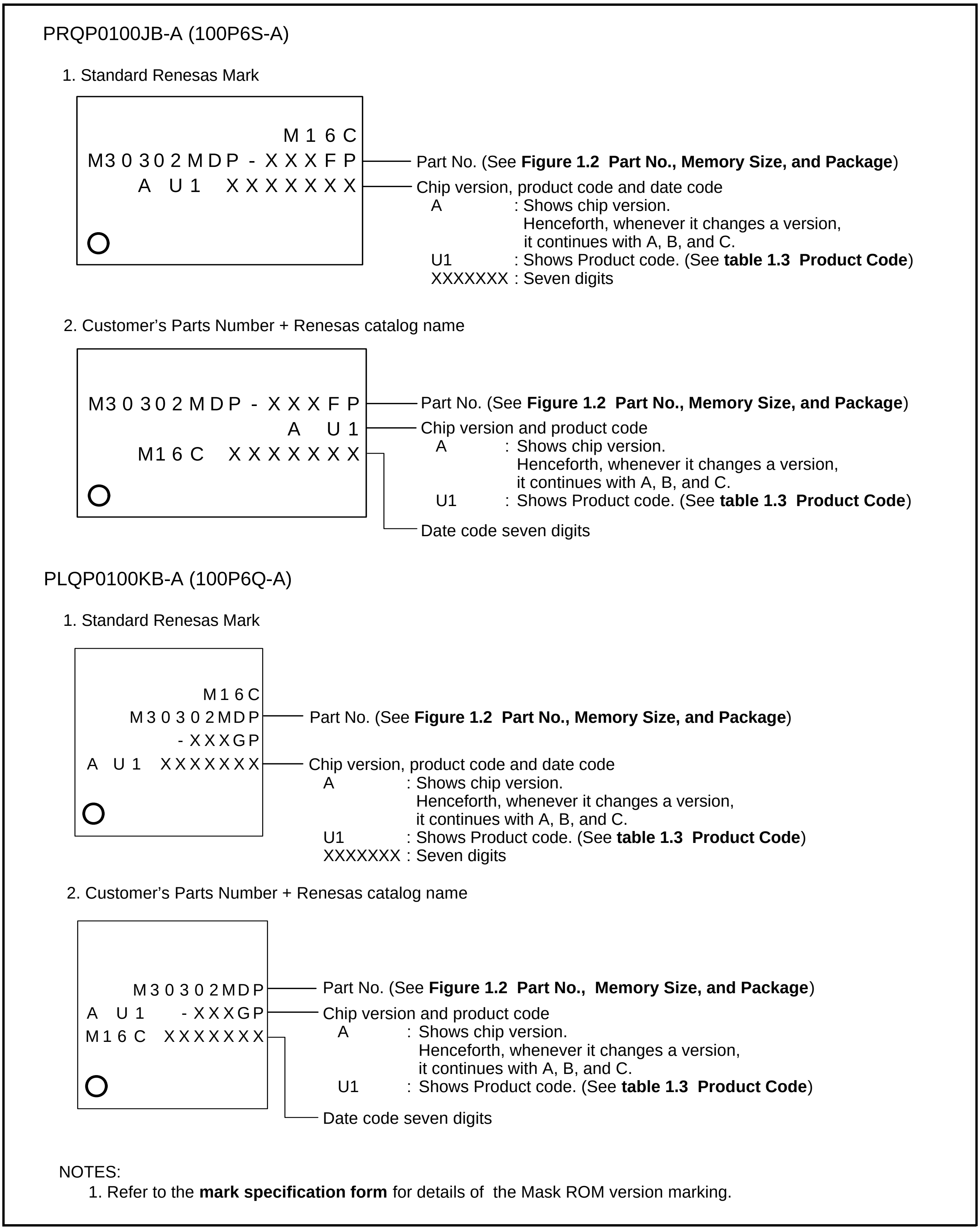


Figure 1.2 Part No., Memory Size, and Package

Table 1.4 Product Code of MASK ROM version for M16C/30P

Product Code	Package	Operating Ambient Temperature
U1	Lead-free	-20°C to 85°C
U4		-40°C to 85°C



Part No. (See **Figure 1.2 Part No., Memory Size, and Package**)

Chip version, product code and date code

A : Shows chip version.
Henceforth, whenever it changes a version,
it continues with A, B, and C.
U1 : Shows Product code. (See **table 1.3 Product Code**)
XXXXXXX : Seven digits

Part No. (See **Figure 1.2 Part No., Memory Size, and Package**)

Chip version and product code

A : Shows chip version.
Henceforth, whenever it changes a version,
it continues with A, B, and C.
U1 : Shows Product code. (See **table 1.3 Product Code**)

Date code seven digits

Part No. (See **Figure 1.2 Part No., Memory Size, and Package**)

Chip version, product code and date code

A : Shows chip version.
Henceforth, whenever it changes a version,
it continues with A, B, and C.
U1 : Shows Product code. (See **table 1.3 Product Code**)
XXXXXXX : Seven digits

Part No. (See **Figure 1.2 Part No., Memory Size, and Package**)

Chip version and product code

A : Shows chip version.
Henceforth, whenever it changes a version,
it continues with A, B, and C.
U1 : Shows Product code. (See **table 1.3 Product Code**)

Date code seven digits

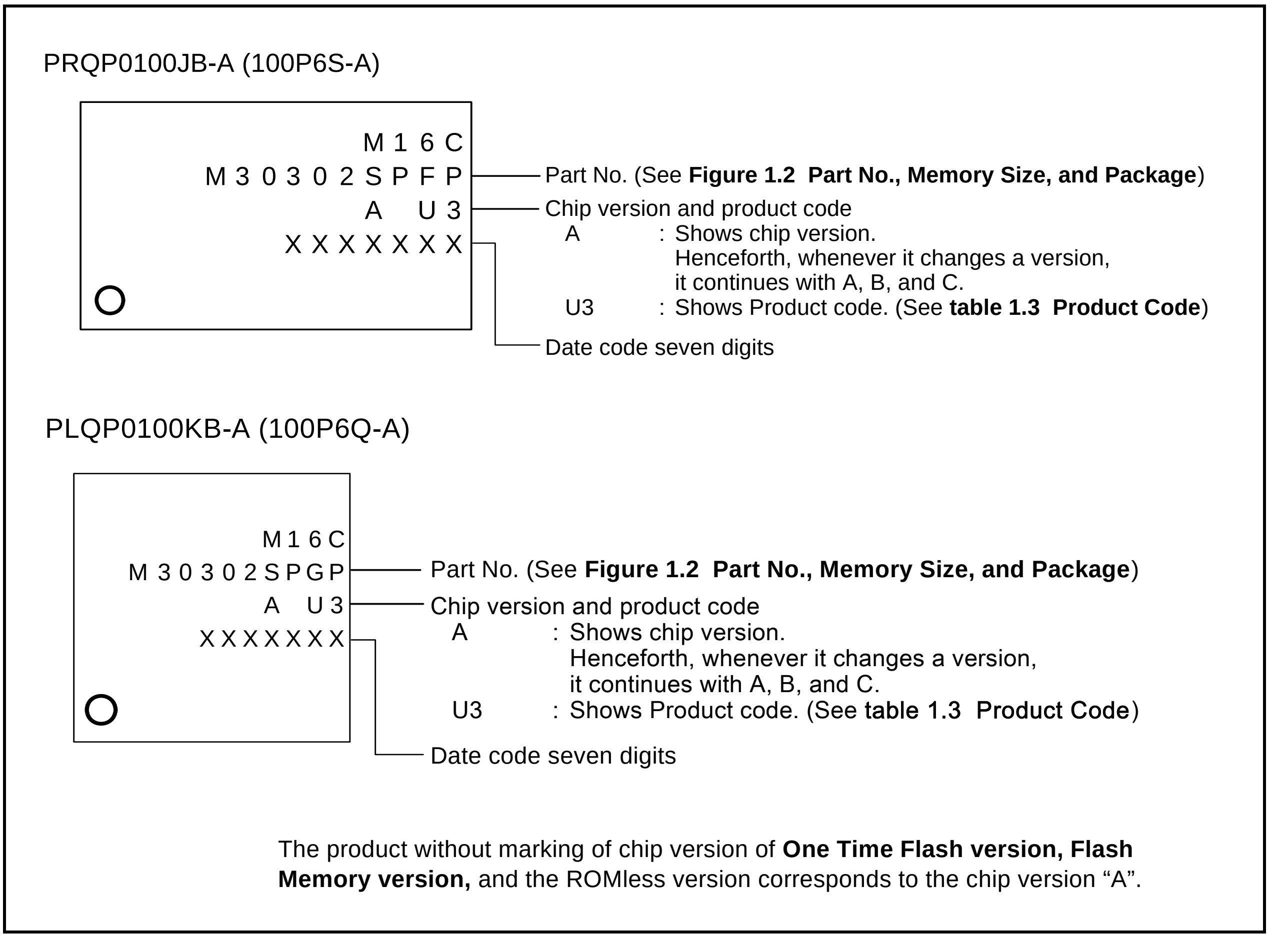
NOTES:
1. Refer to the **mark specification form** for details of the Mask ROM version marking.

Figure 1.3 Marking Diagram of Mask ROM Version for M16C/30P (Top View)

Table 1.5 Product Code of One Time Flash version, Flash Memory version, and ROM-less version for M16C/30P

	Product Code	Package	Internal ROM		Operating Ambient Temperature
			Program and Erase Endurance	Temperature Range	
One Time Flash version	U3	Lead-free	0	0°C to 60°C	-40°C to 85°C
	U5				-20°C to 85°C
Flash Memory version	U3	Lead-free	100	0°C to 60°C	-40°C to 85°C
	U5				-20°C to 85°C
ROM-less version	U3	Lead-free	–	–	-40°C to 85°C
	U5				-20°C to 85°C

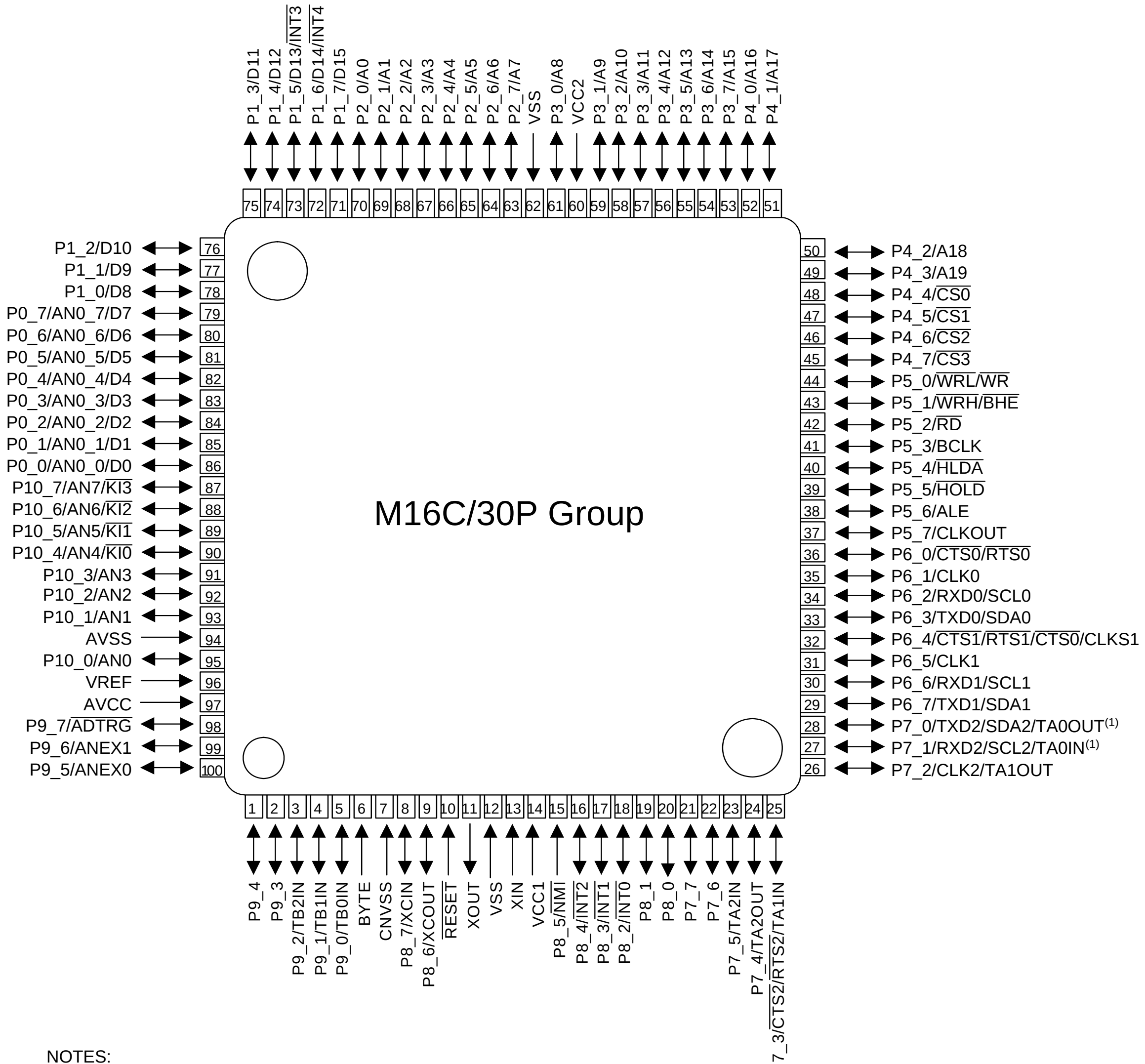
NOTES:The one time flash version can be written once only.



The product without marking of chip version of **One Time Flash version, Flash Memory version,** and the ROMless version corresponds to the chip version “A”.

Figure 1.4 Marking Diagram of One Time Flash version, Flash Memory version, and ROM-less Version for M16C/30P (Top View)

PIN CONFIGURATION (top view)



NOTES:
1. P7_0 and P7_1 are N channel open-drain output pins.
2. Use the M16C/30P on VCC1=VCC2.

Package : PLQP0100KB-A (100P6Q-A)

Figure 1.6 Pin Configuration (Top View)

Table 1.6 Pin Characteristics (1)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
FP	GP							
1	99		P9_6				ANEX1	
2	100		P9_5				ANEX0	
3	1		P9_4					
4	2		P9_3					
5	3		P9_2		TB2IN			
6	4		P9_1		TB1IN			
7	5		P9_0		TB0IN			
8	6	BYTE						
9	7	CNVSS						
10	8	XCIN	P8_7					
11	9	XCOUT	P8_6					
12	10	$\overline{\text{RESET}}$						
13	11	XOUT						
14	12	VSS						
15	13	XIN						
16	14	VCC1						
17	15		P8_5	$\overline{\text{NMI}}$				
18	16		P8_4	$\overline{\text{INT2}}$				
19	17		P8_3	$\overline{\text{INT1}}$				
20	18		P8_2	$\overline{\text{INT0}}$				
21	19		P8_1					
22	20		P8_0					
23	21		P7_7					
24	22		P7_6					
25	23		P7_5		TA2IN			
26	24		P7_4		TA2OUT			
27	25		P7_3		TA1IN	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$		
28	26		P7_2		TA1OUT	CLK2		
29	27		P7_1		TA0IN	RXD2/SCL2		
30	28		P7_0		TA0OUT	TXD2/SDA2		
31	29		P6_7			TXD1/SDA1		
32	30		P6_6			RXD1/SCL1		
33	31		P6_5			CLK1		
34	32		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/CLKS1		
35	33		P6_3			TXD0/SDA0		
36	34		P6_2			RXD0/SCL0		
37	35		P6_1			CLK0		
38	36		P6_0			$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$		
39	37		P5_7					$\overline{\text{RDY}}$/CLKOUT
40	38		P5_6					ALE
41	39		P5_5					$\overline{\text{HOLD}}$
42	40		P5_4					$\overline{\text{HLDA}}$
43	41		P5_3					BCLK
44	42		P5_2					$\overline{\text{RD}}$
45	43		P5_1					$\overline{\text{WRH}}$/$\overline{\text{BHE}}$
46	44		P5_0					$\overline{\text{WRL}}$/$\overline{\text{WR}}$
47	45		P4_7					$\overline{\text{CS3}}$
48	46		P4_6					$\overline{\text{CS2}}$
49	47		P4_5					$\overline{\text{CS1}}$
50	48		P4_4					$\overline{\text{CS0}}$

Table 1.7 Pin Characteristics (2)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
FP	GP							
51	49		P4_3					A19
52	50		P4_2					A18
53	51		P4_1					A17
54	52		P4_0					A16
55	53		P3_7					A15
56	54		P3_6					A14
57	55		P3_5					A13
58	56		P3_4					A12
59	57		P3_3					A11
60	58		P3_2					A10
61	59		P3_1					A9
62	60	VCC2						
63	61		P3_0					A8
64	62	VSS						
65	63		P2_7					A7
66	64		P2_6					A6
67	65		P2_5					A5
68	66		P2_4					A4
69	67		P2_3					A3
70	68		P2_2					A2
71	69		P2_1					A1
72	70		P2_0					A0
73	71		P1_7					D15
74	72		P1_6	$\overline{\text{INT4}}$				D14
75	73		P1_5	$\overline{\text{INT3}}$				D13
76	74		P1_4					D12
77	75		P1_3					D11
78	76		P1_2					D10
79	77		P1_1					D9
80	78		P1_0					D8
81	79		P0_7				AN0_7	D7
82	80		P0_6				AN0_6	D6
83	81		P0_5				AN0_5	D5
84	82		P0_4				AN0_4	D4
85	83		P0_3				AN0_3	D3
86	84		P0_2				AN0_2	D2
87	85		P0_1				AN0_1	D1
88	86		P0_0				AN0_0	D0
89	87		P10_7	$\overline{\text{KI3}}$			AN7	
90	88		P10_6	$\overline{\text{KI2}}$			AN6	
91	89		P10_5	$\overline{\text{KI1}}$			AN5	
92	90		P10_4	$\overline{\text{KI0}}$			AN4	
93	91		P10_3				AN3	
94	92		P10_2				AN2	
95	93		P10_1				AN1	
96	94	AVSS						
97	95		P10_0				AN0	
98	96	VREF						
99	97	AVCC						
100	98		P9_7				$\overline{\text{ADTRG}}$	

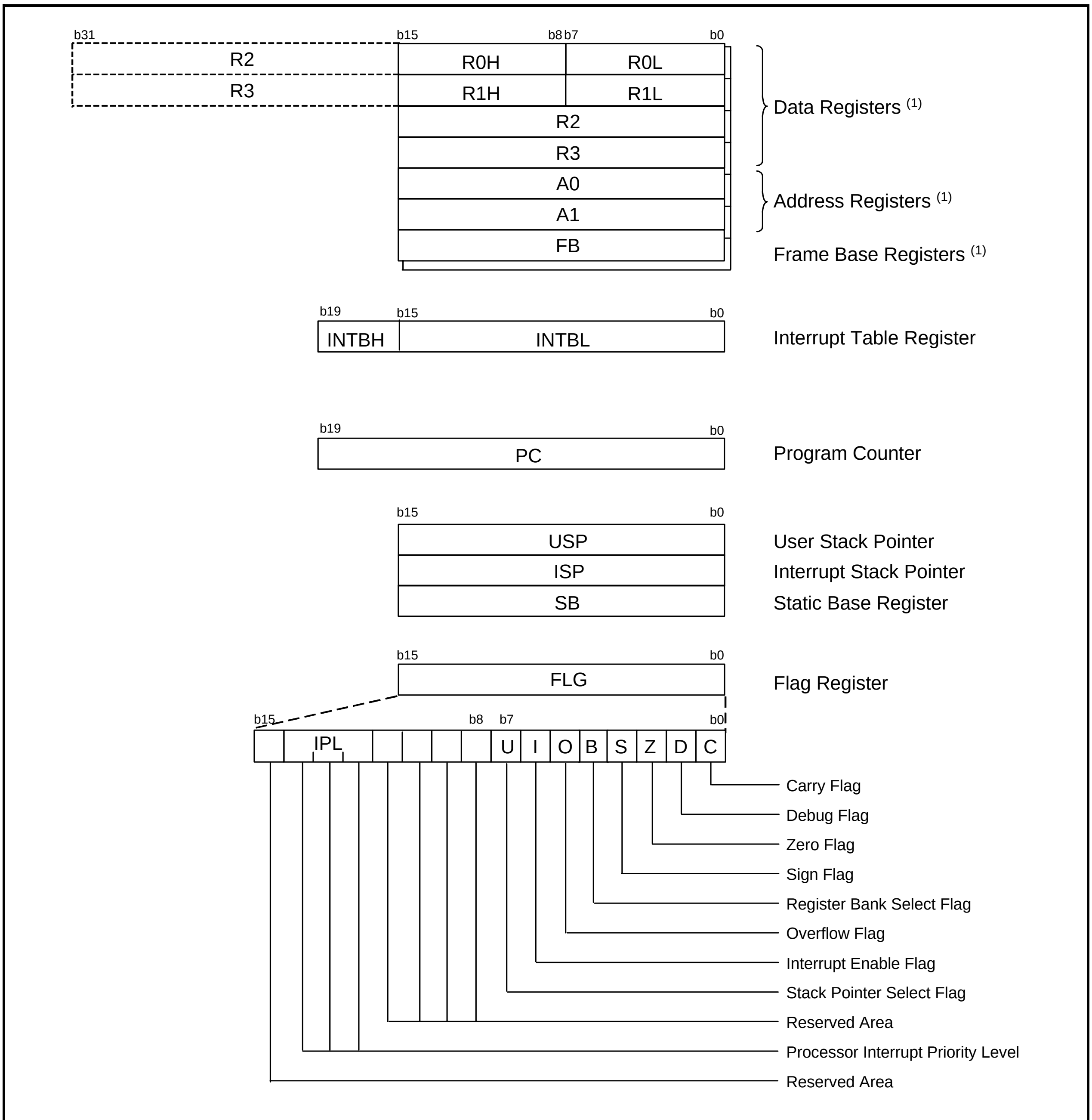
Table 1.9 Pin Description (2)

Signal Name	Pin Name	I/O Type	Description
Main clock input	XIN	I	I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To use the external clock, input the clock from XIN and leave XOUT open.
Main clock output	XOUT	O	
Sub clock input	XCIN	I	I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT. To use the external clock, input the clock from XCIN and leave XCOUT open.
Sub clock output	XCOUT	O	
Clock output	CLKOUT	O	The clock of the same cycle as fC, f8, or f32 is outputted.
$\overline{\mathrm{INT}}$ interrupt input	$\overline{\mathrm{INT0}}$ to $\overline{\mathrm{INT4}}$	I	Input pins for the $\overline{\mathrm{INT}}$ interrupt.
$\overline{\mathrm{NMI}}$ interrupt input	$\overline{\mathrm{NMI}}$	I	Input pin for the $\overline{\mathrm{NMI}}$ interrupt.
Key input interrupt input	$\overline{\mathrm{KI0}}$ to $\overline{\mathrm{KI3}}$	I	Input pins for the key input interrupt.
Timer A	TA0OUT to TA2OUT	I/O	These are timer A0 to timer A2 I/O pins. (however, the output of TA0OUT for the N-channel open drain output.)
	TA0IN to TA2IN	I	These are timer A0 to timer A2 input pins.
Timer B	TB0IN to TB2IN	I	These are timer B0 to timer B2 input pins.
Serial interface	$\overline{\mathrm{CTS0}}$ to $\overline{\mathrm{CTS2}}$	I	These are send control input pins.
	$\overline{\mathrm{RTS0}}$ to $\overline{\mathrm{RTS2}}$	O	These are receive control output pins.
	CLK0 to CLK2	I/O	These are transfer clock I/O pins.
	RXD0 to RXD2	I	These are serial data input pins.
	TXD0 to TXD2	O	These are serial data output pins. (however, TXD2 for the N-channel open drain output.)
	CLKS1	O	This is output pin for transfer clock output from multiple pins function.
I^2C mode	SDA0 to SDA2	I/O	These are serial data I/O pins. (however, SDA2 for the N-channel open drain output.)
	SCL0 to SCL2	I/O	These are transfer clock I/O pins. (however, SCL2 for the N-channel open drain output.)
Reference voltage input	VREF	I	Applies the reference voltage for the A/D converter.
A/D converter	AN0 to AN7, AN0_0 to AN0_7	I	Analog input pins for the A/D converter.
	$\overline{\mathrm{ADTRG}}$	I	This is an A/D trigger input pin.
	ANEX0	I/O	This is the extended analog input pin for the A/D converter, and is the output in external op-amp connection mode.
	ANEX1	I	This is the extended analog input pin for the A/D converter.
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P9_0 to P9_7, P10_0 to P10_7	I/O	8-bit I/O ports in CMOS, having a direction register to select an input or output. Each pin is set as an input port or output port. An input port can be set for a pull-up or for no pull-up in 4-bit unit by program. (however, P7_0 and P7_1 for the N-channel open drain output.)
	P8_0 to P8_4, P8_6, P8_7	I/O	I/O ports having equivalent functions to P0.
Input port	P8_5	I	Input pin for the $\overline{\mathrm{NMI}}$ interrupt. Pin states can be read by the P8_5 bit in the P8 register.

I : Input O : Output I/O : Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.



NOTES:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers.

R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After Reset
0380h	Count Start Flag	TABSR	000XX000b
0381h	Clock Prescaler Reset Fag	CPSRF	0XXXXXXXb
0382h	One-Shot Start Flag	ONSF	00XXX000b
0383h	Trigger Select Register	TRGSR	XXXX0000b
0384h	Up-Down Flag	UDF	XX0XX000b (2)
0385h			
0386h 0387h	Timer A0 Register	TA0	XXh XXh
0388h 0389h	Timer A1 Register	TA1	XXh XXh
038Ah 038Bh	Timer A2 Register	TA2	XXh XXh
038Ch			
038Dh			
038Eh			
038Fh			
0390h 0391h	Timer B0 Register	TB0	XXh XXh
0392h 0393h	Timer B1 Register	TB1	XXh XXh
0394h 0395h	Timer B2 Register	TB2	XXh XXh
0396h	Timer A0 Mode Register	TA0MR	00h
0397h	Timer A1 Mode Register	TA1MR	00h
0398h	Timer A2 Mode Register	TA2MR	00h
0399h			
039Ah			
039Bh	Timer B0 Mode Register	TB0MR	00XX0000b
039Ch	Timer B1 Mode Register	TB1MR	00XX0000b
039Dh	Timer B2 Mode Register	TB2MR	00XX0000b
039Eh			
039Fh			
03A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
03A1h	UART0 Bit Rate Generator	U0BRG	XXh
03A2h 03A3h	UART0 Transmit Buffer Register	U0TB	XXh XXh
03A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
03A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
03A6h 03A7h	UART0 Receive Buffer Register	U0RB	XXh XXh
03A8h	UART1 Transmit/Receive Mode Register	U1MR	00h
03A9h	UART1 Bit Rate Generator	U1BRG	XXh
03AAh 03ABh	UART1 Transmit Buffer Register	U1TB	XXh XXh
03ACh	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
03ADh	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
03AEh 03AFh	UART1 Receive Buffer Register	U1RB	XXh XXh
03B0h	UART Transmit/Receive Control Register 2	UCON	X0000000b
03B1h			
03B2h			
03B3h			
03B4h			
03B5h			
03B6h			
03B7h			
03B8h	DMA0 Request Factor Select Register	DM0SL	00h
03B9h			
03BAh	DMA1 Request Factor Select Register	DM1SL	00h
03BBh			
03BCh 03BDh	CRC Data Register	CRCD	XXh XXh
03BEh	CRC Input Register	CRCIN	XXh
03BFh			

NOTES:
1. The blank areas are reserved and cannot be accessed by users.
2. Bit 5 in the Up-down flag is “0” by reset. However, The values in these bits when read are indeterminate.

X : Nothing is mapped to this bit

Table 5.10 Electrical Characteristics (2) [1]

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
I_{CC}	Power Supply Current (V_{CC1}=V_{CC2}=4.0V to 5.5V)	In single-chip mode, the output pins are open and other pins are V_{SS}	Mask ROM	f(XIN)=16MHz No division		10	15	mA
			One Time Flash	f(XIN)=16MHz, No division		10	18	mA
			Flash Memory	f(XIN)=16MHz, No division		12	18	mA
			One Time Flash	f(XIN)=10MHz, VCC1=5.0V		15		mA
			Flash Memory Program	f(XIN)=10MHz, VCC1=5.0V		15		mA
			Flash Memory Erase	f(XIN)=10MHz, VCC1=5.0V		25		mA
			Mask ROM	f(XCIN)=32kHz Low power dissipation mode, ROM [3]		25		µA
			One Time Flash	f(XCIN)=32kHz Low power dissipation mode, RAM [3]		25		µA
				f(XCIN)=32kHz Low power dissipation mode, Flash Memory [3]		350		µA
			Flash Memory	f(XCIN)=32kHz Low power dissipation mode, RAM [3]		25		µA
				f(XCIN)=32kHz Low power dissipation mode, Flash Memory [3]		420		µA
			Mask ROM One Time Flash Flash Memory	f(XCIN)=32kHz Wait mode [2], Oscillation capability High		7.5		µA
				f(XCIN)=32kHz Wait mode [2], Oscillation capability Low		2.0		µA
				Stop mode Topr =25°C		0.8	3.0	µA

NOTES:
1. Referenced to V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS} = 0V at T_{opr} = –20 to 85°C / –40 to 85°C, f(XIN)=16MHz unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.

VCC1=VCC2=5V

Timing Requirements
(VCC1 = VCC2 = 5V, VSS = 0V, at Topr = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.13 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	40		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	40		ns

Table 5.14 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	200		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	200		ns

Table 5.15 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	100		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	100		ns

Table 5.16 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	100		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	100		ns

Table 5.17 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAiOUT Input HIGH Pulse Width	1000		ns
$t_{w(UPL)}$	TAiOUT Input LOW Pulse Width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

Table 5.18 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT Input Setup Time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN Input Setup Time	200		ns

$V_{CC1}=V_{CC2}=5V$

Switching Characteristics
($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to 85°C / –40 to 85°C unless otherwise specified)

Table 5.26 Memory Expansion and Microprocessor Modes (for 1 wait setting and external area access)

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See **Figure 5.2**		25	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (in relation to BCLK)		–3		ns
$t_{h(RD-AD)}$	Address Output Hold Time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
$t_{d(BCLK-CS)}$	Chip Select Output Delay Time			25	ns
$t_{h(BCLK-CS)}$	Chip Select Output Hold Time (in relation to BCLK)		–3		ns
$t_{d(BCLK-ALE)}$	ALE Signal Output Delay Time			15	ns
$t_{h(BCLK-ALE)}$	ALE Signal Output Hold Time		–4		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			25	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		0		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			25	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(BCLK-DB)}$	Data Output Delay Time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data Output Hold Time (in relation to BCLK) (3)		4		ns
$t_{d(DB-WR)}$	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
th(WR-DB)	Data Output Hold Time (in relation to WR)(3)		(NOTE 2)		ns
$t_{d(BCLK-HLDA)}$	HLDA Output Delay Time			40	ns

NOTES:

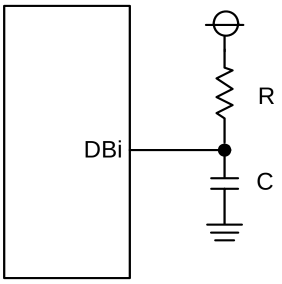
1. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5)x10^9}{f(BCLK)} - 40[ns] \qquad \text{n is “1” for 1-wait setting, f(BCLK) is 12.5MHz or less.}$$

2. Calculated according to the BCLK frequency as follows:

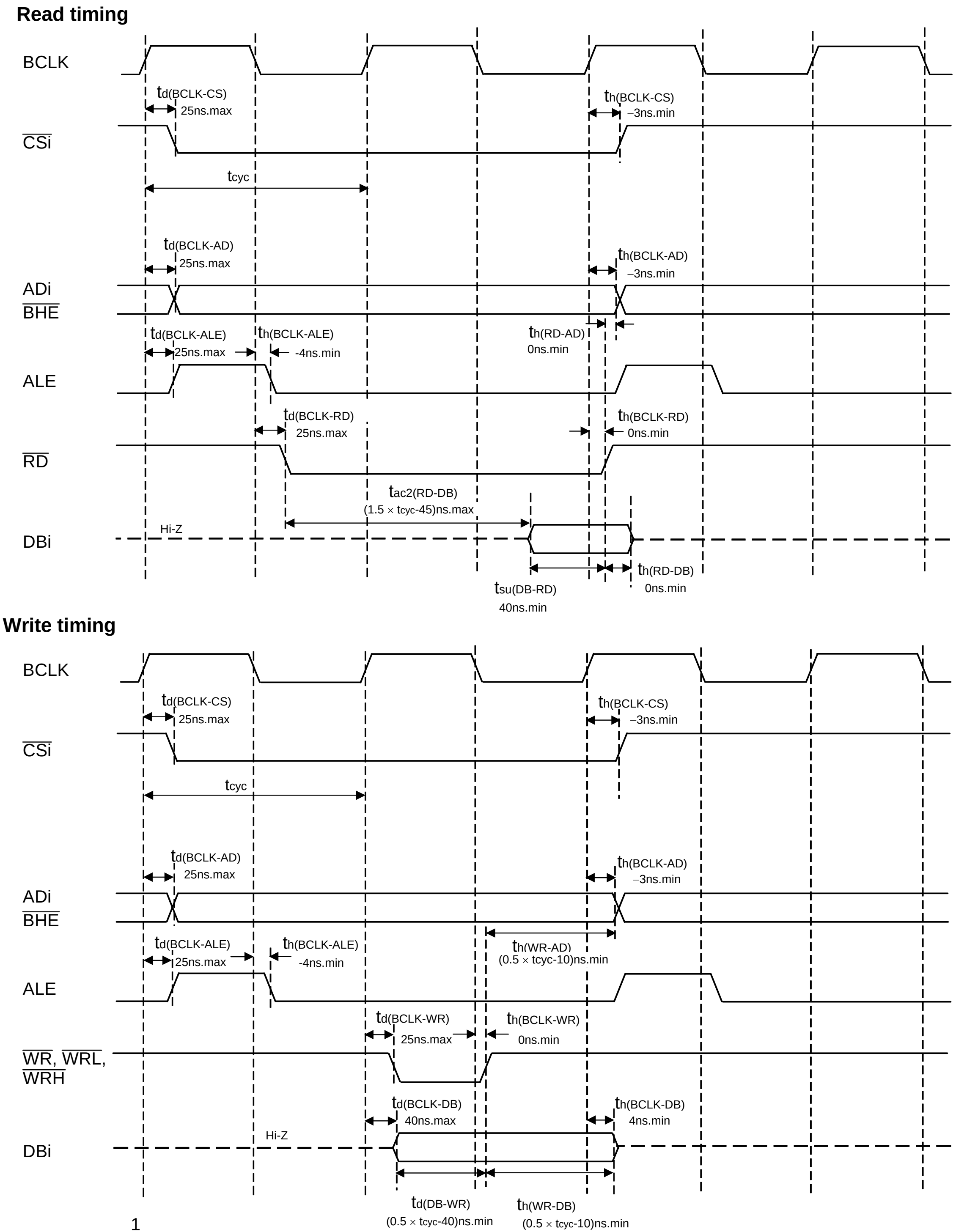
$$\frac{0.5x10^9}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL} / V_{CC1})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC1}$, C = 30pF, R = 1kΩ, hold time of output ”L” level is
$t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC1} / V_{CC1})$
$= 6.7ns.$



$V_{CC1}=V_{CC2}=5V$

Memory Expansion Mode, Microprocessor Mode
(for 1-wait setting and external area access**)**



$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
- $V_{CC1}=V_{CC2}=5V$
- Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
- Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

Figure 5.7 Timing Diagram (5)

VCC1=VCC2=3V

Timing Requirements
(VCC1 = VCC2 = 3V, VSS = 0V, at Topr = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.29 External Clock Input (XIN input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	(NOTE 2)		ns
$t_{w(H)}$	External Clock Input HIGH Pulse Width	(NOTE 3)		ns
$t_{w(L)}$	External Clock Input LOW Pulse Width	(NOTE 3)		ns
t_r	External Clock Rise Time		(NOTE 4)	ns
t_f	External Clock Fall Time		(NOTE 4)	ns

NOTES:

1. The condition is VCC1=VCC2=2.7 to 3.0V.
2. Calculated according to the VCC1 voltage as follows:

$$\frac{10^{-6}}{20 \times V_{CC1} - 44} \text{ [ns]}$$

3. Calculated according to the VCC1 voltage as follows:

$$\frac{10^{-6}}{20 \times V_{CC1} - 44} \times 0.4 \text{ [ns]}$$

4. Calculated according to the VCC1 voltage as follows:

$$-10 \times V_{CC1} + 45 \text{ [ns]}$$

Table 5.30 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (for setting with no wait)		(NOTE 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (for setting with wait)		(NOTE 2)	ns
$t_{su(DB-RD)}$	Data Input Setup Time	50		ns
$t_{su(RDY-BCLK)}$	$\overline{\text{RDY}}$ Input Setup Time	40		ns
$t_{su(HOLD-BCLK)}$	$\overline{\text{HOLD}}$ Input Setup Time	50		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{\text{RDY}}$ Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{\text{HOLD}}$ Input Hold Time	0		ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\text{x}10^{9}}{f(BCLK)} - 60[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5)\text{x}10^{9}}{f(BCLK)} - 60[ns]$$ n is ”2” for 1-wait setting.

$V_{CC1}=V_{CC2}=3V$

Switching Characteristics
(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.44 Memory Expansion and Microprocessor Modes (for 1 wait setting and external area access)

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See **Figure 5.8**		30	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address Output Hold Time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
$t_{d(BCLK-CS)}$	Chip Select Output Delay Time			30	ns
$t_{h(BCLK-CS)}$	Chip Select Output Hold Time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE Signal Output Delay Time			25	ns
$t_{h(BCLK-ALE)}$	ALE Signal Output Hold Time		-4		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			30	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		0		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			30	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(BCLK-DB)}$	Data Output Delay Time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data Output Hold Time (in relation to BCLK) (3)		4		ns
$t_{d(DB-WR)}$	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
th(WR-DB)	Data Output Hold Time (in relation to WR)(3)		(NOTE 2)		ns
$t_{d(BCLK-HLDA)}$	HLDA Output Delay Time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

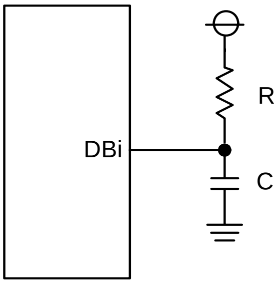
$$\frac{(n-0.5)\text{x}10^9}{f(BCLK)}-40[ns]$$

n is “1” for 1-wait setting, f(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\text{x}10^9}{f(BCLK)}-10[ns]$$

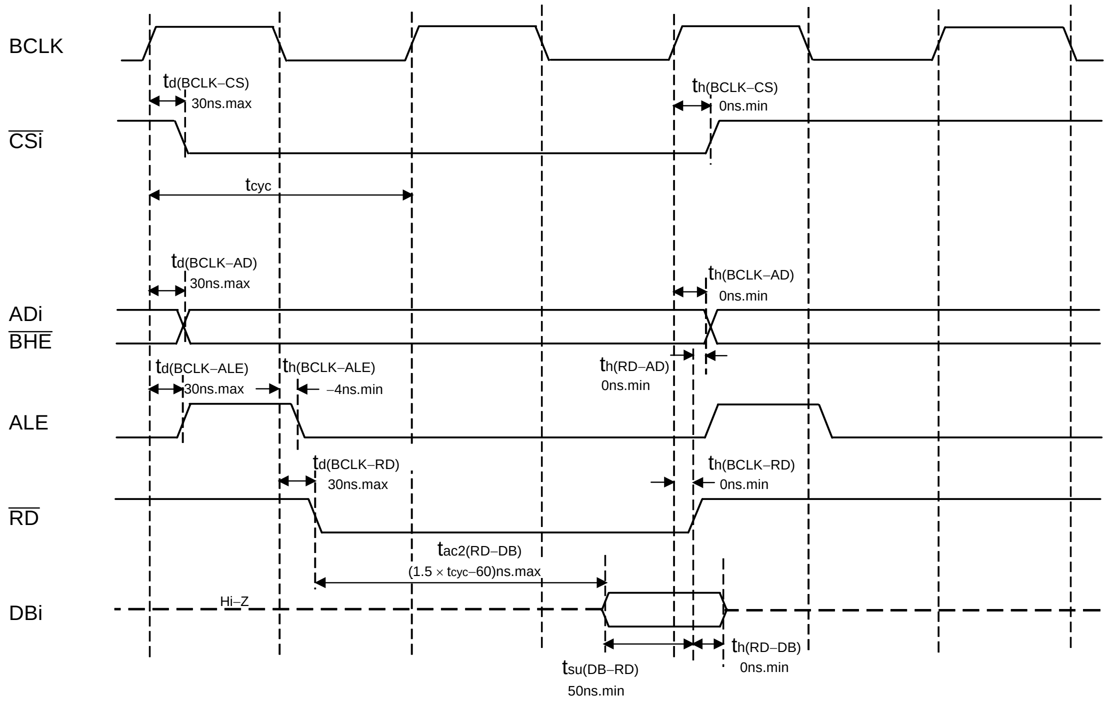
3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \text{ X } \ln(1-V_{OL} / V_{CC1})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC1}$, C = 30pF, R = 1kΩ, hold time of output ”L” level is
$t = -30pF \text{ X } 1k\Omega \text{ X } \ln(1-0.2V_{CC1} / V_{CC1})$
$= 6.7ns.$



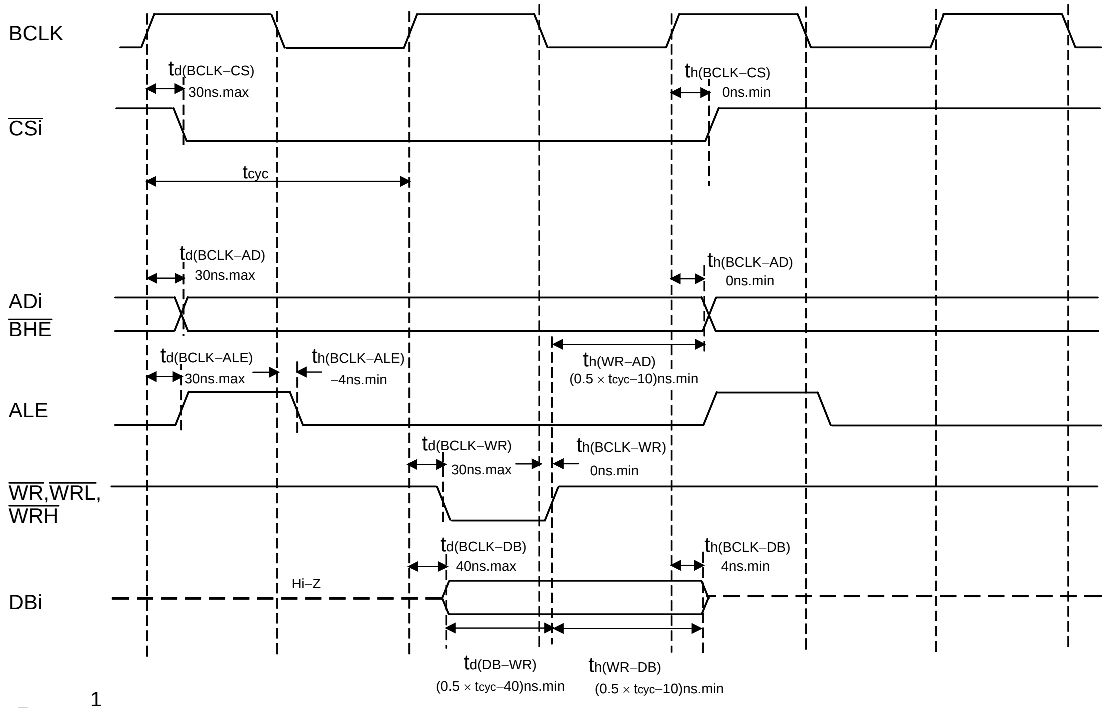
$V_{CC1}=V_{CC2}=3V$

Memory Expansion Mode, Microprocessor Mode
(for 1-wait setting and external area access**)**

Read timing



Write timing



$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

Figure 5.13 Timing Diagram (5)

Rev.	Date	Description	
		Page	Summary
		44	Figure 5.12 Timing Diagram (4) is added.
		45	Figure 5.13 Timing Diagram (5) is added.
1.10	Oct 01, 2005	2	Table 1.1 Performance Outline of M16C/30P Group is partly revised.
		4	Table 1.2 Product List is partly revised.
			Figure 1.2 Type No., Memory Size, and Package is partly revised.
		5	Table 1.3 Product Code of Mask ROM version Version for M16C/30P is added.
			Figure 1.3 Marking Diagram of Mask ROM Version for M16C/30P is added.
		6	Figure 1.4 Marking Diagram of ROM -less Version for M16C/30P is added.
		6	Table 1.4 Product Code of ROM-less version for M16C/30P is added.
		16	Figure 3.1 Memory Map is partly added.
		23	Table 5.2 information is revised.
1.11	May 31, 2006	4	1.4 Product List information is revised.
			Table 1.2 Product List is partly revised.
		5	Figure 1.2 Type No., Memory Size, and Package is partly added.
		7	Table 1.4 Product Code of Flash Memory version and ROM-less version for M16C/30P is partly revised.
			Figure 1.4 Marking Diagram of Flash Memory version and ROM-less Version for M16C/30P (Top View) is partly added.
		17	3. Memory information is revised.
			Figure 3.1 Memory Map is partly revised.
		18	Table 4.1 SFR Information(1) is partly revised.
		19	Table 4.2 SFR Information(2) is partly added.
		23	Table 5.1 Absolute Maximum Ratings information is revised.
		26	Table 5.4 Flash Memory Version Electrical Characteristics is added.
			Table 5.5 Flash Memory Version Program / Erase Voltage and Read Operation Voltage Characteristics is added.
		28	Table 5.7 Electrical Characteristics(1) is partly deleted.
		29	Table 5.8 Electrical Characteristics (2) is partly revised.
		33	Table 5.23 Memory Expansion and Microprocessor Modes NOTES 3 is partly revised.
		34	Table 5.24 Memory Expansion and Microprocessor Modes NOTES 3 is partly revised.
		40	Table 5.25 Electrical Characteristics (1) is partly deleted.
		41	Table 5.26 Electrical Characteristics (2) is partly revised.
		45	Table 5.41 Memory Expansion and Microprocessor Modes NOTES 3 is partly revised.
		46	Table 5.42 Memory Expansion and Microprocessor Modes NOTES 3 is partly revised.

REVISION HISTORY	M16C/30P Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.20	Oct 17, 2006	1	Note is partly deleted.
		2	Table 1.1 Performance Outline of M16C/30P Group is partly added.
		4	Table 1.2 Product List is partly revised.
		5	Figure 1.2 Type No., Memory Size, and Package is added.
		7	Table 1.4 Product Code of One Time Flash version, Flash Memory version, and ROM-less version for M16C/30P is partly added.
		17	Figure 3.1 Memory Map is partly added.
		19	Table 4.2 SFR Information (2) is partly added.
		23	Table 5.1 Absolute Maximum Ratings is partly added.
		27	Table 5.6 One Time Flash Version Electrical Characteristics and Table 5.7 One Time Flash Version Program Voltage and Read Operation Voltage Characteristics is added.
		30	Table 5.10 Electrical Characteristics (2) is partly added.
		42	Table 5.28 Electrical Characteristics (2) is partly added.
1.21	Nov 02 2006	7	Table 1.4 Product Code of One Time Flash version, Flash Memory version, and ROM-less version for M16C/30P is partly revised.
1.22	Mar 30, 2007	4	Table 1.2 Product List (1) is partly revised.
		5	Table 1.3 Product List (2) is partly revised.
		19	Table 4.2 SFR Information (2) is partly revised.

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