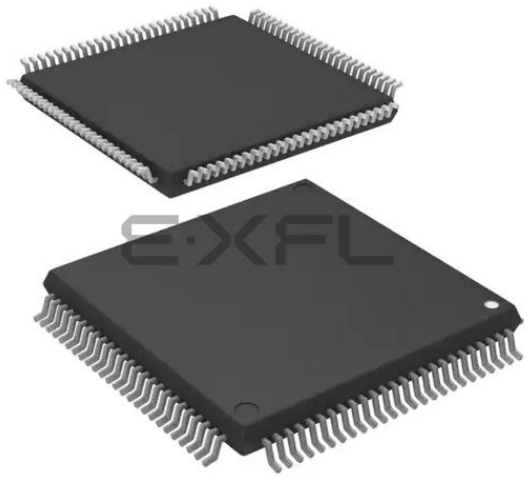
# Renesas Electronics America Inc - M30302FAPGP#U5 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | M16C/60 |
| Core Size | 16-Bit |
| Speed | 16MHz |
| Connectivity | I²C, IEBus, UART/USART |
| Peripherals | DMA, POR, PWM, WDT |
| Number of I/O | 85 |
| Program Memory Size | 96KB (96K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 5K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 18x10b |
| Oscillator Type | External |
| Operating Temperature | -20°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LFQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/m30302fapgp-u5 |

# 1. Overview

The M16C/30P Group of single-chip microcomputers is built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and is packaged in a 100-pin plastic molded QFP.
These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed. In addition, these microcomputers contain a multiplier and DMAC which combined with fast instruction processing capability, make it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

## 1.1 Applications

Audio, cameras, TV, home appliance, office/communications/portable/industrial equipment, etc.

## 1.2 Performance Outline

Table 1.1 lists Performance Outline of M16C/30P Group.

**Table 1.1 Performance Outline of M16C/30P Group**

| Item | | Performance |
|---|---|---|
| CPU | Number of Basic Instructions | 91 instructions |
| | Minimum Instruction Execution Time | 62.5ns(f(XIN)=16MHz, VCC1=VCC2=3.0 to 5.5V, no wait)<br>100ns(f(XIN)=10MHz, VCC1=VCC2=2.7 to 5.5V, no wait) |
| | Operation Mode | Single-chip, memory expansion and microprocessor mode |
| | Memory Space | 1 Mbyte |
| | Memory Capacity | See **Table 1.2 Product List** |
| Peripheral Function | Port | Input/Output : 87 pins, Input : 1 pin |
| | Multifunction Timer | Timer A : 16 bits x 3 channels,<br>Timer B : 16 bits x 3 channels |
| | Serial Interface | 1 channels<br>Clock synchronous, UART, I2CBus(1), IEBus(2)<br>2 channels<br>Clock synchronous, UART, I2CBus(1) |
| | A/D Converter | 10-bit A/D converter: 1 circuit, 18 channels |
| | DMAC | 2 channels |
| | CRC Calculation Circuit | CCITT-CRC |
| | Watchdog Timer | 15 bits x 1 channel (with prescaler) |
| | Interrupt | Internal: 20 sources, External: 7 sources, Software: 4 sources, Priority level: 7 levels |
| | Clock Generating Circuit | 2 circuits<br>Main clock generation circuit (*),<br>Subclock generation circuit (*),<br>(*)Equipped with a built-in feedback resistor. |
| Electric Characteristics | Supply Voltage | VCC1=VCC2=3.0 to 5.5 V (f(XIN)=16MHz)<br>VCC1=VCC2=2.7 to 5.5 V (f(XIN)=10MHz, no wait) |
| | Power Consumption | 10 mA (VCC1=VCC2=5V, f(XIN)=16MHz)<br>8 mA (VCC1=VCC2=3V, f(XIN)=10MHz)<br>1.8 μA (VCC1=VCC2=3V, f(XCIN)=32kHz, wait mode)<br>0.7 μA(VCC1=VCC2=3V, stop mode) |
| One time flash version | Program Supply Voltage | 3.3±0.3 V or 5.0±0.5 V |
| Flash memory version | Program/Erase Supply Voltage | 3.3±0.3 V or 5.0±0.5 V |
| | Program and Erase Endurance | 100 times (all area) |
| Operating Ambient Temperature | | -20 to 85°C, -40 to 85°C |
| Package | | 100-pin plastic mold QFP, LQFP |

NOTES:
1. I2C bus is a registered trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a registered trademark of NEC Electronics Corporation.
3. Use the M16C/30P on VCC1 = VCC2.

## 1.4 Product List

Table 1.2 lists the M16C/30P group products and Figure 1.2 shows the Part No., Memory Size, and Package. Table 1.4 lists Product Code of MASK ROM version for M16C/30P. Figure 1.3 shows the Marking Diagram of Mask ROM Version for M16C/30P (Top View). Table 1.5 lists Product Code of One Time Flash version, Flash Memory version, and ROM-less version for M16C/30P. Figure 1.4 shows the Marking Diagram of One Time Flash version, Flash Memory version, and ROM-less Version for M16C/30P (Top View). Please specify the marking for M16C30P (MASK ROM version) when placing an order for ROM.

**Table 1.2 Product List (1)** **As of March 2007**

| Part No. | ROM Capacity | RAM Capacity | package code (1) | Remarks |
|---|---|---|---|---|
| M30302MAP-XXXFP | 96 Kbytes | 5 Kbytes | PRQP0100JB-A | Mask ROM version |
| M30302MAP-XXXGP | | | PLQP0100KB-A | |
| M30302MCP-XXXFP | 128 Kbytes | | PRQP0100JB-A | |
| M30302MCP-XXXGP | | | PLQP0100KB-A | |
| M30302MDP-XXXFP | 160 Kbytes | 6 Kbytes | PRQP0100JB-A | |
| M30302MDP-XXXGP | | | PLQP0100KB-A | |
| M30302MEP-XXXFP | 192 Kbytes | | PRQP0100JB-A | |
| M30302MEP-XXXGP | | | PLQP0100KB-A | |
| M30302GAPFP | 96 Kbytes | 5 Kbytes | PRQP0100JB-A | One Time Flash version (blank product) |
| M30302GAPGP (D) | | | PLQP0100KB-A | |
| M30302GCPFP | 128 Kbytes | | PRQP0100JB-A | |
| M30302GCPGP (D) | | | PLQP0100KB-A | |
| M30302GDPFP | 160 Kbytes | 6 Kbytes | PRQP0100JB-A | |
| M30302GDPGP (D) | | | PLQP0100KB-A | |
| M30304GDPFP (D) | | 12 Kbytes | PRQP0100JB-A | |
| M30304GDPGP (D) | | | PLQP0100KB-A | |
| M30302GEPFP | 192 Kbytes | 6 Kbytes | PRQP0100JB-A | |
| M30302GEPGP (D) | | | PLQP0100KB-A | |
| M30304GEPFP (D) | | 12 Kbytes | PRQP0100JB-A | |
| M30304GEPGP (D) | | | PLQP0100KB-A | |
| M30302GGPFP (D) | 256 Kbytes | 12 Kbytes | PRQP0100JB-A | |
| M30302GGPGP (D) | | | PLQP0100KB-A | |
| M30302GAP-XXXFP | 96 Kbytes | 5 Kbytes | PRQP0100JB-A | One Time Flash version (factory programmed product) |
| M30302GAPvGP (D) | | | PLQP0100KB-A | |
| M30302GCP-XXXFP | 128 Kbytes | | PRQP0100JB-A | |
| M30302GCP-XXXGP (D) | | | PLQP0100KB-A | |
| M30302GDP-XXXFP | 160 Kbytes | 6 Kbytes | PRQP0100JB-A | |
| M30302GDP-XXXGP (D) | | | PLQP0100KB-A | |
| M30304GDP-XXXFP (D) | | 12 Kbytes | PRQP0100JB-A | |
| M30304GDP-XXXGP (D) | | | PLQP0100KB-A | |
| M30302GEP-XXXFP | 192 Kbytes | 6 Kbytes | PRQP0100JB-A | |
| M30302GEP-XXXGP (D) | | | PLQP0100KB-A | |
| M30304GEP-XXXFP (D) | | 12 Kbytes | PRQP0100JB-A | |
| M30304GEP-XXXGP (D) | | | PLQP0100KB-A | |
| M30302GGP-XXXFP (D) | 256 Kbytes | 12 Kbytes | PRQP0100JB-A | |
| M30302GGP-XXXGP (D) | | | PLQP0100KB-A | |

(D): Under development
(P): Under planning
NOTES:
1. Previous package codes are as follows.
   PRQP0100JB-A : 100P6S-A,
   PLQP0100KB-A : 100P6Q-A
2. Block A (4-Kbytes space) is available in flash memory version.

## 1.5 Pin Configuration

Figures 1.5 to 1.6 show the pin configurations (top view).

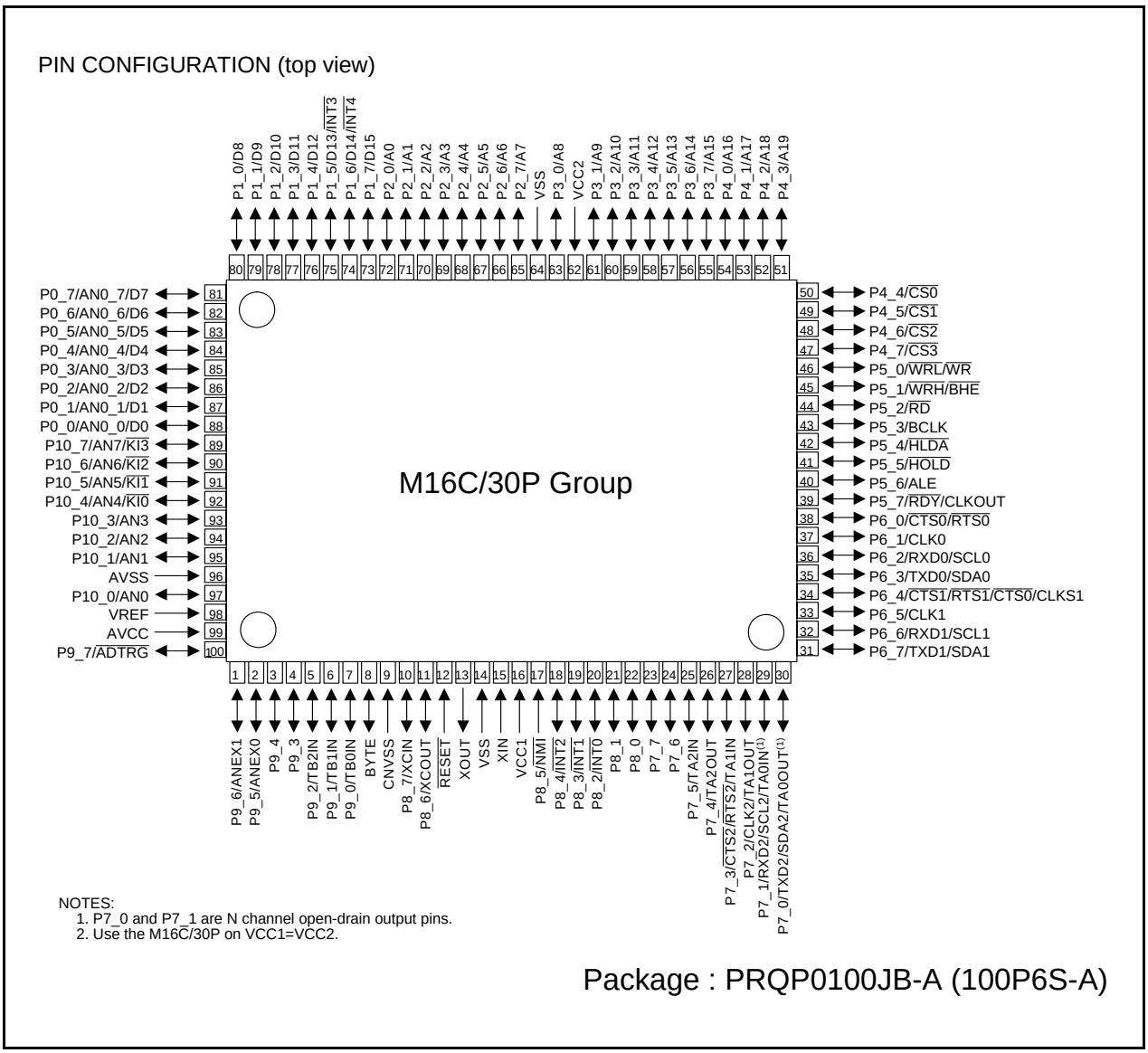



**Figure 1.5 Pin Configuration (Top View)**

## 2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0.
In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.
Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

## 2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

### 2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

### 2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to “0”.

### 2.8.3 Zero Flag (Z Flag)

This flag is set to “1” when an arithmetic operation resulted in 0; otherwise, it is “0”.

### 2.8.4 Sign Flag (S Flag)

This flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, it is “0”.

### 2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is “0” ; register bank 1 is selected when this flag is “1”.

### 2.8.6 Overflow Flag (O Flag)

This flag is set to “1” when the operation resulted in an overflow; otherwise, it is “0”.

### 2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.
Maskable interrupts are disabled when the I flag is “0”, and are enabled when the I flag is “1”. The I flag is cleared to “0” when the interrupt request is accepted.

### 2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is “0”; USP is selected when the U flag is “1”.
The U flag is cleared to “0” when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

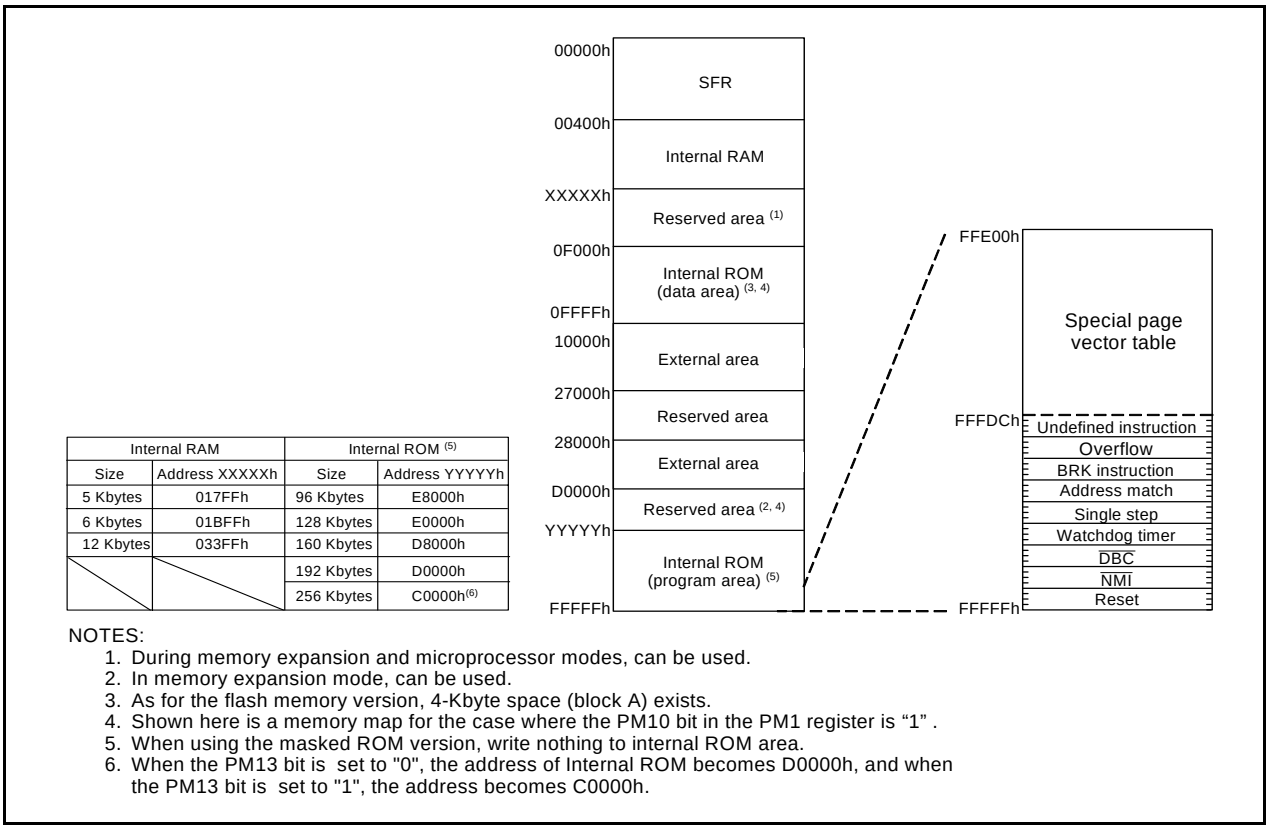
IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has priority greater than IPL, the interrupt is enabled.

### 2.8.10 Reserved Area

When write to this bit, write “0”. When read, its content is indeterminate.

# 3. Memory

Figure 3.1 is a Memory Map of the M16C/30P group. The address space extends the 1 Mbyte from address 00000h to FFFFFh.
The internal ROM is allocated in a lower address direction beginning with address FFFFFh. For example, a 64-Kbyte internal ROM is allocated to the addresses from F0000h to FFFFFh.
The fixed interrupt vector table is allocated to the addresses from FFFDCh to FFFFFh. Therefore, store the start address of each interrupt routine here.
The internal RAM is allocated in an upper address direction beginning with address 00400h. For example, a 5-Kbyte internal RAM is allocated to the addresses from 00400h to 017FFh. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated. The SFR is allocated to the addresses from 00000h to 003FFh. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be used by users.
The special page vector table is allocated to the addresses from FFE00h to FFFDBh. This vector is used by the JMPS or JSRS instruction. For details, refer to the **M16C/60 and M16C/20 Series Software Manual**.




| Internal RAM | | Internal ROM (5) | |
|---|---|---|---|
| Size | Address XXXXXh | Size | Address YYYYYh |
| 5 Kbytes | 017FFh | 96 Kbytes | E8000h |
| 6 Kbytes | 01BFFh | 128 Kbytes | E0000h |
| 12 Kbytes | 033FFh | 160 Kbytes | D8000h |
| | | 192 Kbytes | D0000h |
| | | 256 Kbytes | C0000h(6) |

NOTES:
1. During memory expansion and microprocessor modes, can be used.
2. In memory expansion mode, can be used.
3. As for the flash memory version, 4-Kbyte space (block A) exists.
4. Shown here is a memory map for the case where the PM10 bit in the PM1 register is “1” .
5. When using the masked ROM version, write nothing to internal ROM area.
6. When the PM13 bit is set to "0", the address of Internal ROM becomes D0000h, and when the PM13 bit is set to "1", the address becomes C0000h.

**Figure 3.1 Memory Map**

**Table 4.3 SFR Information (3) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0340h | | | |
| 0341h | | | |
| 0342h | | | |
| 0343h | | | |
| 0344h | | | |
| 0345h | | | |
| 0346h | | | |
| 0347h | | | |
| 0348h | | | |
| 0349h | | | |
| 034Ah | | | |
| 034Bh | | | |
| 034Ch | | | |
| 034Dh | | | |
| 034Eh | | | |
| 034Fh | | | |
| 0350h | | | |
| 0351h | | | |
| 0352h | | | |
| 0353h | | | |
| 0354h | | | |
| 0355h | | | |
| 0356h | | | |
| 0357h | | | |
| 0358h | | | |
| 0359h | | | |
| 035Ah | | | |
| 035Bh | | | |
| 035Ch | | | |
| 035Dh | | | |
| 035Eh | Interrupt Factor Select Register 2 | IFSR2A | 00XXXXXXb |
| 035Fh | Interrupt Factor Select Register | IFSR | 00h |
| 0360h | | | |
| 0361h | | | |
| 0362h | | | |
| 0363h | | | |
| 0364h | | | |
| 0365h | | | |
| 0366h | | | |
| 0367h | | | |
| 0368h | | | |
| 0369h | | | |
| 036Ah | | | |
| 036Bh | | | |
| 036Ch | UART0 Special Mode Register 4 | U0SMR4 | 00h |
| 036Dh | UART0 Special Mode Register 3 | U0SMR3 | 000X0X0Xb |
| 036Eh | UART0 Special Mode Register 2 | U0SMR2 | X0000000b |
| 036Fh | UART0 Special Mode Register | U0SMR | X0000000b |
| 0370h | UART1 Special Mode Register 4 | U1SMR4 | 00h |
| 0371h | UART1 Special Mode Register 3 | U1SMR3 | 000X0X0Xb |
| 0372h | UART1 Special Mode Register 2 | U1SMR2 | X0000000b |
| 0373h | UART1 Special Mode Register | U1SMR | X0000000b |
| 0374h | UART2 Special Mode Register 4 | U2SMR4 | 00h |
| 0375h | UART2 Special Mode Register 3 | U2SMR3 | 000X0X0Xb |
| 0376h | UART2 Special Mode Register 2 | U2SMR2 | X0000000b |
| 0377h | UART2 Special Mode Register | U2SMR | X0000000b |
| 0378h | UART2 Transmit/Receive Mode Register | U2MR | 00h |
| 0379h | UART2 Bit Rate Generator | U2BRG | XXh |
| 037Ah<br>037Bh | UART2 Transmit Buffer Register | U2TB | XXh<br>XXh |
| 037Ch | UART2 Transmit/Receive Control Register 0 | U2C0 | 00001000b |
| 037Dh | UART2 Transmit/Receive Control Register 1 | U2C1 | 00000010b |
| 037Eh<br>037Fh | UART2 Receive Buffer Register | U2RB | XXh<br>XXh |

NOTES:
1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

# 5. Electrical Characteristics

**Table 5.1 Absolute Maximum Ratings**

| Symbol | Parameter | | Condition | Rated Value | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage($V_{CC1}$=$V_{CC2}$) | | $V_{CC1}$=$V_{CC2}$=AVcc | –0.3 to 6.5 | V |
| AVcc | Analog Supply Voltage | | $V_{CC1}$=$V_{CC2}$=AVcc | –0.3 to 6.5 | V |
| $V_I$ | Input Voltage | $\overline{\text{RESET}}$, CNVSS, BYTE, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, VREF, XIN | | –0.3 to $V_{CC}$+0.3 | V |
| | | P7_0, P7_1 | | –0.3 to 6.5 | V |
| $V_O$ | Output Voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, XOUT | | –0.3 to $V_{CC}$+0.3 | V |
| | | P7_0, P7_1 | | –0.3 to 6.5 | V |
| $P_d$ | Power Dissipation | | –40°C<$T_{opr}$≤85°C | 300 | mW |
| $T_{opr}$ | Operating Ambient Temperature | When the Microcomputer is Operating | | –20 to 85 / –40 to 85 | °C |
| | | One Time Flash Program Erase | | 0 to 60 | |
| | | Flash Program Erase | | 0 to 60 | |
| $T_{stg}$ | Storage Temperature | | | –65 to 150 | °C |

**Table 5.2 Recommended Operating Conditions** (1)

| Symbol | Parameter | | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{CC}$ | Supply Voltage ($V_{CC1}$=$V_{CC2}$) | | 2.7 | 5.0 | 5.5 | V |
| AVcc | Analog Supply Voltage | | | Vcc | | V |
| Vss | Supply Voltage | | | 0 | | V |
| AVss | Analog Supply Voltage | | | 0 | | V |
| $V_{IH}$ | HIGH Input Voltage | P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7 | 0.8Vcc | | Vcc | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode) | 0.8Vcc | | Vcc | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor mode) | 0.5Vcc | | Vcc | V |
| | | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, $\overline{\text{RESET}}$, CNVSS, BYTE | 0.8Vcc | | Vcc | V |
| | | P7_0, P7_1 | 0.8Vcc | | 6.5 | V |
| $V_{IL}$ | LOW Input Voltage | P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7 | 0 | | 0.2Vcc | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode) | 0 | | 0.2Vcc | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor mode) | 0 | | 0.16Vcc | V |
| | | P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, XIN, $\overline{\text{RESET}}$, CNVSS, BYTE | 0 | | 0.2Vcc | V |
| $I_{OH(peak)}$ | HIGH Peak Output Current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | | | −10.0 | mA |
| $I_{OH(avg)}$ | HIGH Average Output Current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | | | −5.0 | mA |
| $I_{OL(peak)}$ | LOW Peak Output Current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | | | 10.0 | mA |
| $I_{OL(avg)}$ | LOW Average Output Current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | | | 5.0 | mA |
| f(XIN) | Main Clock Input Oscillation Frequency (4) | Vcc=3.0V to 5.5V | 0 | | 16 | MHz |
| | | Vcc=2.7V to 3.0V | 0 | | 20×$V_{CC1}$−44 | MHz |
| f(XCIN) | Sub-Clock Oscillation Frequency | | | 32.768 | 50 | kHz |
| f(BCLK) | CPU Operation Clock | | 0 | | 16 | MHz |

NOTES:
1. Referenced to $V_{CC1}$ = $V_{CC2}$ = 2.7 to 5.5V at $T_{opr}$ = −20 to 85°C / −40 to 85°C unless otherwise specified.
2. The Average Output Current is the mean value within 100ms.
3. The total $I_{OL(peak)}$ for ports P0, P1, P2, P8_6, P8_7, P9 and P10 must be 80mA max. The total $I_{OL(peak)}$ for ports P3, P4, P5, P6, P7 and P8_0 to P8_4 must be 80mA max. The total $I_{OH(peak)}$ for ports P0, P1, and P2 must be −40mA max. The total $I_{OH(peak)}$ for ports P3, P4 and P5 must be −40mA max. The total $I_{OH(peak)}$ for ports P6, P7, and P8_0 to P8_4 must be −40mA max.
   The total $I_{OH(peak)}$ for ports P8_6, P8_7 and P9 must be −40mA max. Set Average Output Current to 1/2 of peak.
4. Relationship between main clock oscillation frequency, and supply voltage.

Main clock input oscillation frequency

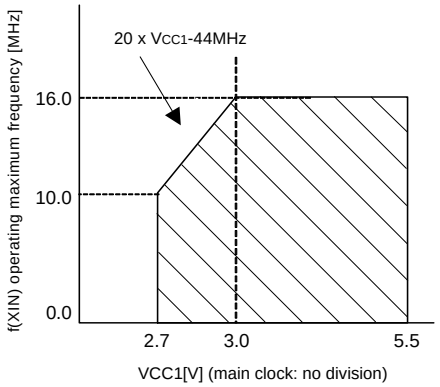


**Table 5.4 Flash Memory Version Electrical Characteristics (1)**

| Symbol | Parameter | | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program and Erase Endurance (2) | | 100(3) | | | cycle |
| – | Word Program Time ($V_{CC1}$=5.0V) | | | 25 | 200 | µs |
| – | Lock Bit Program Time | | | 25 | 200 | µs |
| – | Block Erase Time ($V_{CC1}$=5.0V) | 4-Kbyte block | | 0.3 | 4 | s |
| – | | 8-Kbyte block | | 0.3 | 4 | s |
| – | | 32-Kbyte block | | 0.5 | 4 | s |
| – | | 64-Kbyte block | | 0.8 | 4 | s |
| $t_{PS}$ | Flash Memory Circuit Stabilization Wait Time | | | | 15 | µs |
| – | Data Hold Time (4) | | 10 | | | year |

NOTES:
1. Referenced to $V_{CC1}$=4.5 to 5.5V, 3.0 to 3.6V at Topr = 0 to 60 °C (U3, U5) unless otherwise specified.
2. Program and Erase Endurance refers to the number of times a block erase can be performed.
   If the program and erase endurance is 100, each block can be erased 100 times.
   For example, if a 4 Kbytes block A is erased after writing 1 word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data cannot be written to the same address more than once without erasing the block. (Rewrite prohibited)
3. Maximum number of E/W cycles for which operation is guaranteed.
4. Topr = -40 to 85 °C (U3) / -20 to 85 °C (U5).

**Table 5.5 Flash Memory Version Program / Erase Voltage and Read Operation Voltage Characteristics**

| Flash Program, Erase Voltage | Flash Read Operation Voltage |
|---|---|
| $V_{CC1}$ = 3.3 ± 0.3 V or 5.0 ± 0.5 ($T_{opr}$ = 0°C to 60°C ) | $V_{CC1}$=2.7 to 5.5 V ($T_{opr}$ = -40°C to 85°C (U3)<br>-20°C to 85°C (U5)) |

**Table 5.10 Electrical Characteristics (2)** (1)

| Symbol | Parameter | | Measuring Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $I_{CC}$ | Power Supply Current ($V_{CC1}$=$V_{CC2}$=4.0V to 5.5V) | In single-chip mode, the output pins are open and other pins are $V_{SS}$ | Mask ROM | f(XIN)=16MHz No division | | 10 | 15 | mA |
| | | | One Time Flash | f(XIN)=16MHz, No division | | 10 | 18 | mA |
| | | | Flash Memory | f(XIN)=16MHz, No division | | 12 | 18 | mA |
| | | | One Time Flash | f(XIN)=10MHz, VCC1=5.0V | | 15 | | mA |
| | | | Flash Memory Program | f(XIN)=10MHz, VCC1=5.0V | | 15 | | mA |
| | | | Flash Memory Erase | f(XIN)=10MHz, VCC1=5.0V | | 25 | | mA |
| | | | Mask ROM | f(XCIN)=32kHz Low power dissipation mode, ROM (3) | | 25 | | µA |
| | | | One Time Flash | f(XCIN)=32kHz Low power dissipation mode, RAM (3) | | 25 | | µA |
| | | | | f(XCIN)=32kHz Low power dissipation mode, Flash Memory (3) | | 350 | | µA |
| | | | Flash Memory | f(XCIN)=32kHz Low power dissipation mode, RAM (3) | | 25 | | µA |
| | | | | f(XCIN)=32kHz Low power dissipation mode, Flash Memory (3) | | 420 | | µA |
| | | | Mask ROM One Time Flash Flash Memory | f(XCIN)=32kHz Wait mode (2), Oscillation capability High | | 7.5 | | µA |
| | | | | f(XCIN)=32kHz Wait mode (2), Oscillation capability Low | | 2.0 | | µA |
| | | | | Stop mode Topr =25°C | | 0.8 | 3.0 | µA |

NOTES:
1. Referenced to $V_{CC1}$=$V_{CC2}$=4.2 to 5.5V, $V_{SS}$ = 0V at $T_{opr}$ = –20 to 85°C / –40 to 85°C, f(XIN)=16MHz unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.

# $V_{CC1}=V_{CC2}=5V$

## Timing Requirements

**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

### Table 5.19 Timer B Input (Counter Input in Event Counter Mode)

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time (counted on one edge) | 100 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width (counted on one edge) | 40 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width (counted on one edge) | 40 | | ns |
| $t_{c(TB)}$ | TBiIN Input Cycle Time (counted on both edges) | 200 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width (counted on both edges) | 80 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width (counted on both edges) | 80 | | ns |

### Table 5.20 Timer B Input (Pulse Period Measurement Mode)

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time | 400 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width | 200 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width | 200 | | ns |

### Table 5.21 Timer B Input (Pulse Width Measurement Mode)

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time | 400 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width | 200 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width | 200 | | ns |

### Table 5.22 A/D Trigger Input

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(AD)}$ | $\overline{\text{ADTRG}}$ Input Cycle Time | 1000 | | ns |
| $t_{w(ADL)}$ | $\overline{\text{ADTRG}}$ input LOW Pulse Width | 125 | | ns |

### Table 5.23 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi Input Cycle Time | 200 | | ns |
| $t_{w(CKH)}$ | CLKi Input HIGH Pulse Width | 100 | | ns |
| $t_{w(CKL)}$ | CLKi Input LOW Pulse Width | 100 | | ns |
| $t_{d(C-Q)}$ | TXDi Output Delay Time | | 80 | ns |
| $t_{h(C-Q)}$ | TXDi Hold Time | 0 | | ns |
| $t_{su(D-C)}$ | RXDi Input Setup Time | 70 | | ns |
| $t_{h(C-D)}$ | RXDi Input Hold Time | 90 | | ns |

### Table 5.24 External Interrupt $\overline{\text{INTi}}$ Input

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(INH)}$ | $\overline{\text{INTi}}$ Input HIGH Pulse Width | 250 | | ns |
| $t_{w(INL)}$ | $\overline{\text{INTi}}$ Input LOW Pulse Width | 250 | | ns |

$V_{CC1}=V_{CC2}=5V$

**Switching Characteristics**
**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.26 Memory Expansion and Microprocessor Modes (for 1 wait setting and external area access)**

| Symbol | Parameter | | Standard | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $t_{d(BCLK-AD)}$ | Address Output Delay Time | See **Figure 5.2** | | 25 | ns |
| $t_{h(BCLK-AD)}$ | Address Output Hold Time (in relation to BCLK) | | –3 | | ns |
| $t_{h(RD-AD)}$ | Address Output Hold Time (in relation to RD) | | 0 | | ns |
| $t_{h(WR-AD)}$ | Address Output Hold Time (in relation to WR) | | (NOTE 2) | | ns |
| $t_{d(BCLK-CS)}$ | Chip Select Output Delay Time | | | 25 | ns |
| $t_{h(BCLK-CS)}$ | Chip Select Output Hold Time (in relation to BCLK) | | –3 | | ns |
| $t_{d(BCLK-ALE)}$ | ALE Signal Output Delay Time | | | 15 | ns |
| $t_{h(BCLK-ALE)}$ | ALE Signal Output Hold Time | | –4 | | ns |
| $t_{d(BCLK-RD)}$ | RD Signal Output Delay Time | | | 25 | ns |
| $t_{h(BCLK-RD)}$ | RD Signal Output Hold Time | | 0 | | ns |
| $t_{d(BCLK-WR)}$ | WR Signal Output Delay Time | | | 25 | ns |
| $t_{h(BCLK-WR)}$ | WR Signal Output Hold Time | | 0 | | ns |
| $t_{d(BCLK-DB)}$ | Data Output Delay Time (in relation to BCLK) | | | 40 | ns |
| $t_{h(BCLK-DB)}$ | Data Output Hold Time (in relation to BCLK) (3) | | 4 | | ns |
| $t_{d(DB-WR)}$ | Data Output Delay Time (in relation to WR) | | (NOTE 1) | | ns |
| $t_{h(WR-DB)}$ | Data Output Hold Time (in relation to WR)(3) | | (NOTE 2) | | ns |
| $t_{d(BCLK-HLDA)}$ | HLDA Output Delay Time | | | 40 | ns |

NOTES:

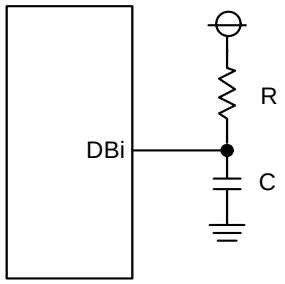
1. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5)\times 10^9}{f(BCLK)} - 40[ns]$$ n is “1” for 1-wait setting, f(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
t = –CR X ln (1–$V_{OL}$ / $V_{CC1}$)
by a circuit of the right figure.
For example, when $V_{OL}$ = 0.2$V_{CC1}$, C = 30pF, R = 1kΩ, hold time of output ”L” level is
t = –30pF X 1kΩ X ln(1–0.2$V_{CC1}$ / $V_{CC1}$)
= 6.7ns.



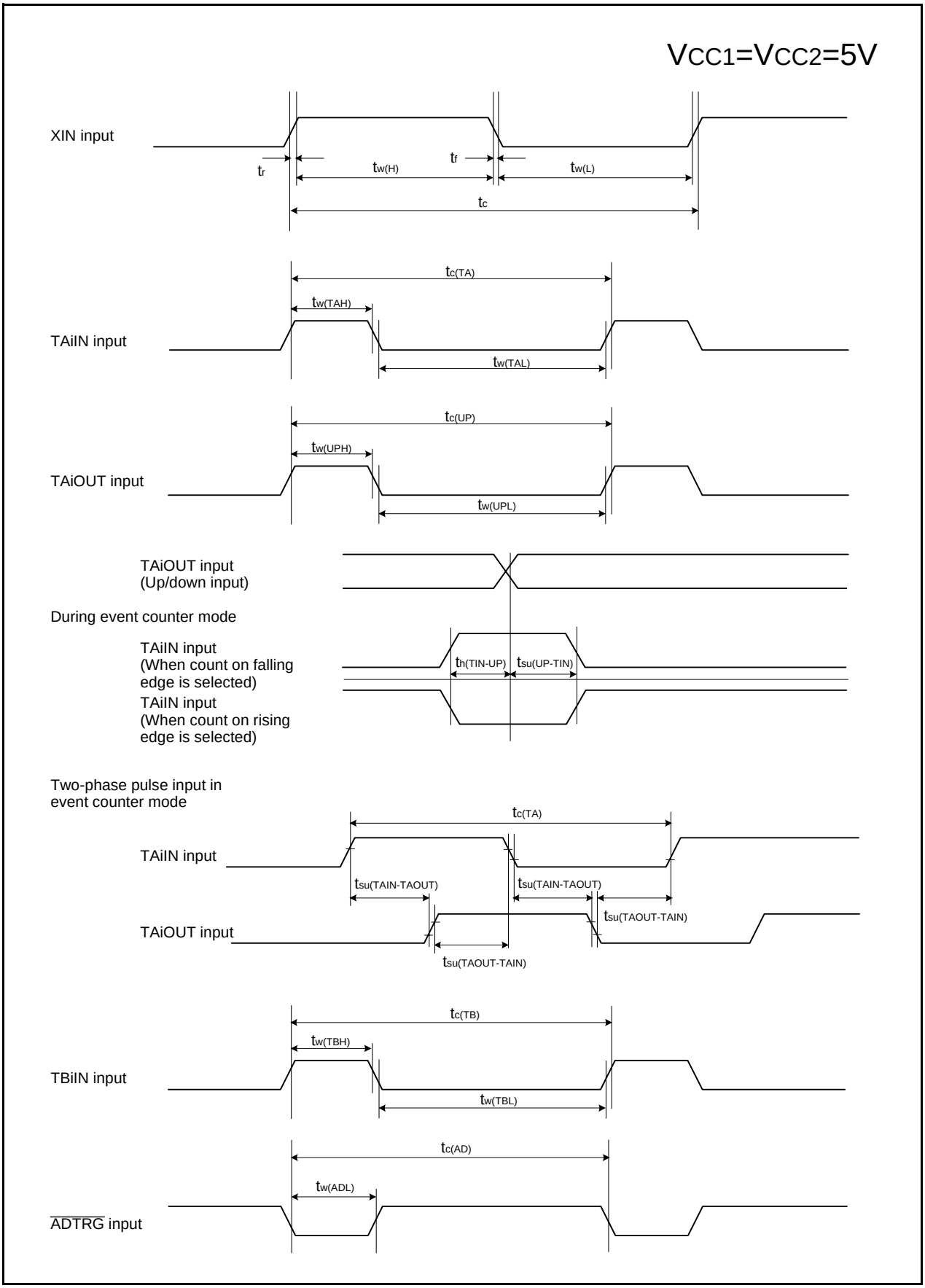
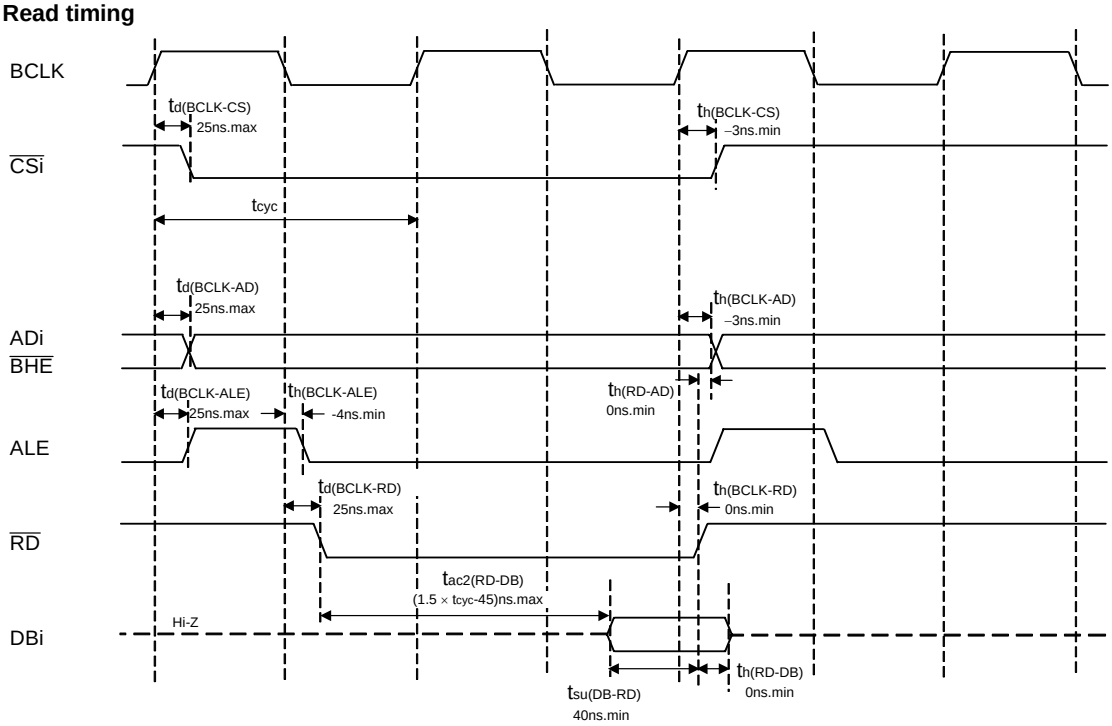



**Figure 5.3 Timing Diagram (1)**

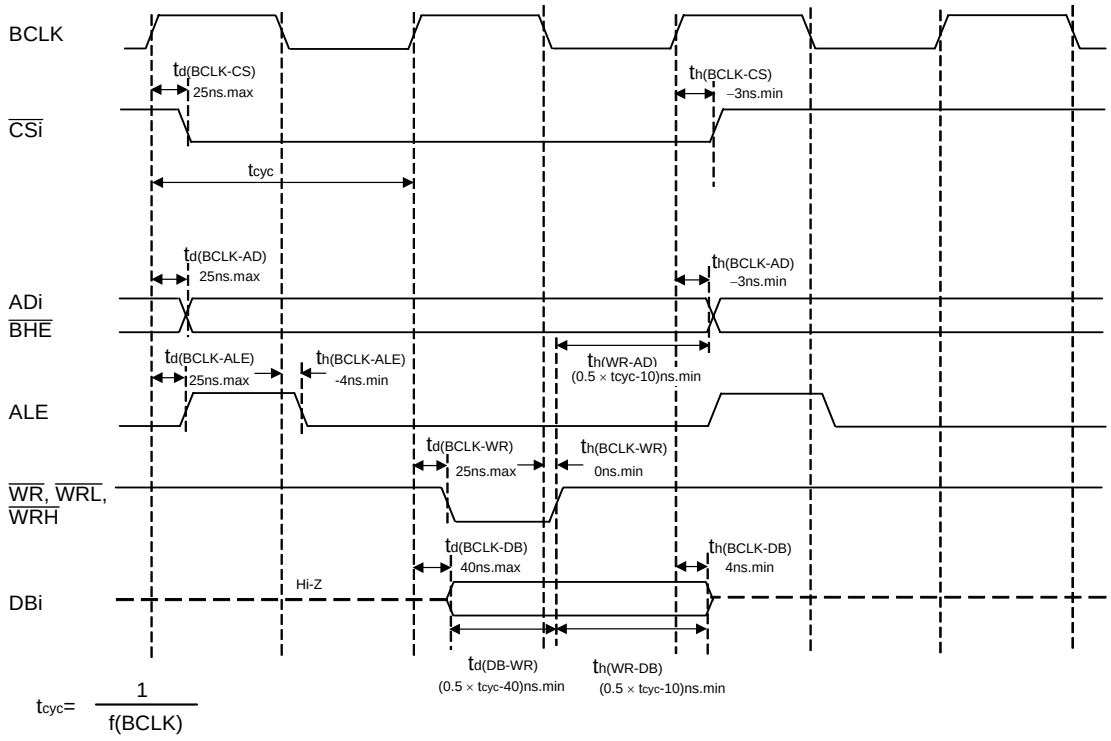
$V_{CC1}=V_{CC2}=5V$

**Memory Expansion Mode, Microprocessor Mode**
**(**for 1-wait setting and external area access**)**

**Read timing**




**Write timing**




$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
· Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

**Figure 5.7 Timing Diagram (5)**

# $V_{CC1}=V_{CC2}=3V$

## Timing Requirements

**($V_{CC1}$ = $V_{CC2}$ = 3V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

### Table 5.29 External Clock Input (XIN input)

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_c$ | External Clock Input Cycle Time | (NOTE 2) | | ns |
| $t_{w(H)}$ | External Clock Input HIGH Pulse Width | (NOTE 3) | | ns |
| $t_{w(L)}$ | External Clock Input LOW Pulse Width | (NOTE 3) | | ns |
| $t_r$ | External Clock Rise Time | | (NOTE 4) | ns |
| $t_f$ | External Clock Fall Time | | (NOTE 4) | ns |

NOTES:

1. The condition is $V_{CC1}$=$V_{CC2}$=2.7 to 3.0V.
2. Calculated according to the $V_{CC1}$ voltage as follows:

$$\frac{10^{-6}}{20 \times V_{CC1} - 44} \text{ [ns]}$$

3. Calculated according to the $V_{CC1}$ voltage as follows:

$$\frac{10^{-6}}{20 \times V_{CC1} - 44} \times 0.4 \text{ [ns]}$$

4. Calculated according to the $V_{CC1}$ voltage as follows:

$$-10 \times V_{CC1} + 45 \text{ [ns]}$$

### Table 5.30 Memory Expansion Mode and Microprocessor Mode

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{ac1(RD-DB)}$ | Data Input Access Time (for setting with no wait) | | (NOTE 1) | ns |
| $t_{ac2(RD-DB)}$ | Data Input Access Time (for setting with wait) | | (NOTE 2) | ns |
| $t_{su(DB-RD)}$ | Data Input Setup Time | 50 | | ns |
| $t_{su(RDY-BCLK)}$ | $\overline{RDY}$ Input Setup Time | 40 | | ns |
| $t_{su(HOLD-BCLK)}$ | $\overline{HOLD}$ Input Setup Time | 50 | | ns |
| $t_{h(RD-DB)}$ | Data Input Hold Time | 0 | | ns |
| $t_{h(BCLK-RDY)}$ | $\overline{RDY}$ Input Hold Time | 0 | | ns |
| $t_{h(BCLK-HOLD)}$ | $\overline{HOLD}$ Input Hold Time | 0 | | ns |

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 60 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(BCLK)} - 60 \text{ [ns]}$$ n is "2" for 1-wait setting.

# $V_{CC1}=V_{CC2}=3V$

## Switching Characteristics

**($V_{CC1}$ = $V_{CC2}$ = 3V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.43 Memory Expansion and Microprocessor Modes (for setting with no wait)**

| Symbol | Parameter | | Standard | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| td(BCLK-AD) | Address Output Delay Time | See **Figure 5.8** | | 30 | ns |
| th(BCLK-AD) | Address Output Hold Time (in relation to BCLK) | | 0 | | ns |
| th(RD-AD) | Address Output Hold Time (in relation to RD) | | 0 | | ns |
| th(WR-AD) | Address Output Hold Time (in relation to WR) | | (NOTE 2) | | ns |
| td(BCLK-CS) | Chip Select Output Delay Time | | | 30 | ns |
| th(BCLK-CS) | Chip Select Output Hold Time (in relation to BCLK) | | 0 | | ns |
| td(BCLK-ALE) | ALE Signal Output Delay Time | | | 25 | ns |
| th(BCLK-ALE) | ALE Signal Output Hold Time | | –4 | | ns |
| td(BCLK-RD) | RD Signal Output Delay Time | | | 30 | ns |
| th(BCLK-RD) | RD Signal Output Hold Time | | 0 | | ns |
| td(BCLK-WR) | WR Signal Output Delay Time | | | 30 | ns |
| th(BCLK-WR) | WR Signal Output Hold Time | | 0 | | ns |
| td(BCLK-DB) | Data Output Delay Time (in relation to BCLK) | | | 40 | ns |
| th(BCLK-DB) | Data Output Hold Time (in relation to BCLK) (3) | | 4 | | ns |
| td(DB-WR) | Data Output Delay Time (in relation to WR) | | (NOTE 1) | | ns |
| th(WR-DB) | Data Output Hold Time (in relation to WR) (3) | | (NOTE 2) | | ns |
| td(BCLK-HLDA) | HLDA Output Delay Time | | | 40 | ns |

NOTES:

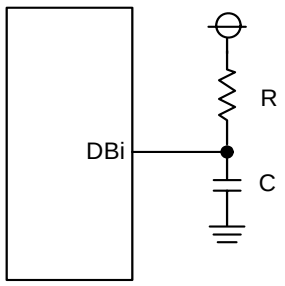
1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times10^{9}}{f(BCLK)} - 40[ns]$$ f(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times10^{9}}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
   Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
   Hold time of data bus is expressed in
   $t = -CR \times \ln(1 - V_{OL} / V_{CC1})$
   by a circuit of the right figure.
   For example, when $V_{OL}$ = 0.2$V_{CC1}$, C = 30pF, R = 1kΩ, hold time of output "L" level is
   $t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC1} / V_{CC1})$
   = 6.7ns.



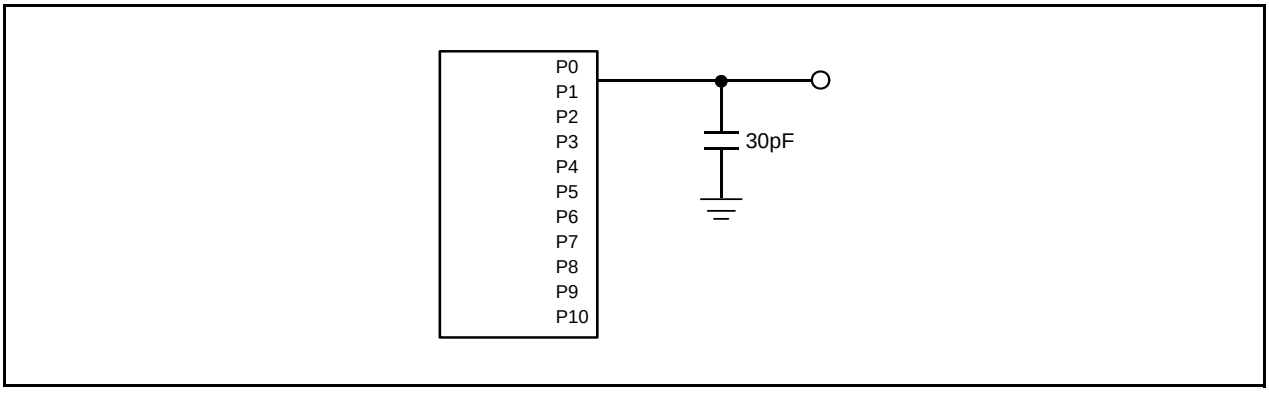



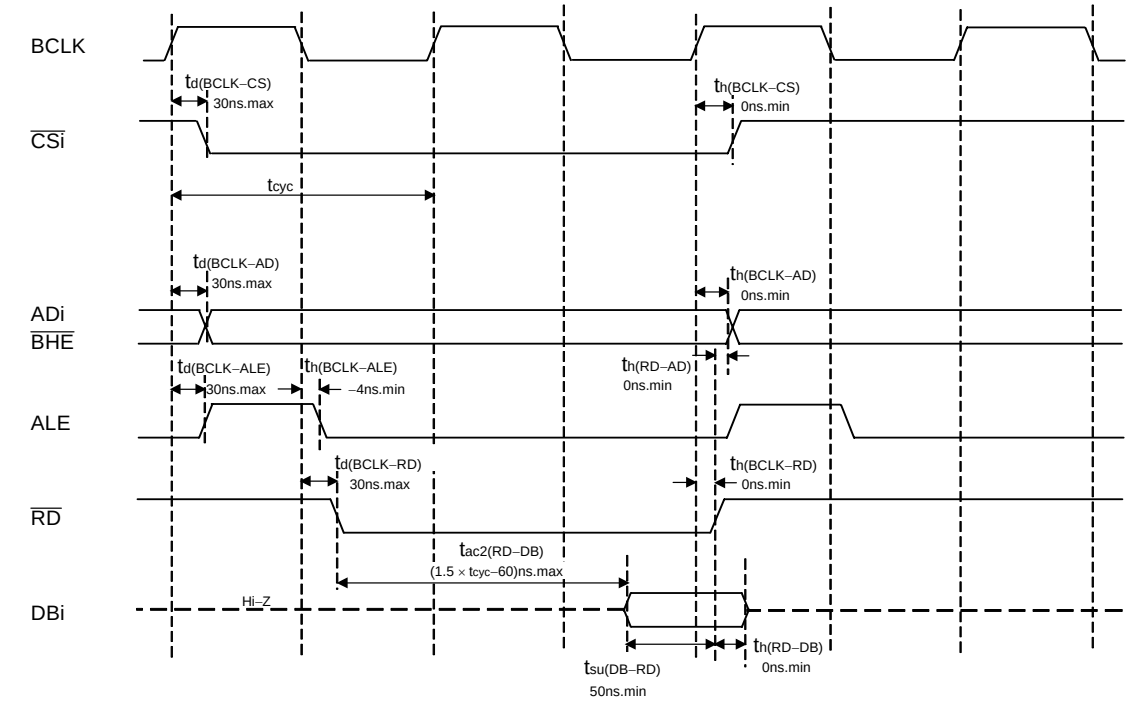

**Figure 5.8 Ports P0 to P10 Measurement Circuit**

## Memory Expansion Mode, Microprocessor Mode

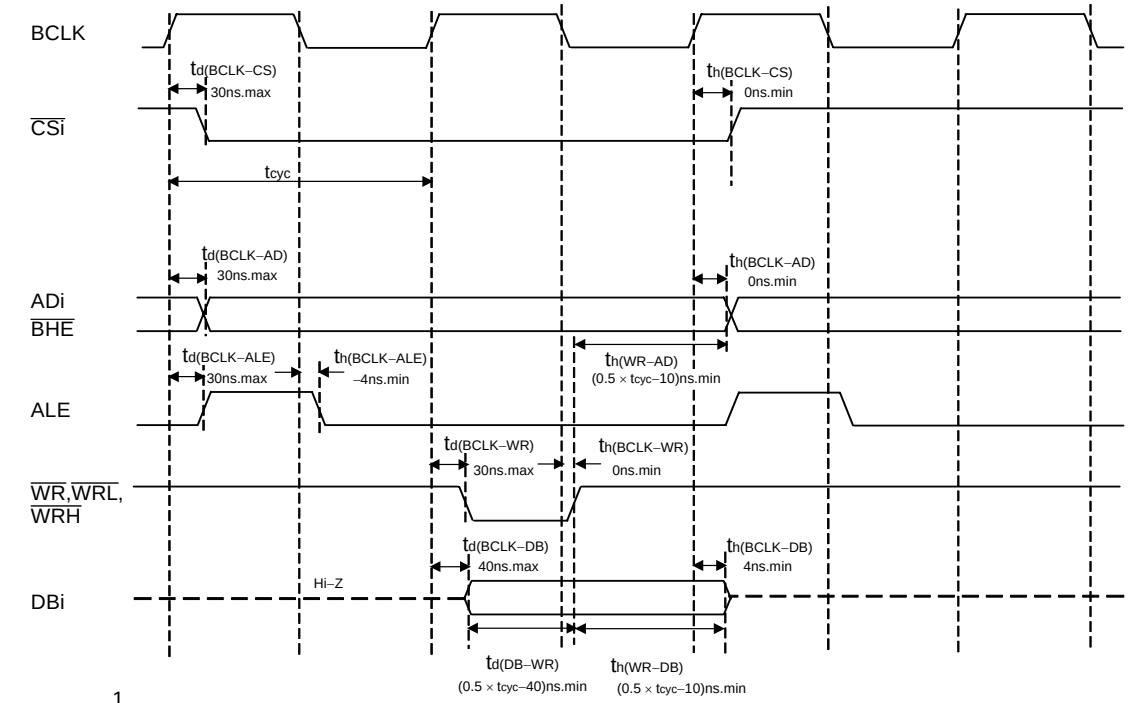
(for 1-wait setting and external area access)

$V_{CC1}=V_{CC2}=3V$

**Read timing**




**Write timing**




$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

**Figure 5.13 Timing Diagram (5)**

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