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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	16MHz
Connectivity	I²C, IEBus, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	5K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 18x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30302fcpfp-u3

1. Overview

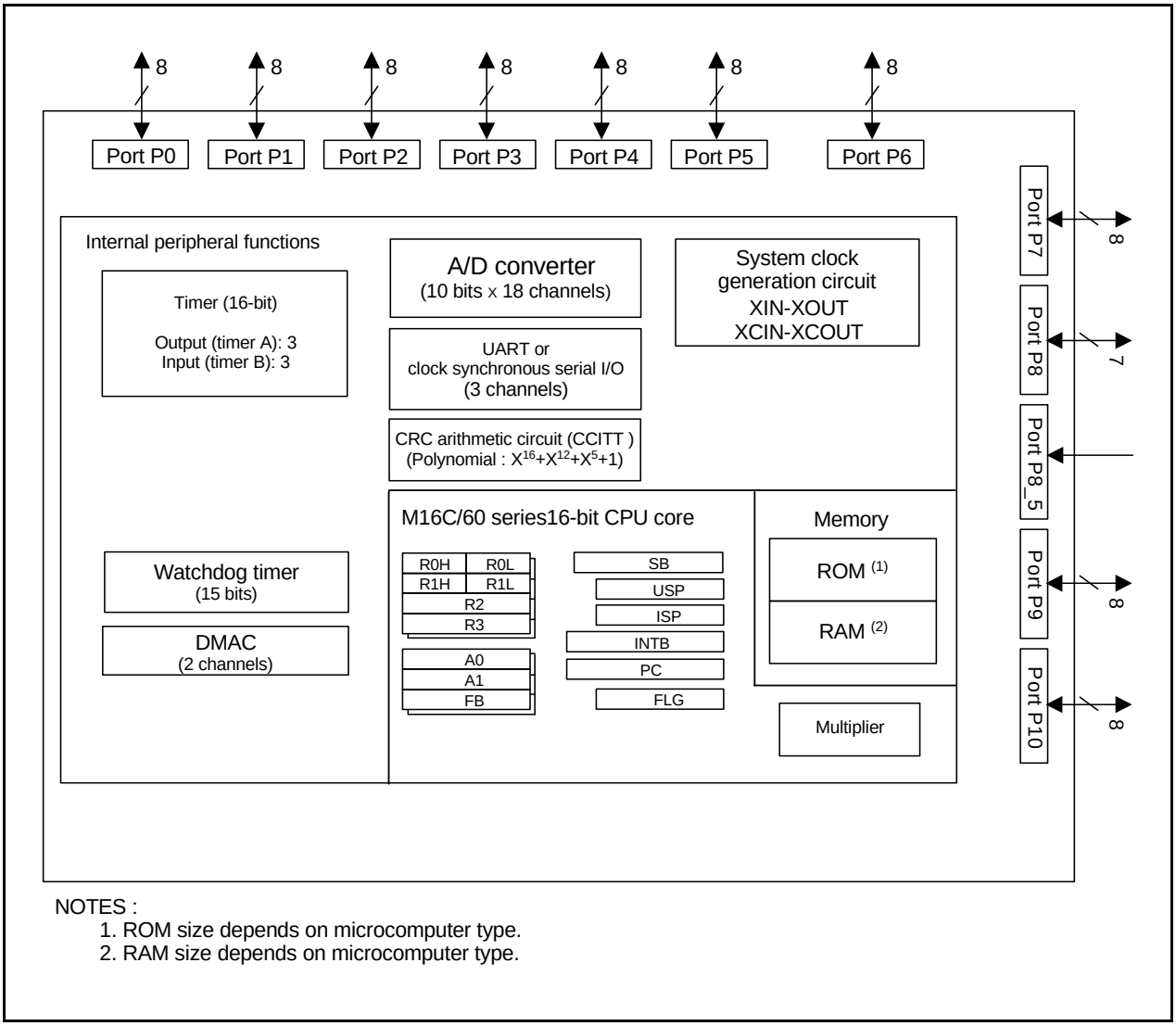
The M16C/30P Group of single-chip microcomputers is built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and is packaged in a 100-pin plastic molded QFP.
These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed. In addition, these microcomputers contain a multiplier and DMAC which combined with fast instruction processing capability, make it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

Audio, cameras, TV, home appliance, office/communications/portable/industrial equipment, etc.

1.3 Block Diagram

Figure 1.1 is a M16C/30P Group Block Diagram.



NOTES :
1. ROM size depends on microcomputer type.
2. RAM size depends on microcomputer type.

Figure 1.1 M16C/30P Group Block Diagram

Table 1.5 Product Code of One Time Flash version, Flash Memory version, and ROM-less version for M16C/30P

	Product Code	Package	Internal ROM		Operating Ambient Temperature
			Program and Erase Endurance	Temperature Range	
One Time Flash version	U3	Lead-free	0	0°C to 60°C	-40°C to 85°C
	U5				-20°C to 85°C
Flash Memory version	U3	Lead-free	100	0°C to 60°C	-40°C to 85°C
	U5				-20°C to 85°C
ROM-less version	U3	Lead-free	–	–	-40°C to 85°C
	U5				-20°C to 85°C

NOTES:The one time flash version can be written once only.

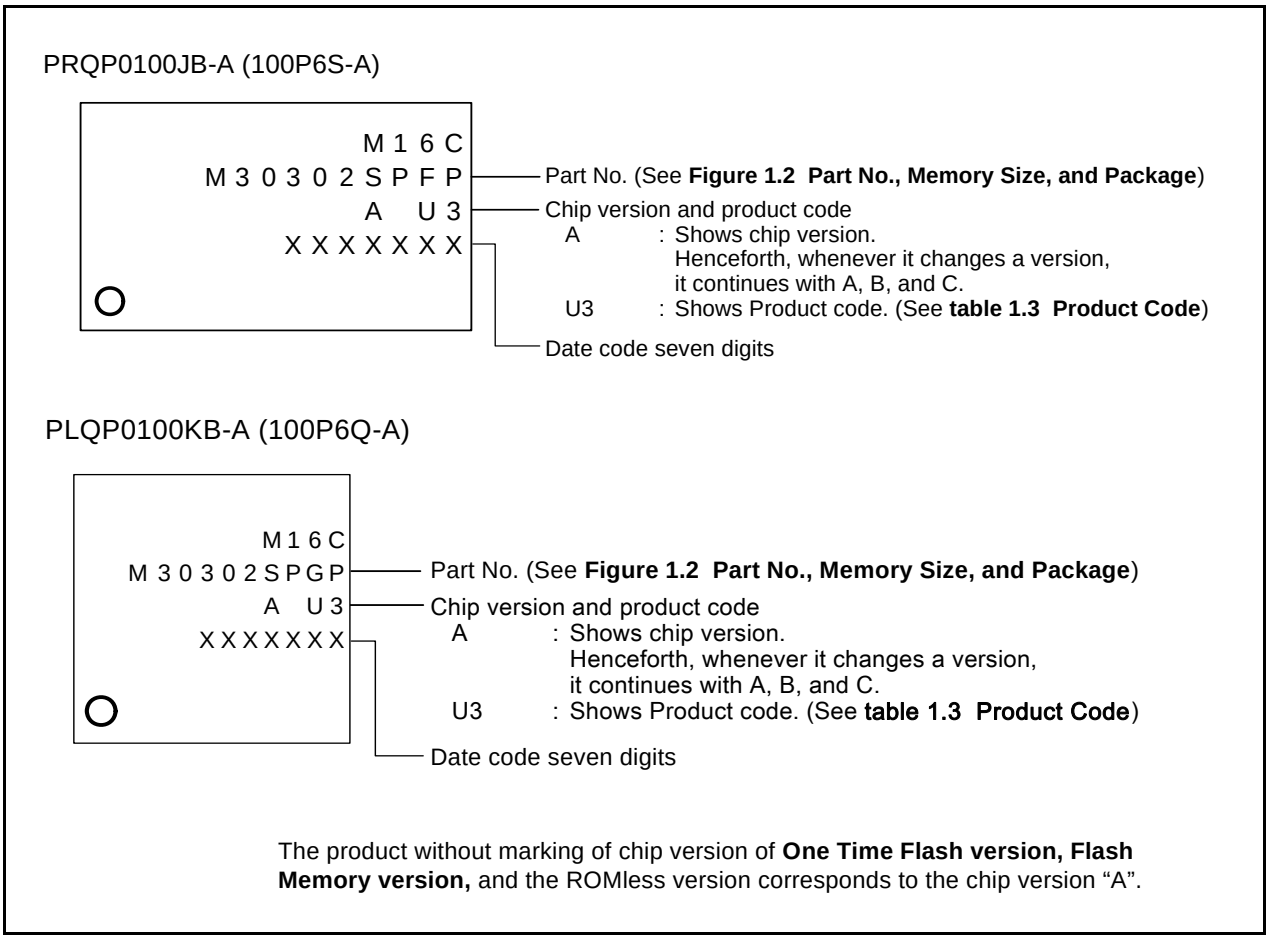


Figure 1.4 Marking Diagram of One Time Flash version, Flash Memory version, and ROM-less Version for M16C/30P (Top View)

1.5 Pin Configuration

Figures 1.5 to 1.6 show the pin configurations (top view).

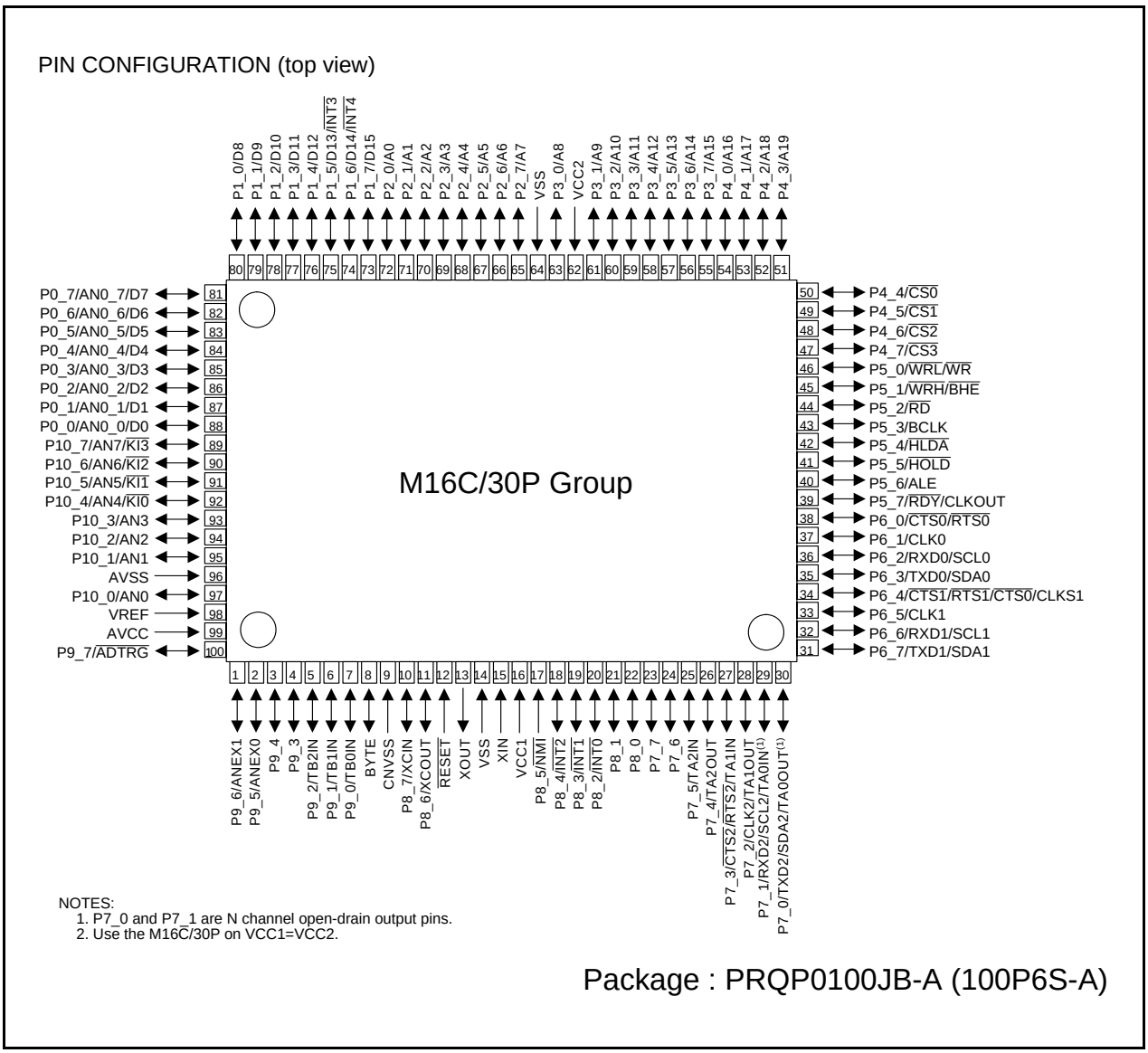


Figure 1.5 Pin Configuration (Top View)

1.6 Pin Description

Table 1.8 Pin Description (1)

Signal Name	Pin Name	I/O Type	Description
Power supply input	VCC1, VCC2 VSS	I	Apply 2.7 to 5.5 V to the VCC1 and VCC2 pins and 0 V to the VSS pin. The VCC apply condition is that VCC1 = VCC2.
Analog power supply input	AVCC AVSS	I	Applies the power supply for the A/D converter. Connect the AVCC pin to VCC1. Connect the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	The microcomputer is in a reset state when applying “L” to the this pin.
CNVSS	CNVSS	I	Switches processor mode. Connect this pin to VSS to when after a reset to start up in single-chip mode. Connect this pin to VCC1 to start up in microprocessor mode.
External data bus width select input	BYTE	I	Switches the data bus in external memory space. The data bus is 16 bits long when the this pin is held "L" and 8 bits long when the this pin is held "H". Set it to either one. Connect this pin to VSS when an single-chip mode.
Bus control pins	D0 to D7	I/O	Inputs and outputs data (D0 to D7) when these pins are set as the separate bus.
	D8 to D15	I/O	Inputs and outputs data (D8 to D15) when external 16-bit data bus is set as the separate bus.
	A0 to A19	O	Output address bits (A0 to A19).
	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	Output $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ signals. $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ are chip-select signals to specify an external space.
	$\overline{\text{WRL}}$/$\overline{\text{WR}}$ $\overline{\text{WRH}}$/$\overline{\text{BHE}}$ $\overline{\text{RD}}$	O	Output $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, ($\overline{\text{WR}}$, $\overline{\text{BHE}}$), $\overline{\text{RD}}$ signals. $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ or $\overline{\text{BHE}}$ and $\overline{\text{WR}}$ can be switched by program. • $\overline{\text{WRL}}$, $\overline{\text{WRH}}$ and $\overline{\text{RD}}$ are selected The $\overline{\text{WRL}}$ signal becomes "L" by writing data to an even address in an external memory space. The $\overline{\text{WRH}}$ signal becomes "L" by writing data to an odd address in an external memory space. The $\overline{\text{RD}}$ pin signal becomes "L" by reading data in an external memory space. • $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ are selected The $\overline{\text{WR}}$ signal becomes "L" by writing data in an external memory space. The $\overline{\text{RD}}$ signal becomes "L" by reading data in an external memory space. The $\overline{\text{BHE}}$ signal becomes "L" by accessing an odd address. Select $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ for an external 8-bit data bus.
	ALE	O	ALE is a signal to latch the address.
	$\overline{\text{HOLD}}$	I	While the $\overline{\text{HOLD}}$ pin is held "L", the microcomputer is placed in a hold state.
	$\overline{\text{HLDA}}$	O	In a hold state, $\overline{\text{HLDA}}$ outputs a "L" signal.
	$\overline{\text{RDY}}$	I	While applying a "L" signal to the $\overline{\text{RDY}}$ pin, the microcomputer is placed in a wait state.

I : Input O : Output I/O : Input and output

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0.
In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.
Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to “0”.

2.8.3 Zero Flag (Z Flag)

This flag is set to “1” when an arithmetic operation resulted in 0; otherwise, it is “0”.

2.8.4 Sign Flag (S Flag)

This flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, it is “0”.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is “0” ; register bank 1 is selected when this flag is “1”.

2.8.6 Overflow Flag (O Flag)

This flag is set to “1” when the operation resulted in an overflow; otherwise, it is “0”.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.
Maskable interrupts are disabled when the I flag is “0”, and are enabled when the I flag is “1”. The I flag is cleared to “0” when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is “0”; USP is selected when the U flag is “1”.
The U flag is cleared to “0” when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

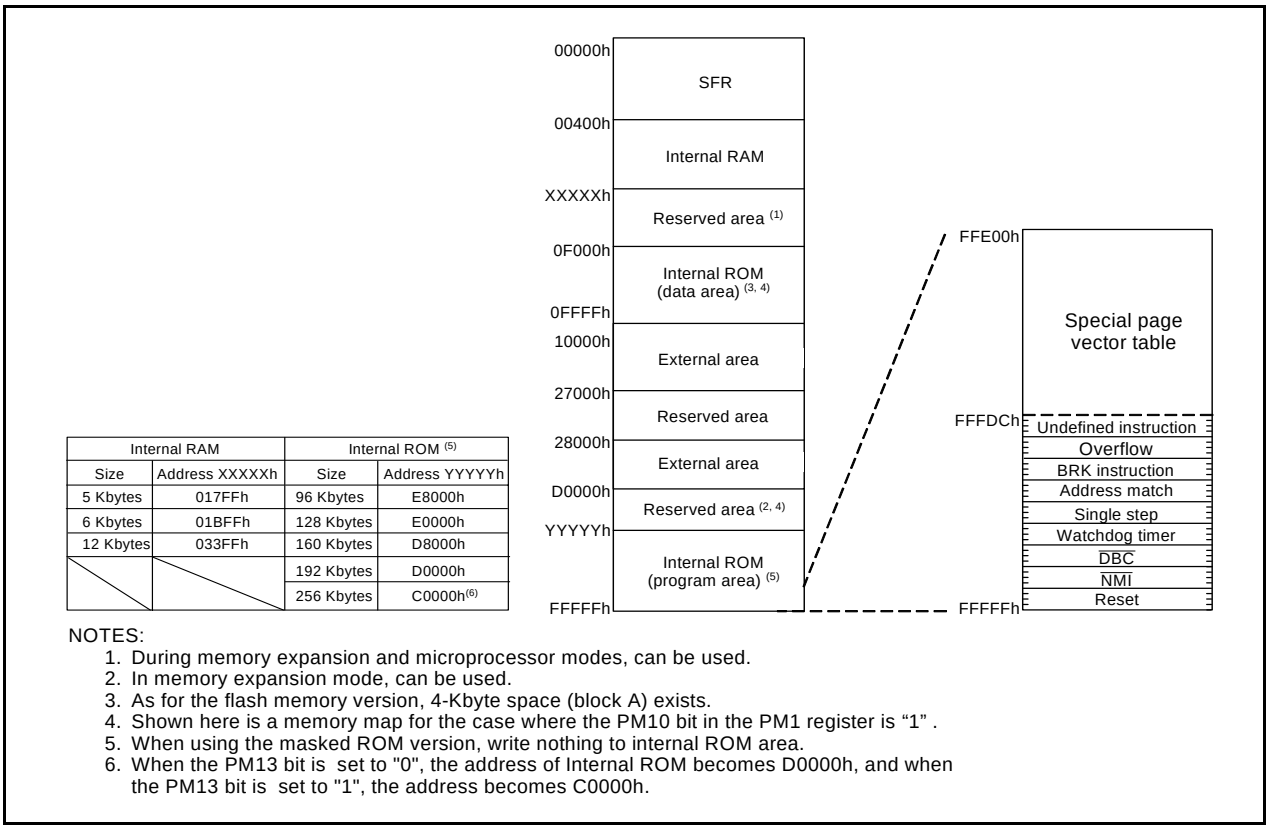
IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write “0”. When read, its content is indeterminate.

3. Memory

Figure 3.1 is a Memory Map of the M16C/30P group. The address space extends the 1 Mbyte from address 00000h to FFFFFh.
The internal ROM is allocated in a lower address direction beginning with address FFFFFh. For example, a 64-Kbyte internal ROM is allocated to the addresses from F0000h to FFFFFh.
The fixed interrupt vector table is allocated to the addresses from FFFDCh to FFFFFh. Therefore, store the start address of each interrupt routine here.
The internal RAM is allocated in an upper address direction beginning with address 00400h. For example, a 5-Kbyte internal RAM is allocated to the addresses from 00400h to 017FFh. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated. The SFR is allocated to the addresses from 00000h to 003FFh. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be used by users.
The special page vector table is allocated to the addresses from FFE00h to FFFDBh. This vector is used by the JMPS or JSRS instruction. For details, refer to the **M16C/60 and M16C/20 Series Software Manual**.



Internal RAM		Internal ROM (5)	
Size	Address XXXXXh	Size	Address YYYYYh
5 Kbytes	017FFh	96 Kbytes	E8000h
6 Kbytes	01BFFh	128 Kbytes	E0000h
12 Kbytes	033FFh	160 Kbytes	D8000h
		192 Kbytes	D0000h
		256 Kbytes	C0000h(6)

NOTES:
1. During memory expansion and microprocessor modes, can be used.
2. In memory expansion mode, can be used.
3. As for the flash memory version, 4-Kbyte space (block A) exists.
4. Shown here is a memory map for the case where the PM10 bit in the PM1 register is “1” .
5. When using the masked ROM version, write nothing to internal ROM area.
6. When the PM13 bit is set to "0", the address of Internal ROM becomes D0000h, and when the PM13 bit is set to "1", the address becomes C0000h.

Figure 3.1 Memory Map

4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.5 list the SFR information.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0 (2)	PM0	00000000b(CNVSS pin is "L") 00000011b(CNVSS pin is "H")
0005h	Processor Mode Register 1	PM1	00XXX0X0b
0006h	System Clock Control Register 0	CM0	01001000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Chip Select Control Register	CSR	00000001b
0009h	Address Match Interrupt Enable Register	AIER	XXXXXX00b
000Ah	Protect Register	PRCR	XX000000b
000Bh			
000Ch			
000Dh			
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00XXXXXXb
0010h 0011h 0012h	Address Match Interrupt Register 0	RMAD0	00h 00h X0h
0013h			
0014h 0015h 0016h	Address Match Interrupt Register 1	RMAD1	00h 00h X0h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch			
001Dh			
001Eh			
001Fh			
0020h 0021h 0022h	DMA0 Source Pointer	SAR0	XXh XXh XXh
0023h			
0024h 0025h 0026h	DMA0 Destination Pointer	DAR0	XXh XXh XXh
0027h			
0028h 0029h	DMA0 Transfer Counter	TCR0	XXh XXh
002Ah			
002Bh			
002Ch	DMA0 Control Register	DM0CON	00000X00b
002Dh			
002Eh			
002Fh			
0030h 0031h 0032h	DMA1 Source Pointer	SAR1	XXh XXh XXh
0033h			
0034h 0035h 0036h	DMA1 Destination Pointer	DAR1	XXh XXh XXh
0037h			
0038h 0039h	DMA1 Transfer Counter	TCR1	XXh XXh
003Ah			
003Bh			
003Ch	DMA1 Control Register	DM1CON	00000X00b
003Dh			
003Eh			
003Fh			

NOTES:
1. The blank areas are reserved and cannot be accessed by users.
2. The PM00 and PM01 bits do not change at software reset.

X : Nothing is mapped to this bit

Table 5.6 One Time Flash Version Electrical Characteristics (1)

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
–	Program Endurance			1	cycle
–	Word Program Time (V_{CC1}=5.0V)		50	500	µs
tPS	One Time Flash Memory Circuit Stabilization Wait Time			15	µs
–	Data Hold Time (4)	10			year

NOTES:
1. Referenced to V_{CC1}=4.5 to 5.5V, 3.0 to 3.6V at Topr = 0 to 60 °C (U3, U5) unless otherwise specified.
2. Topr = -40 to 85 °C (U3) / -20 to 85 °C (U5).

Table 5.7 One Time Flash Version Program Voltage and Read Operation Voltage Characteristics

Flash Program Voltage	Flash Read Operation Voltage
V_{CC1} = 3.3 ± 0.3 V or 5.0 ± 0.5 (T_{opr} = 0°C to 60°C)	V_{CC1}=2.7 to 5.5 V (T_{opr} = -40°C to 85°C (U3) -20°C to 85°C (U5))

$V_{CC1}=V_{CC2}=5V$

Table 5.9 Electrical Characteristics(1) (1)

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	HIGH Output Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	I_{OH}=–5mA	V_{CC}–2.0		V_{CC}	V
V_{OH}	HIGH Output Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	I_{OH}=–200µA	V_{CC}–0.3		V_{CC}	V
V_{OH}	HIGH Output Voltage XOUT	HIGHPOWER	I_{OH}=–1mA	V_{CC}–2.0		V_{CC}	V
		LOWPOWER	I_{OH}=–0.5mA	V_{CC}–2.0		V_{CC}	
	HIGH Output Voltage XCOUT	HIGHPOWER	With no load applied		2.5		V
		LOWPOWER	With no load applied		1.6		
V_{OL}	LOW Output Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	I_{OL}=5mA			2.0	V
V_{OL}	LOW Output Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	I_{OL}=200µA			0.45	V
V_{OL}	LOW Output Voltage XOUT	HIGHPOWER	I_{OL}=1mA			2.0	V
		LOWPOWER	I_{OL}=0.5mA			2.0	
	LOW Output Voltage XCOUT	HIGHPOWER	With no load applied		0		V
		LOWPOWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	TA0IN to TA2IN, TB0IN to TB2IN, $\overline{INT0}$ to $\overline{INT4}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, CLK0 to CLK2, TA0OUT to TA2OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD2, SCL0 to SCL2, SDA0 to SDA2		0.2		1.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$		0.2		2.5	V
I_{IH}	HIGH Input Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, $\overline{RESET}$, CNVSS, BYTE	V_I=5V			5.0	µA
I_{IL}	LOW Input Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, $\overline{RESET}$, CNVSS, BYTE	V_I=0V			–5.0	µA
R_{PULLUP}	Pull-Up Resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	V_I=0V	30	50	170	kΩ
R_{fXIN}	Feedback Resistance XIN				1.5		MΩ
R_{fXCIN}	Feedback Resistance XCIN				15		MΩ
V_{RAM}	RAM Retention Voltage		At stop mode	2.0			V

NOTES:
1. Referenced to $V_{CC1}=V_{CC2}$=4.2 to 5.5V, V_{SS} = 0V at T_{opr} = –20 to 85°C / –40 to 85°C, f(XIN) =16MHz unless otherwise specified.

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.11 External Clock Input (XIN input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	62.5		ns
$t_{w(H)}$	External Clock Input HIGH Pulse Width	25		ns
$t_{w(L)}$	External Clock Input LOW Pulse Width	25		ns
t_r	External Clock Rise Time		15	ns
t_f	External Clock Fall Time		15	ns

NOTES:
1. The condition is V_{CC1}=V_{CC2}=3.0 to 5.0V.

Table 5.12 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (for setting with no wait)		(NOTE 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (for setting with wait)		(NOTE 2)	ns
$t_{su(DB-RD)}$	Data Input Setup Time	40		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ Input Setup Time	30		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ Input Setup Time	40		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ Input Hold Time	0		ns

NOTES:
1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 45[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(BCLK)} - 45[ns]$$ n is "2" for 1-wait setting.

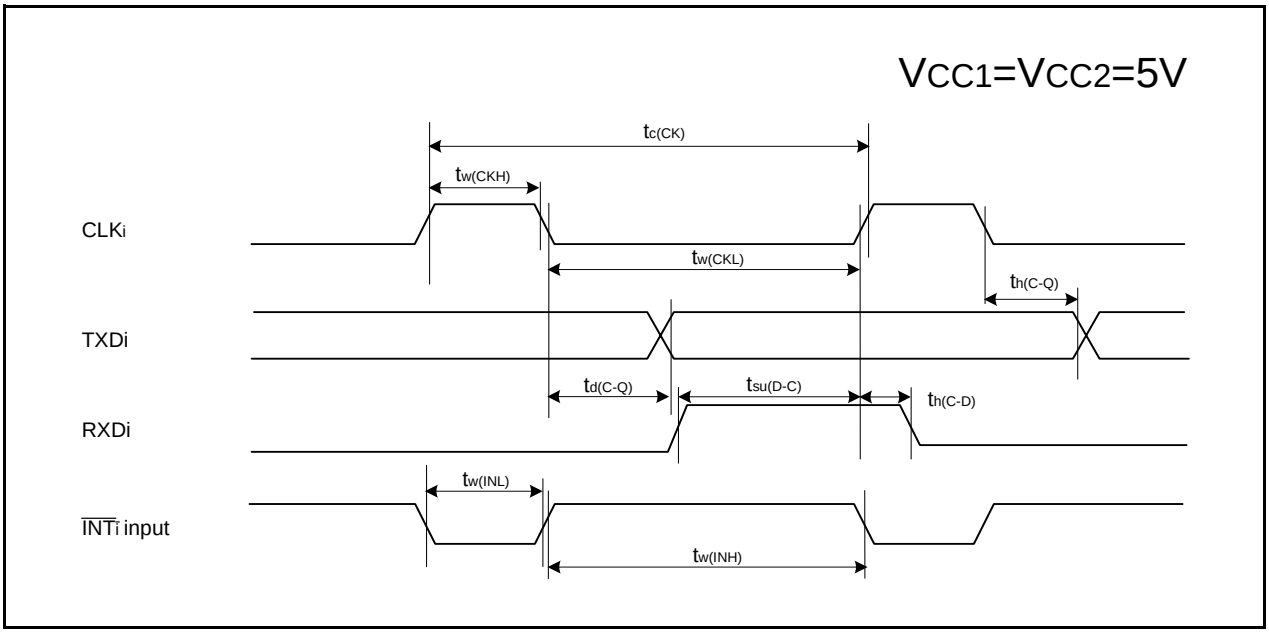
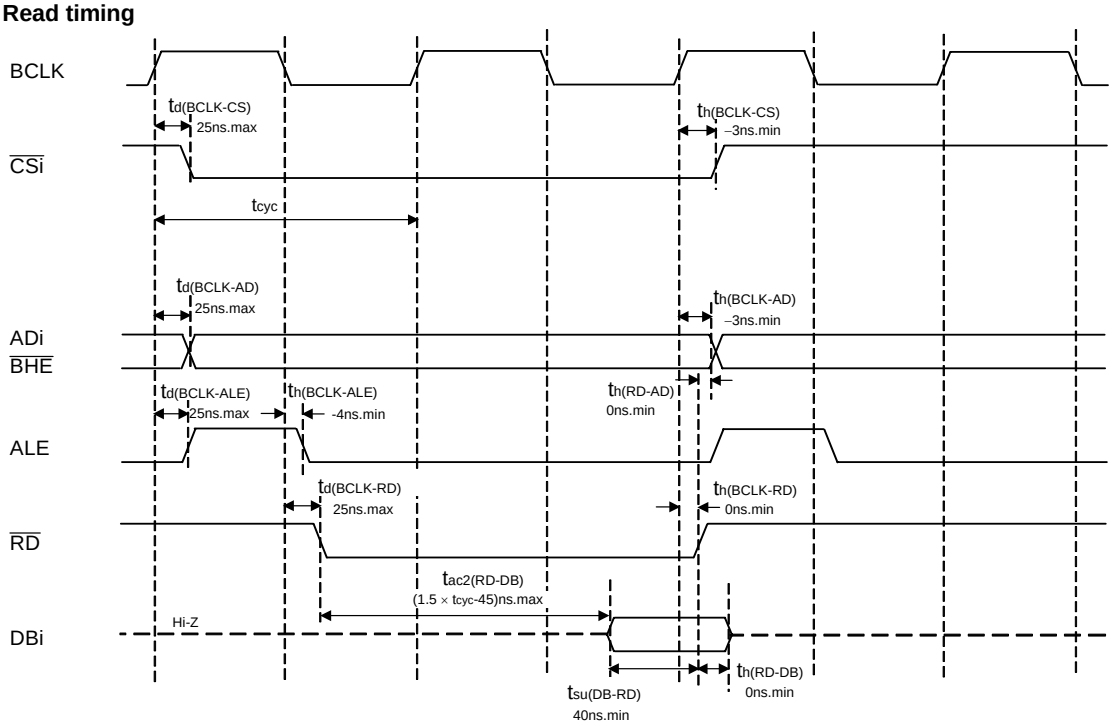


Figure 5.4 Timing Diagram (2)

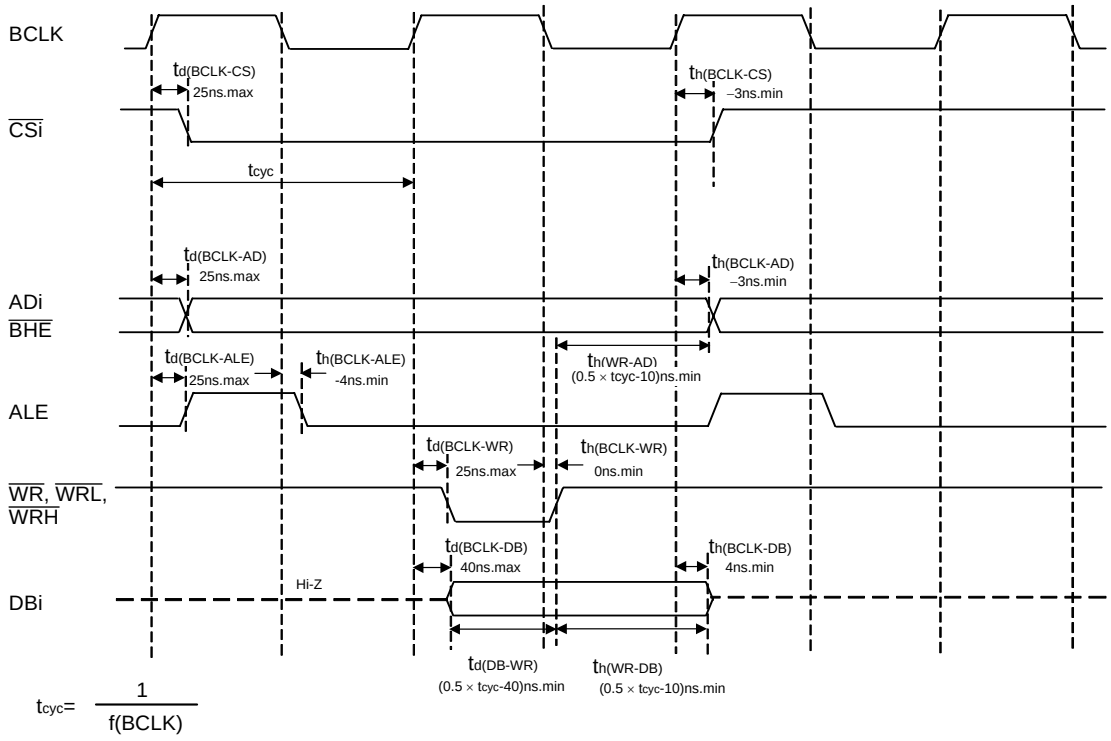
$V_{CC1}=V_{CC2}=5V$

Memory Expansion Mode, Microprocessor Mode
(for 1-wait setting and external area access**)**

Read timing



Write timing



$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
· Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

Figure 5.7 Timing Diagram (5)

Table 5.28 Electrical Characteristics (2) (1)

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
I_{CC}	Power Supply Current (V_{CC1}=V_{CC2}=2.7V to 3.6V)	In single-chip mode, the output pins are open and other pins are V_{SS}	Mask ROM	f(XIN)=10MHz No division		8	11	mA
			One Time Flash	f(XIN)=10MHz, No division		8	13	mA
			Flash Memory	f(XIN)=10MHz, No division		8	13	mA
			Flash Memory Program	f(XIN)=10MHz, VCC1=3.0V		12		mA
			One Time Flash Program	f(XIN)=10MHz, VCC1=3.0V		12		mA
			Flash Memory Erase	f(XIN)=10MHz, VCC1=3.0V		22		mA
			Mask ROM	f(XCIN)=32kHz Low power dissipation mode, ROM (3)		25		µA
			One Time Flash	f(XCIN)=32kHz Low power dissipation mode, RAM (3)		25		µA
				f(XCIN)=32kHz Low power dissipation mode, Flash Memory (3)		350		µA
			Flash Memory	f(XCIN)=32kHz Low power dissipation mode, RAM (3)		25		µA
				f(XCIN)=32kHz Low power dissipation mode, Flash Memory (3)		420		µA
			Mask ROM One Time Flash Flash Memory	f(XCIN)=32kHz Wait mode (2), Oscillation capability High		6.0		µA
				f(XCIN)=32kHz Wait mode (2), Oscillation capability Low		1.8		µA
				Stop mode Topr =25°C		0.7	3.0	µA

NOTES:
1. Referenced to V_{CC1}=V_{CC2}=2.7 to 3.3V, V_{SS} = 0V at T_{opr} = –20 to 85°C / –40 to 85°C, f(XIN)=10MHz unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.

$V_{CC1}=V_{CC2}=3V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.43 Memory Expansion and Microprocessor Modes (for setting with no wait)

Symbol	Parameter		Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address Output Delay Time	See **Figure 5.8**		30	ns
th(BCLK-AD)	Address Output Hold Time (in relation to BCLK)		0		ns
th(RD-AD)	Address Output Hold Time (in relation to RD)		0		ns
th(WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
td(BCLK-CS)	Chip Select Output Delay Time			30	ns
th(BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		0		ns
td(BCLK-ALE)	ALE Signal Output Delay Time			25	ns
th(BCLK-ALE)	ALE Signal Output Hold Time		–4		ns
td(BCLK-RD)	RD Signal Output Delay Time			30	ns
th(BCLK-RD)	RD Signal Output Hold Time		0		ns
td(BCLK-WR)	WR Signal Output Delay Time			30	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(BCLK-DB)	Data Output Delay Time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data Output Hold Time (in relation to BCLK) (3)		4		ns
td(DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
th(WR-DB)	Data Output Hold Time (in relation to WR) (3)		(NOTE 2)		ns
td(BCLK-HLDA)	HLDA Output Delay Time			40	ns

NOTES:

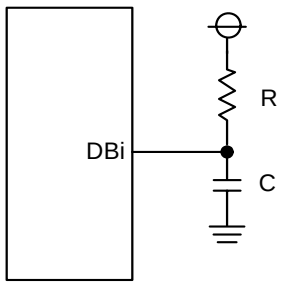
1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times10^{9}}{f(BCLK)} - 40[ns]$$ f(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times10^{9}}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
   Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
   Hold time of data bus is expressed in
   $t = -CR \times \ln(1 - V_{OL} / V_{CC1})$
   by a circuit of the right figure.
   For example, when V_{OL} = 0.2V_{CC1}, C = 30pF, R = 1kΩ, hold time of output "L" level is
   $t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC1} / V_{CC1})$
   = 6.7ns.



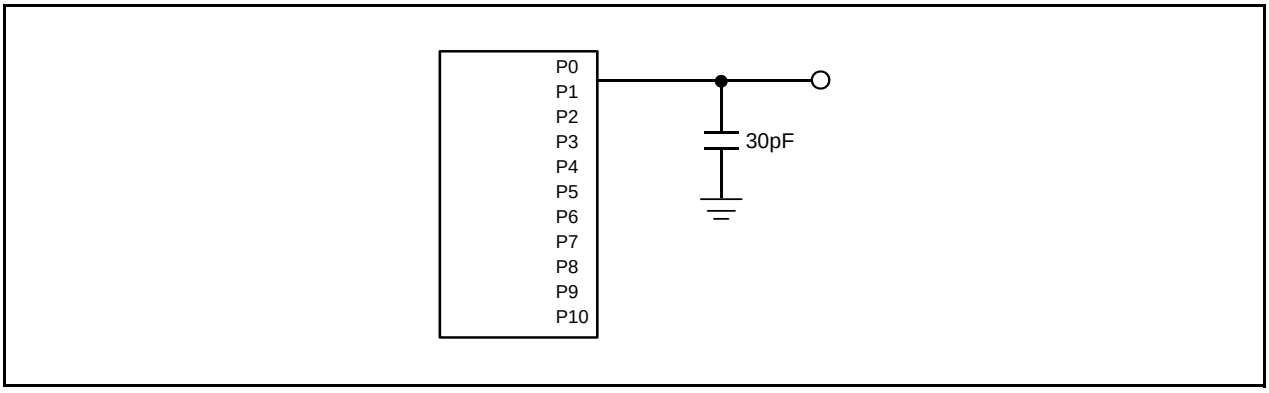
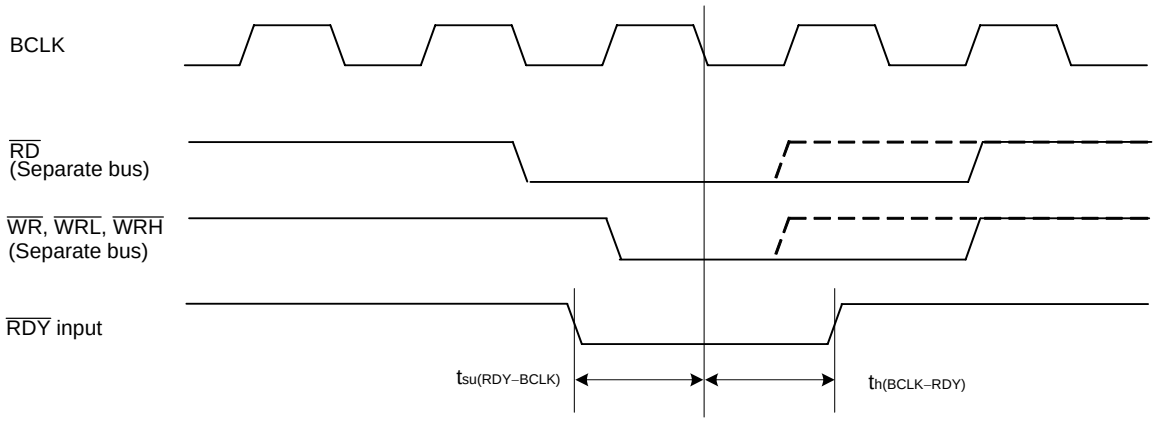


Figure 5.8 Ports P0 to P10 Measurement Circuit

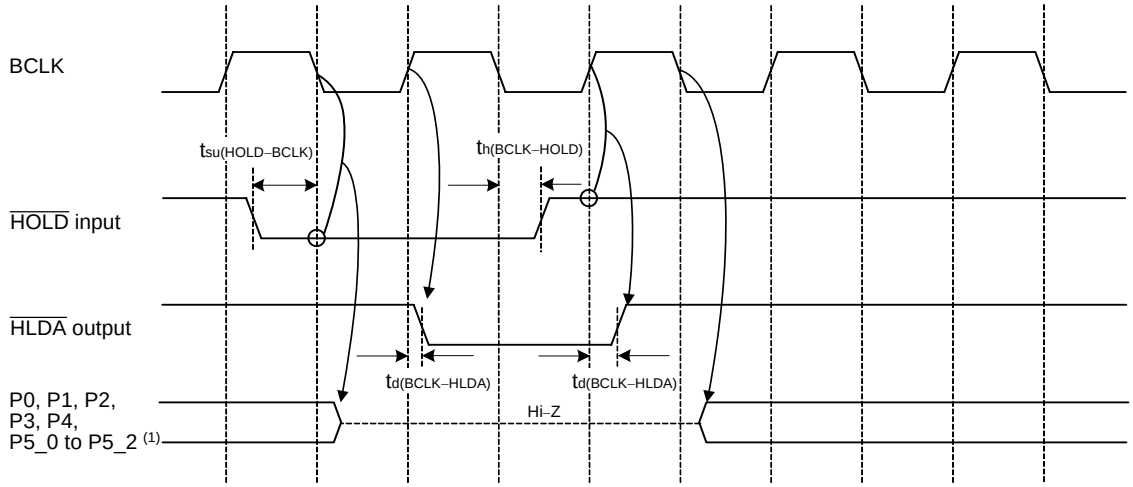
Memory Expansion Mode, Microprocessor Mode

$V_{CC1}=V_{CC2}=3V$

(Effective for setting with wait)



(Common to setting with wait and setting without wait)



NOTES:
1. These pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit in PM0 register.

Measuring conditions :
· $V_{CC1}=V_{CC2}=3V$
· Input timing voltage : Determined with $V_{IL}=0.6V$, $V_{IH}=2.4V$
· Output timing voltage : Determined with $V_{OL}=1.5V$, $V_{OH}=1.5V$

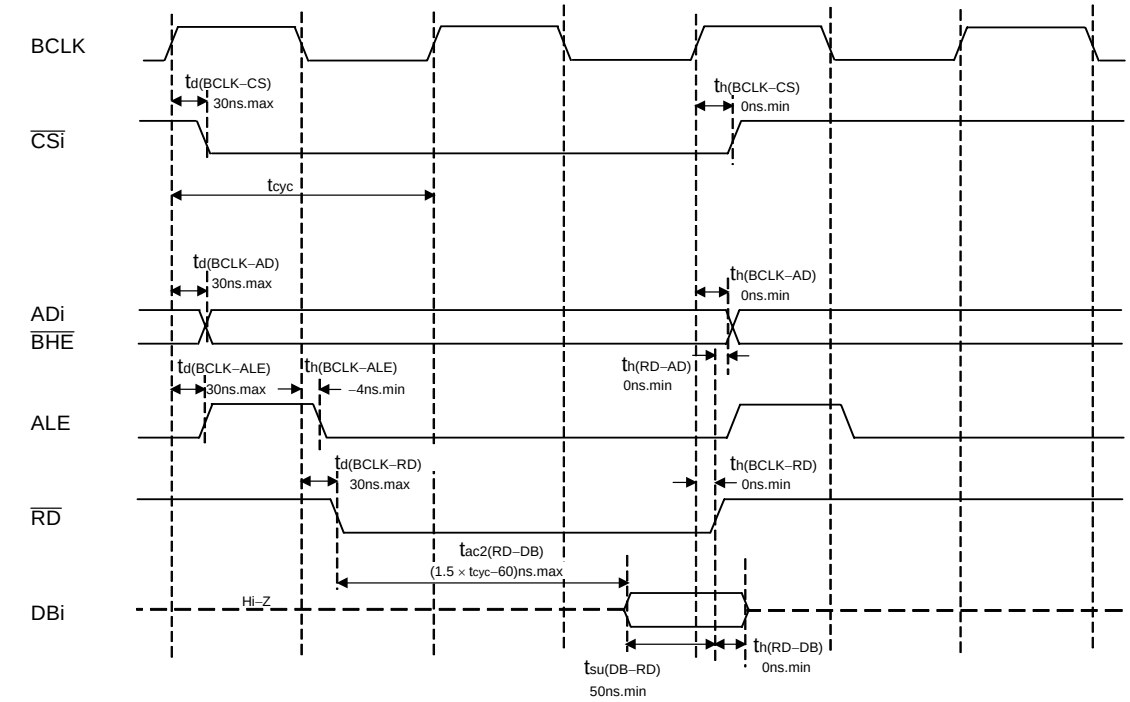
Figure 5.11 Timing Diagram (3)

Memory Expansion Mode, Microprocessor Mode

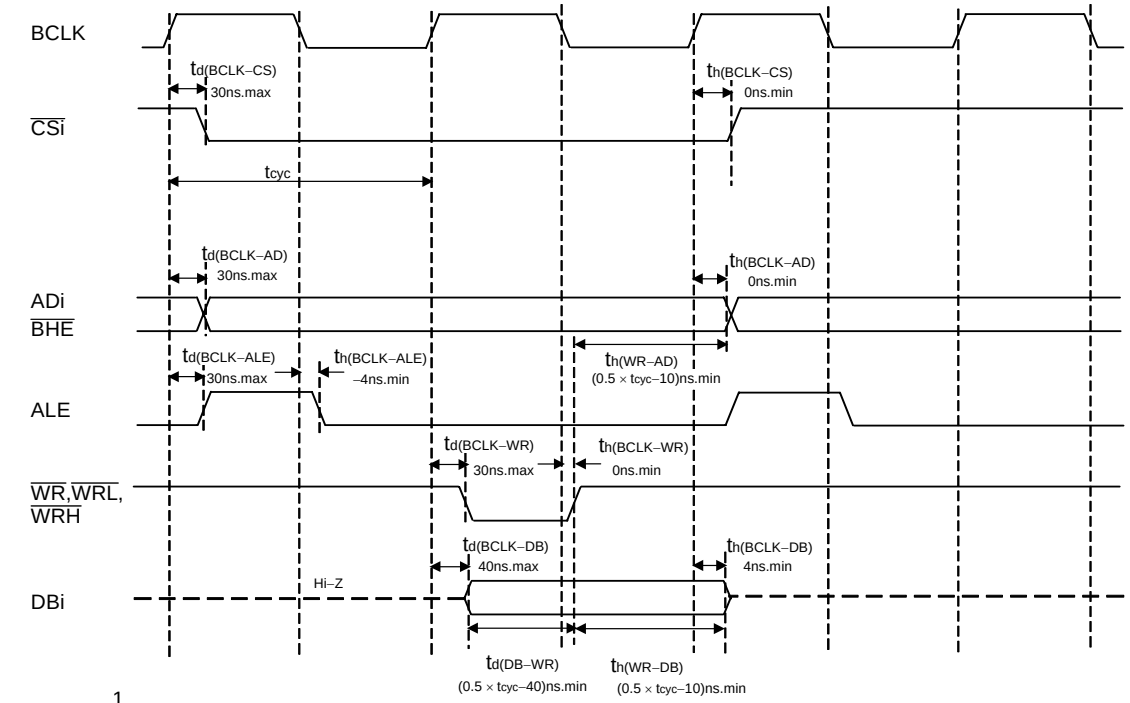
(for 1-wait setting and external area access)

$V_{CC1}=V_{CC2}=3V$

Read timing



Write timing



$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

Figure 5.13 Timing Diagram (5)

REVISION HISTORY	M16C/30P Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.70	Aug 26, 2004	–	First Edition issued
0.80	Mar 18, 2005	–	development support tools -> development tools
		–	BCLK -> CPU clock
		2	Table 1.1 Performance Outline of M16C/30P Group Serial interface is revised.
		4	Figure 1.2 Type., Memory Size, and Package is partly revised.
		8	Table 1.4 Pin Detection (2) is partly revised.
		20	Note 2 Table 5.3 A/D Conversion Characteristics is partly revised.
		21	Symbol of Table 5.4 Power Supply Circuit Timing Characteristics is partly revised.
		22	Table 5.5 Electrical Characteristics is revised.
		28	Table 5.19 Electrical Characteristics is revised.
1.00	Sep 01, 2005	2	Table 1.1 Performance Outline of M16C/30P Group is partly revised.
		4	Table 1.2 Product List is partly revised.
			Figure 1.2 Type No., Memory Size, and Package is partly revised.
		5	Figure 1.3 Pin Configuration is partly revised.
		6	Figure 1.4 Pin Configuration is partly revised.
		7-8	Tables 1.3 to 1.4 Pin Characteristics are added.
		9	Table 1.5 Pin Description is revised.
		14	3. Memory is partly revised.
		15	Table 4.1 SFR Information is partly revised.
		19	Table 4.5 SFR Information is partly revised
		21	Table 5.2 Recommended Operating Conditions is partly revised.
		22	Table 5.3 A/D Conversion Characteristics is partly revised.
		25	Note 1 is added in Table 5.6 External Clock Input (XIN input)
			Table 5.7 Memory Expansion Mode and Microprocessor Mode is added.
		28	Table 5.20 Memory Expansion Mode and Microprocessor Modes (for setting with no wait) is added.
			Figure 5.2 Ports P0 to P10 Measurement Circuit is added.
		29	Table 5.21 Memory Expansion Mode and Microprocessor Modes (for 1- to 3-wait setting and external area access) is added.
		32	Figure 5.5 Timing Diagram (3) is added.
		33	Figure 5.6 Timing Diagram (4) is added.
		34	Figure 5.7 Timing Diagram (5) is added.
		36	Note 1 to 4 are added in Table 5.23 External Clock Input (XIN input)
			Table 5.24 Memory Expansion Mode and Microprocessor Mode is added.
		39	Table 5.37 Memory Expansion Mode and Microprocessor Modes (for setting with no wait) is added.
			Figure 5.8 Ports P0 to P10 Measurement Circuit is added.
		40	Table 5.38 Memory Expansion Mode and Microprocessor Modes (for 1- to 3-wait setting and external area access) is added.
		43	Figure 5.11 Timing Diagram (3) is added.

REVISION HISTORY	M16C/30P Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.20	Oct 17, 2006	1	Note is partly deleted.
		2	Table 1.1 Performance Outline of M16C/30P Group is partly added.
		4	Table 1.2 Product List is partly revised.
		5	Figure 1.2 Type No., Memory Size, and Package is added.
		7	Table 1.4 Product Code of One Time Flash version, Flash Memory version, and ROM-less version for M16C/30P is partly added.
		17	Figure 3.1 Memory Map is partly added.
		19	Table 4.2 SFR Information (2) is partly added.
		23	Table 5.1 Absolute Maximum Ratings is partly added.
		27	Table 5.6 One Time Flash Version Electrical Characteristics and Table 5.7 One Time Flash Version Program Voltage and Read Operation Voltage Characteristics is added.
		30	Table 5.10 Electrical Characteristics (2) is partly added.
		42	Table 5.28 Electrical Characteristics (2) is partly added.
1.21	Nov 02 2006	7	Table 1.4 Product Code of One Time Flash version, Flash Memory version, and ROM-less version for M16C/30P is partly revised.
1.22	Mar 30, 2007	4	Table 1.2 Product List (1) is partly revised.
		5	Table 1.3 Product List (2) is partly revised.
		19	Table 4.2 SFR Information (2) is partly revised.