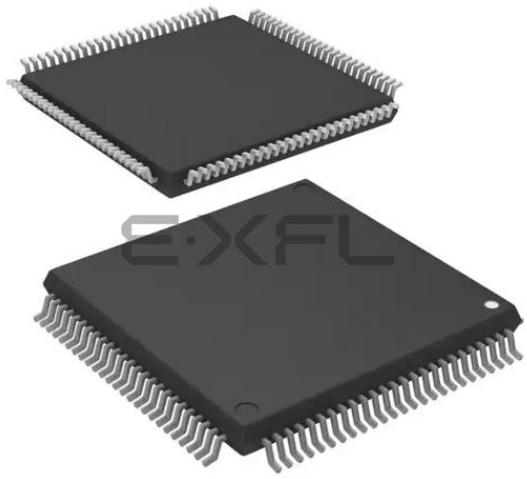
# Renesas Electronics America Inc - M30302FEPGP#U3 Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | M16C/60 |
| Core Size | 16-Bit |
| Speed | 16MHz |
| Connectivity | I²C, IEBus, UART/USART |
| Peripherals | DMA, POR, PWM, WDT |
| Number of I/O | 85 |
| Program Memory Size | 192KB (192K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 6K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 18x10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LFQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/m30302fepgp-u3 |

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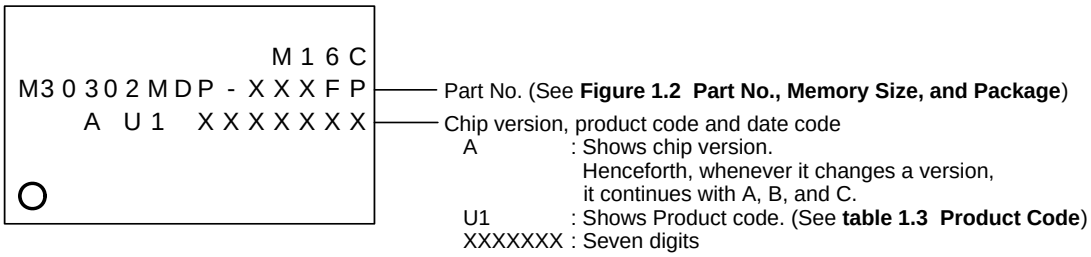
**Table 1.4 Product Code of MASK ROM version for M16C/30P**

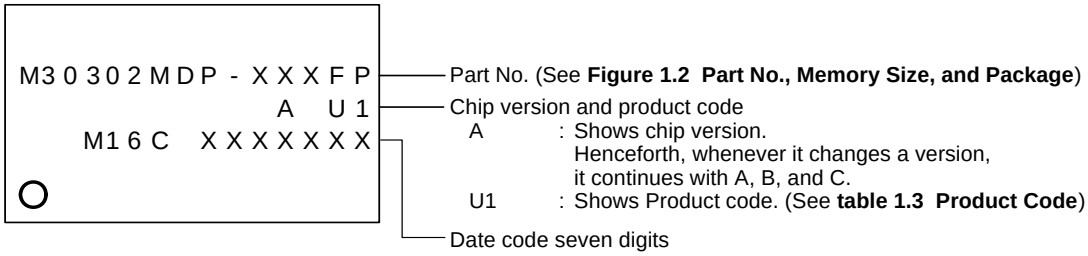
| Product Code | Package | Operating Ambient Temperature |
|---|---|---|
| U1 | Lead-free | -20°C to 85°C |
| U4 | | -40°C to 85°C |

PRQP0100JB-A (100P6S-A)

1. Standard Renesas Mark

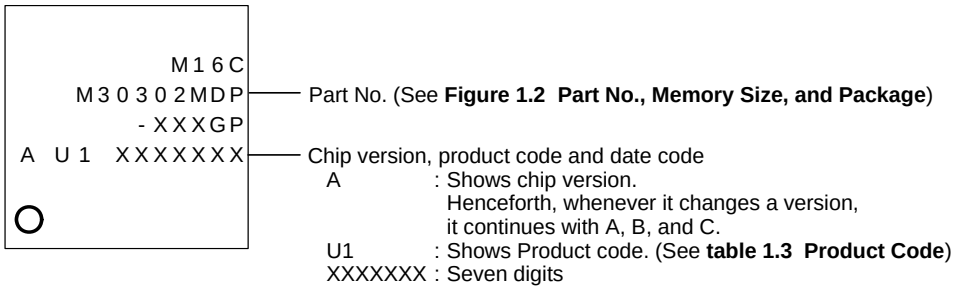



2. Customer's Parts Number + Renesas catalog name

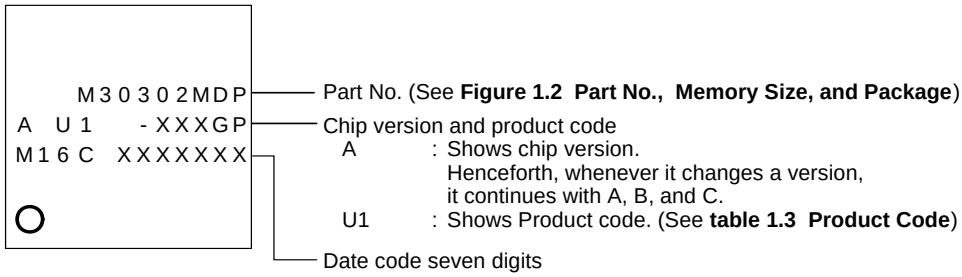



PLQP0100KB-A (100P6Q-A)

1. Standard Renesas Mark




2. Customer's Parts Number + Renesas catalog name




NOTES:
1. Refer to the **mark specification form** for details of the Mask ROM version marking.

**Figure 1.3 Marking Diagram of Mask ROM Version for M16C/30P (Top View)**

**Table 1.6 Pin Characteristics (1)**

| Pin No. | | Control Pin | Port | Interrupt Pin | Timer Pin | UART Pin | Analog Pin | Bus Control Pin |
|---|---|---|---|---|---|---|---|---|
| FP | GP | | | | | | | |
| 1 | 99 | | P9_6 | | | | ANEX1 | |
| 2 | 100 | | P9_5 | | | | ANEX0 | |
| 3 | 1 | | P9_4 | | | | | |
| 4 | 2 | | P9_3 | | | | | |
| 5 | 3 | | P9_2 | | TB2IN | | | |
| 6 | 4 | | P9_1 | | TB1IN | | | |
| 7 | 5 | | P9_0 | | TB0IN | | | |
| 8 | 6 | BYTE | | | | | | |
| 9 | 7 | CNVSS | | | | | | |
| 10 | 8 | XCIN | P8_7 | | | | | |
| 11 | 9 | XCOUT | P8_6 | | | | | |
| 12 | 10 | $\overline{\text{RESET}}$ | | | | | | |
| 13 | 11 | XOUT | | | | | | |
| 14 | 12 | VSS | | | | | | |
| 15 | 13 | XIN | | | | | | |
| 16 | 14 | VCC1 | | | | | | |
| 17 | 15 | | P8_5 | $\overline{\text{NMI}}$ | | | | |
| 18 | 16 | | P8_4 | $\overline{\text{INT2}}$ | | | | |
| 19 | 17 | | P8_3 | $\overline{\text{INT1}}$ | | | | |
| 20 | 18 | | P8_2 | $\overline{\text{INT0}}$ | | | | |
| 21 | 19 | | P8_1 | | | | | |
| 22 | 20 | | P8_0 | | | | | |
| 23 | 21 | | P7_7 | | | | | |
| 24 | 22 | | P7_6 | | | | | |
| 25 | 23 | | P7_5 | | TA2IN | | | |
| 26 | 24 | | P7_4 | | TA2OUT | | | |
| 27 | 25 | | P7_3 | | TA1IN | $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ | | |
| 28 | 26 | | P7_2 | | TA1OUT | CLK2 | | |
| 29 | 27 | | P7_1 | | TA0IN | RXD2/SCL2 | | |
| 30 | 28 | | P7_0 | | TA0OUT | TXD2/SDA2 | | |
| 31 | 29 | | P6_7 | | | TXD1/SDA1 | | |
| 32 | 30 | | P6_6 | | | RXD1/SCL1 | | |
| 33 | 31 | | P6_5 | | | CLK1 | | |
| 34 | 32 | | P6_4 | | | $\overline{\text{CTS1}}/\overline{\text{RTS1}}/\overline{\text{CTS0}}$/CLKS1 | | |
| 35 | 33 | | P6_3 | | | TXD0/SDA0 | | |
| 36 | 34 | | P6_2 | | | RXD0/SCL0 | | |
| 37 | 35 | | P6_1 | | | CLK0 | | |
| 38 | 36 | | P6_0 | | | $\overline{\text{CTS0}}/\overline{\text{RTS0}}$ | | |
| 39 | 37 | | P5_7 | | | | | $\overline{\text{RDY}}$/CLKOUT |
| 40 | 38 | | P5_6 | | | | | ALE |
| 41 | 39 | | P5_5 | | | | | $\overline{\text{HOLD}}$ |
| 42 | 40 | | P5_4 | | | | | $\overline{\text{HLDA}}$ |
| 43 | 41 | | P5_3 | | | | | BCLK |
| 44 | 42 | | P5_2 | | | | | $\overline{\text{RD}}$ |
| 45 | 43 | | P5_1 | | | | | $\overline{\text{WRH}}/\overline{\text{BHE}}$ |
| 46 | 44 | | P5_0 | | | | | $\overline{\text{WRL}}/\overline{\text{WR}}$ |
| 47 | 45 | | P4_7 | | | | | $\overline{\text{CS3}}$ |
| 48 | 46 | | P4_6 | | | | | $\overline{\text{CS2}}$ |
| 49 | 47 | | P4_5 | | | | | $\overline{\text{CS1}}$ |
| 50 | 48 | | P4_4 | | | | | $\overline{\text{CS0}}$ |

**Table 1.9 Pin Description (2)**

| Signal Name | Pin Name | I/O Type | Description |
|---|---|---|---|
| Main clock input | XIN | I | I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To use the external clock, input the clock from XIN and leave XOUT open. |
| Main clock output | XOUT | O | |
| Sub clock input | XCIN | I | I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT. To use the external clock, input the clock from XCIN and leave XCOUT open. |
| Sub clock output | XCOUT | O | |
| Clock output | CLKOUT | O | The clock of the same cycle as fC, f8, or f32 is outputted. |
| $\overline{\text{INT}}$ interrupt input | $\overline{\text{INT0}}$ to $\overline{\text{INT4}}$ | I | Input pins for the $\overline{\text{INT}}$ interrupt. |
| $\overline{\text{NMI}}$ interrupt input | $\overline{\text{NMI}}$ | I | Input pin for the $\overline{\text{NMI}}$ interrupt. |
| Key input interrupt input | $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ | I | Input pins for the key input interrupt. |
| Timer A | TA0OUT to TA2OUT | I/O | These are timer A0 to timer A2 I/O pins. (however, the output of TA0OUT for the N-channel open drain output.) |
| | TA0IN to TA2IN | I | These are timer A0 to timer A2 input pins. |
| Timer B | TB0IN to TB2IN | I | These are timer B0 to timer B2 input pins. |
| Serial interface | $\overline{\text{CTS0}}$ to $\overline{\text{CTS2}}$ | I | These are send control input pins. |
| | $\overline{\text{RTS0}}$ to $\overline{\text{RTS2}}$ | O | These are receive control output pins. |
| | CLK0 to CLK2 | I/O | These are transfer clock I/O pins. |
| | RXD0 to RXD2 | I | These are serial data input pins. |
| | TXD0 to TXD2 | O | These are serial data output pins. (however, TXD2 for the N-channel open drain output.) |
| | CLKS1 | O | This is output pin for transfer clock output from multiple pins function. |
| $I^2C$ mode | SDA0 to SDA2 | I/O | These are serial data I/O pins. (however, SDA2 for the N-channel open drain output.) |
| | SCL0 to SCL2 | I/O | These are transfer clock I/O pins. (however, SCL2 for the N-channel open drain output.) |
| Reference voltage input | VREF | I | Applies the reference voltage for the A/D converter. |
| A/D converter | AN0 to AN7, AN0_0 to AN0_7 | I | Analog input pins for the A/D converter. |
| | $\overline{\text{ADTRG}}$ | I | This is an A/D trigger input pin. |
| | ANEX0 | I/O | This is the extended analog input pin for the A/D converter, and is the output in external op-amp connection mode. |
| | ANEX1 | I | This is the extended analog input pin for the A/D converter. |
| I/O port | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P9_0 to P9_7, P10_0 to P10_7 | I/O | 8-bit I/O ports in CMOS, having a direction register to select an input or output.<br>Each pin is set as an input port or output port. An input port can be set for a pull-up or for no pull-up in 4-bit unit by program. (however, P7_0 and P7_1 for the N-channel open drain output.) |
| | P8_0 to P8_4, P8_6, P8_7 | I/O | I/O ports having equivalent functions to P0. |
| Input port | P8_5 | I | Input pin for the $\overline{\text{NMI}}$ interrupt. Pin states can be read by the P8_5 bit in the P8 register. |

I : Input O : Output I/O : Input and output

# 4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.5 list the SFR information.

**Table 4.1 SFR Information (1) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0000h | | | |
| 0001h | | | |
| 0002h | | | |
| 0003h | | | |
| 0004h | Processor Mode Register 0 (2) | PM0 | 00000000b(CNVSS pin is "L")<br>00000011b(CNVSS pin is "H") |
| 0005h | Processor Mode Register 1 | PM1 | 00XXX0X0b |
| 0006h | System Clock Control Register 0 | CM0 | 01001000b |
| 0007h | System Clock Control Register 1 | CM1 | 00100000b |
| 0008h | Chip Select Control Register | CSR | 00000001b |
| 0009h | Address Match Interrupt Enable Register | AIER | XXXXXX00b |
| 000Ah | Protect Register | PRCR | XX000000b |
| 000Bh | | | |
| 000Ch | | | |
| 000Dh | | | |
| 000Eh | Watchdog Timer Start Register | WDTS | XXh |
| 000Fh | Watchdog Timer Control Register | WDC | 00XXXXXXb |
| 0010h<br>0011h<br>0012h | Address Match Interrupt Register 0 | RMAD0 | 00h<br>00h<br>X0h |
| 0013h | | | |
| 0014h<br>0015h<br>0016h | Address Match Interrupt Register 1 | RMAD1 | 00h<br>00h<br>X0h |
| 0017h | | | |
| 0018h | | | |
| 0019h | | | |
| 001Ah | | | |
| 001Bh | | | |
| 001Ch | | | |
| 001Dh | | | |
| 001Eh | | | |
| 001Fh | | | |
| 0020h<br>0021h<br>0022h | DMA0 Source Pointer | SAR0 | XXh<br>XXh<br>XXh |
| 0023h | | | |
| 0024h<br>0025h<br>0026h | DMA0 Destination Pointer | DAR0 | XXh<br>XXh<br>XXh |
| 0027h | | | |
| 0028h<br>0029h | DMA0 Transfer Counter | TCR0 | XXh<br>XXh |
| 002Ah | | | |
| 002Bh | | | |
| 002Ch | DMA0 Control Register | DM0CON | 00000X00b |
| 002Dh | | | |
| 002Eh | | | |
| 002Fh | | | |
| 0030h<br>0031h<br>0032h | DMA1 Source Pointer | SAR1 | XXh<br>XXh<br>XXh |
| 0033h | | | |
| 0034h<br>0035h<br>0036h | DMA1 Destination Pointer | DAR1 | XXh<br>XXh<br>XXh |
| 0037h | | | |
| 0038h<br>0039h | DMA1 Transfer Counter | TCR1 | XXh<br>XXh |
| 003Ah | | | |
| 003Bh | | | |
| 003Ch | DMA1 Control Register | DM1CON | 00000X00b |
| 003Dh | | | |
| 003Eh | | | |
| 003Fh | | | |

NOTES:
1. The blank areas are reserved and cannot be accessed by users.
2. The PM00 and PM01 bits do not change at software reset.

X : Nothing is mapped to this bit

**Table 4.3 SFR Information (3) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0340h | | | |
| 0341h | | | |
| 0342h | | | |
| 0343h | | | |
| 0344h | | | |
| 0345h | | | |
| 0346h | | | |
| 0347h | | | |
| 0348h | | | |
| 0349h | | | |
| 034Ah | | | |
| 034Bh | | | |
| 034Ch | | | |
| 034Dh | | | |
| 034Eh | | | |
| 034Fh | | | |
| 0350h | | | |
| 0351h | | | |
| 0352h | | | |
| 0353h | | | |
| 0354h | | | |
| 0355h | | | |
| 0356h | | | |
| 0357h | | | |
| 0358h | | | |
| 0359h | | | |
| 035Ah | | | |
| 035Bh | | | |
| 035Ch | | | |
| 035Dh | | | |
| 035Eh | Interrupt Factor Select Register 2 | IFSR2A | 00XXXXXXb |
| 035Fh | Interrupt Factor Select Register | IFSR | 00h |
| 0360h | | | |
| 0361h | | | |
| 0362h | | | |
| 0363h | | | |
| 0364h | | | |
| 0365h | | | |
| 0366h | | | |
| 0367h | | | |
| 0368h | | | |
| 0369h | | | |
| 036Ah | | | |
| 036Bh | | | |
| 036Ch | UART0 Special Mode Register 4 | U0SMR4 | 00h |
| 036Dh | UART0 Special Mode Register 3 | U0SMR3 | 000X0X0Xb |
| 036Eh | UART0 Special Mode Register 2 | U0SMR2 | X0000000b |
| 036Fh | UART0 Special Mode Register | U0SMR | X0000000b |
| 0370h | UART1 Special Mode Register 4 | U1SMR4 | 00h |
| 0371h | UART1 Special Mode Register 3 | U1SMR3 | 000X0X0Xb |
| 0372h | UART1 Special Mode Register 2 | U1SMR2 | X0000000b |
| 0373h | UART1 Special Mode Register | U1SMR | X0000000b |
| 0374h | UART2 Special Mode Register 4 | U2SMR4 | 00h |
| 0375h | UART2 Special Mode Register 3 | U2SMR3 | 000X0X0Xb |
| 0376h | UART2 Special Mode Register 2 | U2SMR2 | X0000000b |
| 0377h | UART2 Special Mode Register | U2SMR | X0000000b |
| 0378h | UART2 Transmit/Receive Mode Register | U2MR | 00h |
| 0379h | UART2 Bit Rate Generator | U2BRG | XXh |
| 037Ah<br>037Bh | UART2 Transmit Buffer Register | U2TB | XXh<br>XXh |
| 037Ch | UART2 Transmit/Receive Control Register 0 | U2C0 | 00001000b |
| 037Dh | UART2 Transmit/Receive Control Register 1 | U2C1 | 00000010b |
| 037Eh<br>037Fh | UART2 Receive Buffer Register | U2RB | XXh<br>XXh |

NOTES:
1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

**Table 4.4 SFR Information (4) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0380h | Count Start Flag | TABSR | 000XX000b |
| 0381h | Clock Prescaler Reset Fag | CPSRF | 0XXXXXXXb |
| 0382h | One-Shot Start Flag | ONSF | 00XXX000b |
| 0383h | Trigger Select Register | TRGSR | XXXX0000b |
| 0384h | Up-Down Flag | UDF | XX0XX000b (2) |
| 0385h | | | |
| 0386h<br>0387h | Timer A0 Register | TA0 | XXh<br>XXh |
| 0388h<br>0389h | Timer A1 Register | TA1 | XXh<br>XXh |
| 038Ah<br>038Bh | Timer A2 Register | TA2 | XXh<br>XXh |
| 038Ch | | | |
| 038Dh | | | |
| 038Eh | | | |
| 038Fh | | | |
| 0390h<br>0391h | Timer B0 Register | TB0 | XXh<br>XXh |
| 0392h<br>0393h | Timer B1 Register | TB1 | XXh<br>XXh |
| 0394h<br>0395h | Timer B2 Register | TB2 | XXh<br>XXh |
| 0396h | Timer A0 Mode Register | TA0MR | 00h |
| 0397h | Timer A1 Mode Register | TA1MR | 00h |
| 0398h | Timer A2 Mode Register | TA2MR | 00h |
| 0399h | | | |
| 039Ah | | | |
| 039Bh | Timer B0 Mode Register | TB0MR | 00XX0000b |
| 039Ch | Timer B1 Mode Register | TB1MR | 00XX0000b |
| 039Dh | Timer B2 Mode Register | TB2MR | 00XX0000b |
| 039Eh | | | |
| 039Fh | | | |
| 03A0h | UART0 Transmit/Receive Mode Register | U0MR | 00h |
| 03A1h | UART0 Bit Rate Generator | U0BRG | XXh |
| 03A2h<br>03A3h | UART0 Transmit Buffer Register | U0TB | XXh<br>XXh |
| 03A4h | UART0 Transmit/Receive Control Register 0 | U0C0 | 00001000b |
| 03A5h | UART0 Transmit/Receive Control Register 1 | U0C1 | 00000010b |
| 03A6h<br>03A7h | UART0 Receive Buffer Register | U0RB | XXh<br>XXh |
| 03A8h | UART1 Transmit/Receive Mode Register | U1MR | 00h |
| 03A9h | UART1 Bit Rate Generator | U1BRG | XXh |
| 03AAh<br>03ABh | UART1 Transmit Buffer Register | U1TB | XXh<br>XXh |
| 03ACh | UART1 Transmit/Receive Control Register 0 | U1C0 | 00001000b |
| 03ADh | UART1 Transmit/Receive Control Register 1 | U1C1 | 00000010b |
| 03AEh<br>03AFh | UART1 Receive Buffer Register | U1RB | XXh<br>XXh |
| 03B0h | UART Transmit/Receive Control Register 2 | UCON | X0000000b |
| 03B1h | | | |
| 03B2h | | | |
| 03B3h | | | |
| 03B4h | | | |
| 03B5h | | | |
| 03B6h | | | |
| 03B7h | | | |
| 03B8h | DMA0 Request Factor Select Register | DM0SL | 00h |
| 03B9h | | | |
| 03BAh | DMA1 Request Factor Select Register | DM1SL | 00h |
| 03BBh | | | |
| 03BCh<br>03BDh | CRC Data Register | CRCD | XXh<br>XXh |
| 03BEh | CRC Input Register | CRCIN | XXh |
| 03BFh | | | |

NOTES:
1. The blank areas are reserved and cannot be accessed by users.
2. Bit 5 in the Up-down flag is “0” by reset. However, The values in these bits when read are indeterminate.

X : Nothing is mapped to this bit

**Table 4.5 SFR Information (5) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 03C0h | A/D Register 0 | AD0 | XXh |
| 03C1h | | | XXh |
| 03C2h | A/D Register 1 | AD1 | XXh |
| 03C3h | | | XXh |
| 03C4h | A/D Register 2 | AD2 | XXh |
| 03C5h | | | XXh |
| 03C6h | A/D Register 3 | AD3 | XXh |
| 03C7h | | | XXh |
| 03C8h | A/D Register 4 | AD4 | XXh |
| 03C9h | | | XXh |
| 03CAh | A/D Register 5 | AD5 | XXh |
| 03CBh | | | XXh |
| 03CCh | A/D Register 6 | AD6 | XXh |
| 03CDh | | | XXh |
| 03CEh | A/D Register 7 | AD7 | XXh |
| 03CFh | | | XXh |
| 03D0h | | | |
| 03D1h | | | |
| 03D2h | | | |
| 03D3h | | | |
| 03D4h | A/D Control Register 2 | ADCON2 | XXX000X0b |
| 03D5h | | | |
| 03D6h | A/D Control Register 0 | ADCON0 | 000X0XXXb |
| 03D7h | A/D Control Register 1 | ADCON1 | 00000XXXb |
| 03D8h | | | |
| 03D9h | | | |
| 03DAh | | | |
| 03DBh | | | |
| 03DCh | | | |
| 03DDh | | | |
| 03DEh | | | |
| 03DFh | | | |
| 03E0h | Port P0 Register | P0 | XXh |
| 03E1h | Port P1 Register | P1 | XXh |
| 03E2h | Port P0 Direction Register | PD0 | 00h |
| 03E3h | Port P1 Direction Register | PD1 | 00h |
| 03E4h | Port P2 Register | P2 | XXh |
| 03E5h | Port P3 Register | P3 | XXh |
| 03E6h | Port P2 Direction Register | PD2 | 00h |
| 03E7h | Port P3 Direction Register | PD3 | 00h |
| 03E8h | Port P4 Register | P4 | XXh |
| 03E9h | Port P5 Register | P5 | XXh |
| 03EAh | Port P4 Direction Register | PD4 | 00h |
| 03EBh | Port P5 Direction Register | PD5 | 00h |
| 03ECh | Port P6 Register | P6 | XXh |
| 03EDh | Port P7 Register | P7 | XXh |
| 03EEh | Port P6 Direction Register | PD6 | 00h |
| 03EFh | Port P7 Direction Register | PD7 | 00h |
| 03F0h | Port P8 Register | P8 | XXh |
| 03F1h | Port P9 Register | P9 | XXh |
| 03F2h | Port P8 Direction Register | PD8 | 00X00000b |
| 03F3h | Port P9 Direction Register | PD9 | 00h |
| 03F4h | Port P10 Register | P10 | XXh |
| 03F5h | | | |
| 03F6h | Port P10 Direction Register | PD10 | 00h |
| 03F7h | | | |
| 03F8h | | | |
| 03F9h | | | |
| 03FAh | | | |
| 03FBh | | | |
| 03FCh | Pull-Up Control Register 0 | PUR0 | 00h |
| 03FDh | Pull-Up Control Register 1 | PUR1 | 00000000b (2)<br>00000010b (2) |
| 03FEh | Pull-Up Control Register 2 | PUR2 | 00h |
| 03FFh | Port Control Register | PCR | 00h |

NOTES:
1. The blank areas are reserved and cannot be accessed by users.
2. At hardware reset, the register is as follows:
   - "00000000b" where "L" is inputted to the CNVSS pin
   - "00000010b" where "H" is inputted to the CNVSS pin

   At software reset, the register is as follows:
   - "00000000b" where the PM01 to PM00 bits in the PM0 register are "00b" (single-chip mode).
   - "00000010b" where the PM01 to PM00 bits in the PM0 register are "01b" (memory expansion mode) or "11b" (microprocessor mode).

X : Nothing is mapped to this bit

# 5. Electrical Characteristics

**Table 5.1 Absolute Maximum Ratings**

| Symbol | Parameter | | Condition | Rated Value | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage($V_{CC1}$=$V_{CC2}$) | | $V_{CC1}$=$V_{CC2}$=AVcc | –0.3 to 6.5 | V |
| AVcc | Analog Supply Voltage | | $V_{CC1}$=$V_{CC2}$=AVcc | –0.3 to 6.5 | V |
| $V_I$ | Input Voltage | $\overline{\text{RESET}}$, CNVSS, BYTE, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, VREF, XIN | | –0.3 to $V_{CC}$+0.3 | V |
| | | P7_0, P7_1 | | –0.3 to 6.5 | V |
| $V_O$ | Output Voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, XOUT | | –0.3 to $V_{CC}$+0.3 | V |
| | | P7_0, P7_1 | | –0.3 to 6.5 | V |
| $P_d$ | Power Dissipation | | –40°C<$T_{opr}$≤85°C | 300 | mW |
| $T_{opr}$ | Operating Ambient Temperature | When the Microcomputer is Operating | | –20 to 85 / –40 to 85 | °C |
| | | One Time Flash Program Erase | | 0 to 60 | |
| | | Flash Program Erase | | 0 to 60 | |
| $T_{stg}$ | Storage Temperature | | | –65 to 150 | °C |

**Table 5.3 A/D Conversion Characteristics** (1)

| Symbol | Parameter | | Measuring Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| – | Resolution | | $V_{REF}=V_{CC}$ | | | | 10 | Bits |
| INL | Integral Non-Linearity Error | 10bit | $V_{REF}=V_{CC}=5V$ | AN0 to AN7 input, AN0_0 to AN0_7 input, ANEX0, ANEX1 input | | | ±5 | LSB |
| | | | $V_{REF}=V_{CC}=3.3V$ | AN0 to AN7 input, AN0_0 to AN0_7 input, ANEX0, ANEX1 input | | | ±7 | LSB |
| | | 8bit | $V_{REF}=V_{CC}=5V, 3.3V$ | | | | ±2 | LSB |
| – | Absolute Accuracy | 10bit | $V_{REF}=V_{CC}=5V$ | AN0 to AN7 input, AN0_0 to AN0_7 input, ANEX0, ANEX1 input | | | ±5 | LSB |
| | | | $V_{REF}=V_{CC}=3.3V$ | AN0 to AN7 input, AN0_0 to AN0_7 input, ANEX0, ANEX1 input | | | ±7 | LSB |
| | | 8bit | $V_{REF}=V_{CC}=5V, 3.3V$ | | | | ±2 | LSB |
| – | Tolerance Level Impedance | | | | | 3 | | kΩ |
| DNL | Differential Non-Linearity Error | | | | | | ±2 | LSB |
| – | Offset Error | | | | | | ±5 | LSB |
| – | Gain Error | | | | | | ±5 | LSB |
| $R_{LADDER}$ | Ladder Resistance | | $V_{REF}=V_{CC}$ | | 10 | | 40 | kΩ |
| $t_{CONV}$ | 10-bit Conversion Time, Sample & Hold Function Available | | $V_{REF}=V_{CC}=5V$, ϕAD=10MHz | | 3.3 | | | µs |
| $t_{CONV}$ | 8-bit Conversion Time, Sample & Hold Function Available | | $V_{REF}=V_{CC}=5V$, ϕAD=10MHz | | 2.8 | | | µs |
| $t_{SAMP}$ | Sampling Time | | | | 0.3 | | | µs |
| $V_{REF}$ | Reference Voltage | | | | 3.0 | | $V_{CC}$ | V |
| $V_{IA}$ | Analog Input Voltage | | | | 0 | | $V_{REF}$ | V |

NOTES:
1. Referenced to $V_{CC}=AV_{CC}=V_{REF}=3.3$ to 5.5V, $V_{SS}=AV_{SS}=0V$ at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified.
2. ϕAD frequency must be 10 MHz or less.
3. When sample & hold function is disabled, ϕAD frequency must be 250 kHz or more, in addition to the limitation in Note 2.
4. When sample & hold function is enabled, ϕAD frequency must be 1MHz or more, in addition to the limitation in Note 2.

**Table 5.4 Flash Memory Version Electrical Characteristics (1)**

| Symbol | Parameter | | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program and Erase Endurance (2) | | 100(3) | | | cycle |
| – | Word Program Time ($V_{CC1}$=5.0V) | | | 25 | 200 | µs |
| – | Lock Bit Program Time | | | 25 | 200 | µs |
| – | Block Erase Time ($V_{CC1}$=5.0V) | 4-Kbyte block | | 0.3 | 4 | s |
| – | | 8-Kbyte block | | 0.3 | 4 | s |
| – | | 32-Kbyte block | | 0.5 | 4 | s |
| – | | 64-Kbyte block | | 0.8 | 4 | s |
| $t_{PS}$ | Flash Memory Circuit Stabilization Wait Time | | | | 15 | µs |
| – | Data Hold Time (4) | | 10 | | | year |

NOTES:
1. Referenced to $V_{CC1}$=4.5 to 5.5V, 3.0 to 3.6V at Topr = 0 to 60 °C (U3, U5) unless otherwise specified.
2. Program and Erase Endurance refers to the number of times a block erase can be performed.
   If the program and erase endurance is 100, each block can be erased 100 times.
   For example, if a 4 Kbytes block A is erased after writing 1 word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data cannot be written to the same address more than once without erasing the block. (Rewrite prohibited)
3. Maximum number of E/W cycles for which operation is guaranteed.
4. Topr = -40 to 85 °C (U3) / -20 to 85 °C (U5).

**Table 5.5 Flash Memory Version Program / Erase Voltage and Read Operation Voltage Characteristics**

| Flash Program, Erase Voltage | Flash Read Operation Voltage |
|---|---|
| $V_{CC1}$ = 3.3 ± 0.3 V or 5.0 ± 0.5 ($T_{opr}$ = 0°C to 60°C ) | $V_{CC1}$=2.7 to 5.5 V ($T_{opr}$ = -40°C to 85°C (U3)<br>-20°C to 85°C (U5)) |

# $V_{CC1}=V_{CC2}=5V$

**Table 5.9 Electrical Characteristics(1)** (1)

| Symbol | Parameter | | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | HIGH Output Voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | $I_{OH}$=–5mA | $V_{CC}$–2.0 | | $V_{CC}$ | V |
| $V_{OH}$ | HIGH Output Voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | $I_{OH}$=–200µA | $V_{CC}$–0.3 | | $V_{CC}$ | V |
| $V_{OH}$ | HIGH Output Voltage XOUT | HIGHPOWER | $I_{OH}$=–1mA | $V_{CC}$–2.0 | | $V_{CC}$ | V |
| | | LOWPOWER | $I_{OH}$=–0.5mA | $V_{CC}$–2.0 | | $V_{CC}$ | |
| | HIGH Output Voltage XCOUT | HIGHPOWER | With no load applied | | 2.5 | | V |
| | | LOWPOWER | With no load applied | | 1.6 | | |
| $V_{OL}$ | LOW Output Voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | $I_{OL}$=5mA | | | 2.0 | V |
| $V_{OL}$ | LOW Output Voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | $I_{OL}$=200µA | | | 0.45 | V |
| $V_{OL}$ | LOW Output Voltage XOUT | HIGHPOWER | $I_{OL}$=1mA | | | 2.0 | V |
| | | LOWPOWER | $I_{OL}$=0.5mA | | | 2.0 | |
| | LOW Output Voltage XCOUT | HIGHPOWER | With no load applied | | 0 | | V |
| | | LOWPOWER | With no load applied | | 0 | | |
| $V_{T+}$-$V_{T-}$ | Hysteresis | TA0IN to TA2IN, TB0IN to TB2IN, $\overline{INT0}$ to $\overline{INT4}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, CLK0 to CLK2, TA0OUT to TA2OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD2, SCL0 to SCL2, SDA0 to SDA2 | | 0.2 | | 1.0 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{RESET}$ | | 0.2 | | 2.5 | V |
| $I_{IH}$ | HIGH Input Current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, $\overline{RESET}$, CNVSS, BYTE | $V_I$=5V | | | 5.0 | µA |
| $I_{IL}$ | LOW Input Current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, $\overline{RESET}$, CNVSS, BYTE | $V_I$=0V | | | –5.0 | µA |
| $R_{PULLUP}$ | Pull-Up Resistance | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | $V_I$=0V | 30 | 50 | 170 | kΩ |
| $R_{fXIN}$ | Feedback Resistance XIN | | | | 1.5 | | MΩ |
| $R_{fXCIN}$ | Feedback Resistance XCIN | | | | 15 | | MΩ |
| $V_{RAM}$ | RAM Retention Voltage | | At stop mode | 2.0 | | | V |

NOTES:
1. Referenced to $V_{CC1}=V_{CC2}$=4.2 to 5.5V, $V_{SS}$ = 0V at $T_{opr}$ = –20 to 85°C / –40 to 85°C, f(XIN) =16MHz unless otherwise specified.

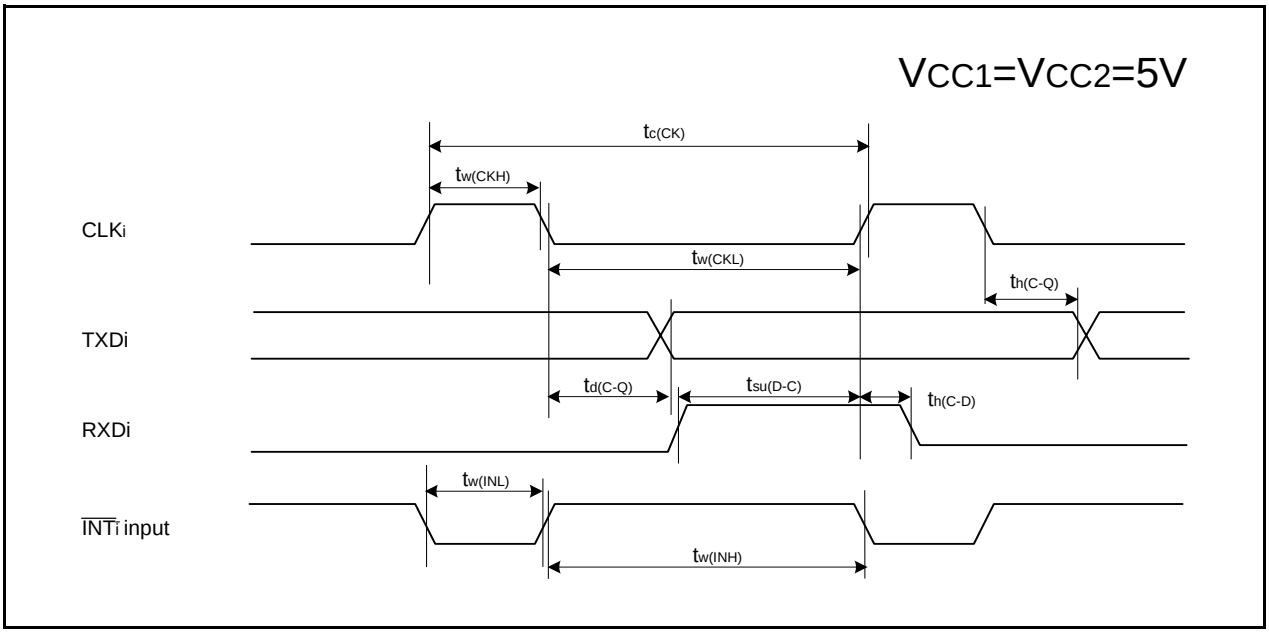



**Figure 5.4 Timing Diagram (2)**

# $V_{CC1}=V_{CC2}=3V$

## Timing Requirements

**($V_{CC1}$ = $V_{CC2}$ = 3V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

### Table 5.37 Timer B Input (Counter Input in Event Counter Mode)

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time (counted on one edge) | 150 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width (counted on one edge) | 60 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width (counted on one edge) | 60 | | ns |
| $t_{c(TB)}$ | TBiIN Input Cycle Time (counted on both edges) | 300 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width (counted on both edges) | 120 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width (counted on both edges) | 120 | | ns |

### Table 5.38 Timer B Input (Pulse Period Measurement Mode)

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time | 600 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width | 300 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width | 300 | | ns |

### Table 5.39 Timer B Input (Pulse Width Measurement Mode)

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time | 600 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width | 300 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width | 300 | | ns |

### Table 5.40 A/D Trigger Input

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(AD)}$ | $\overline{\text{ADTRG}}$ Input Cycle Time | 1500 | | ns |
| $t_{w(ADL)}$ | $\overline{\text{ADTRG}}$ Input LOW Pulse Width | 200 | | ns |

### Table 5.41 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi Input Cycle Time | 300 | | ns |
| $t_{w(CKH)}$ | CLKi Input HIGH Pulse Width | 150 | | ns |
| $t_{w(CKL)}$ | CLKi Input LOW Pulse Width | 150 | | ns |
| $t_{d(C-Q)}$ | TXDi Output Delay Time | | 160 | ns |
| $t_{h(C-Q)}$ | TXDi Hold Time | 0 | | ns |
| $t_{su(D-C)}$ | RXDi Input Setup Time | 100 | | ns |
| $t_{h(C-D)}$ | RXDi Input Hold Time | 90 | | ns |

### Table 5.42 External Interrupt $\overline{\text{INTi}}$ Input

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(INH)}$ | $\overline{\text{INTi}}$ Input HIGH Pulse Width | 380 | | ns |
| $t_{w(INL)}$ | $\overline{\text{INTi}}$ Input LOW Pulse Width | 380 | | ns |

# $V_{CC1}=V_{CC2}=3V$

## Switching Characteristics

**($V_{CC1}$ = $V_{CC2}$ = 3V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.43 Memory Expansion and Microprocessor Modes (for setting with no wait)**

| Symbol | Parameter | | Standard | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| td(BCLK-AD) | Address Output Delay Time | See **Figure 5.8** | | 30 | ns |
| th(BCLK-AD) | Address Output Hold Time (in relation to BCLK) | | 0 | | ns |
| th(RD-AD) | Address Output Hold Time (in relation to RD) | | 0 | | ns |
| th(WR-AD) | Address Output Hold Time (in relation to WR) | | (NOTE 2) | | ns |
| td(BCLK-CS) | Chip Select Output Delay Time | | | 30 | ns |
| th(BCLK-CS) | Chip Select Output Hold Time (in relation to BCLK) | | 0 | | ns |
| td(BCLK-ALE) | ALE Signal Output Delay Time | | | 25 | ns |
| th(BCLK-ALE) | ALE Signal Output Hold Time | | –4 | | ns |
| td(BCLK-RD) | RD Signal Output Delay Time | | | 30 | ns |
| th(BCLK-RD) | RD Signal Output Hold Time | | 0 | | ns |
| td(BCLK-WR) | WR Signal Output Delay Time | | | 30 | ns |
| th(BCLK-WR) | WR Signal Output Hold Time | | 0 | | ns |
| td(BCLK-DB) | Data Output Delay Time (in relation to BCLK) | | | 40 | ns |
| th(BCLK-DB) | Data Output Hold Time (in relation to BCLK) (3) | | 4 | | ns |
| td(DB-WR) | Data Output Delay Time (in relation to WR) | | (NOTE 1) | | ns |
| th(WR-DB) | Data Output Hold Time (in relation to WR) (3) | | (NOTE 2) | | ns |
| td(BCLK-HLDA) | HLDA Output Delay Time | | | 40 | ns |

NOTES:

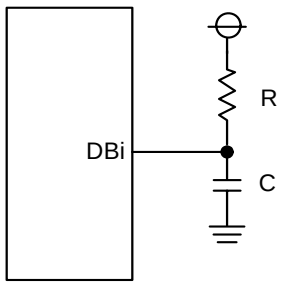
1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times10^{9}}{f(BCLK)} - 40[ns]$$ f(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times10^{9}}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
   Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
   Hold time of data bus is expressed in
   $t = -CR \times \ln(1 - V_{OL} / V_{CC1})$
   by a circuit of the right figure.
   For example, when $V_{OL}$ = 0.2$V_{CC1}$, C = 30pF, R = 1kΩ, hold time of output "L" level is
   $t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC1} / V_{CC1})$
   = 6.7ns.



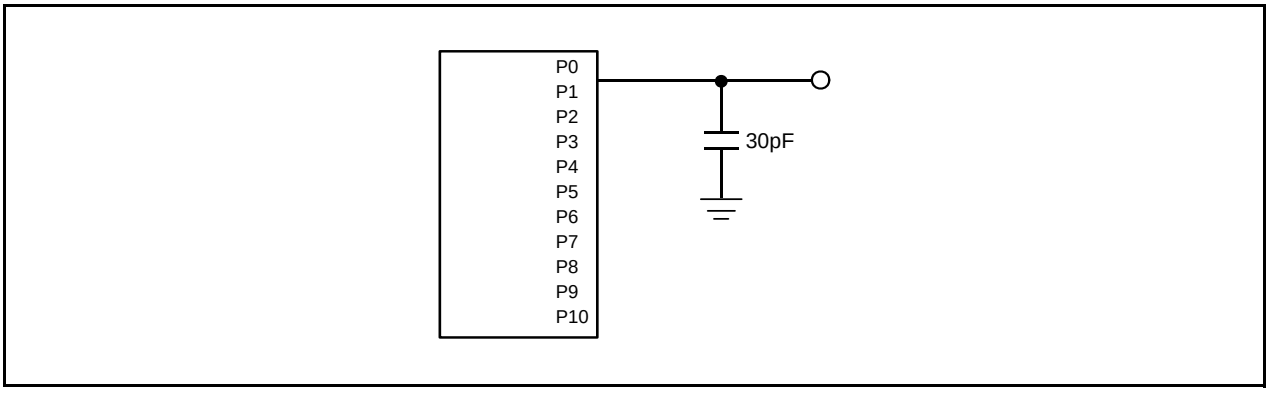
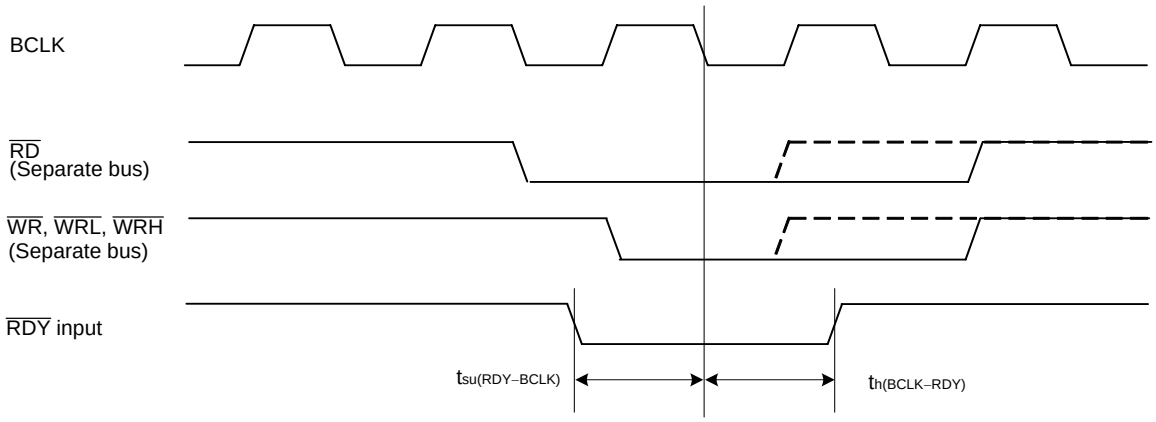




**Figure 5.8 Ports P0 to P10 Measurement Circuit**

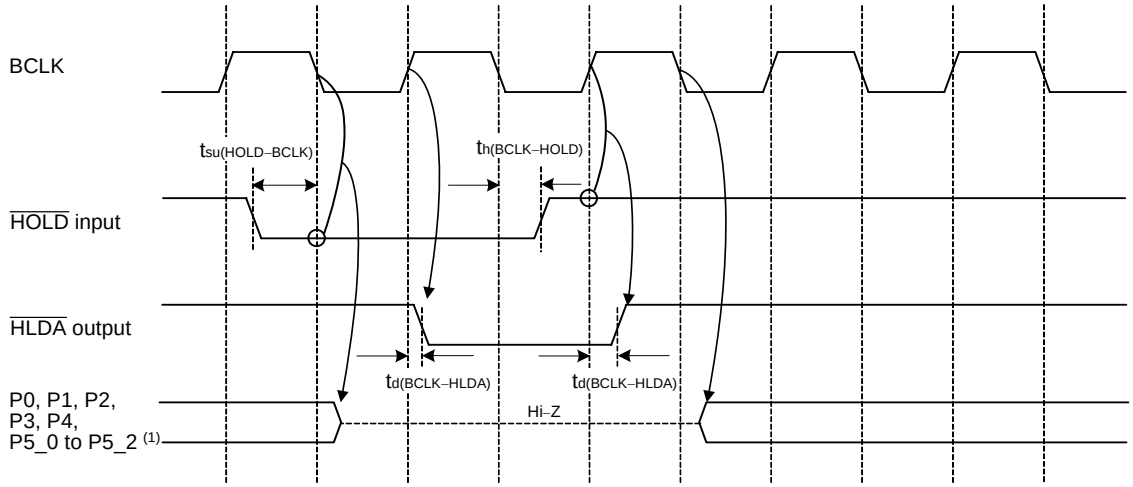
**Memory Expansion Mode, Microprocessor Mode**

$V_{CC1}=V_{CC2}=3V$

(Effective for setting with wait)




(Common to setting with wait and setting without wait)




NOTES:
1. These pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit in PM0 register.

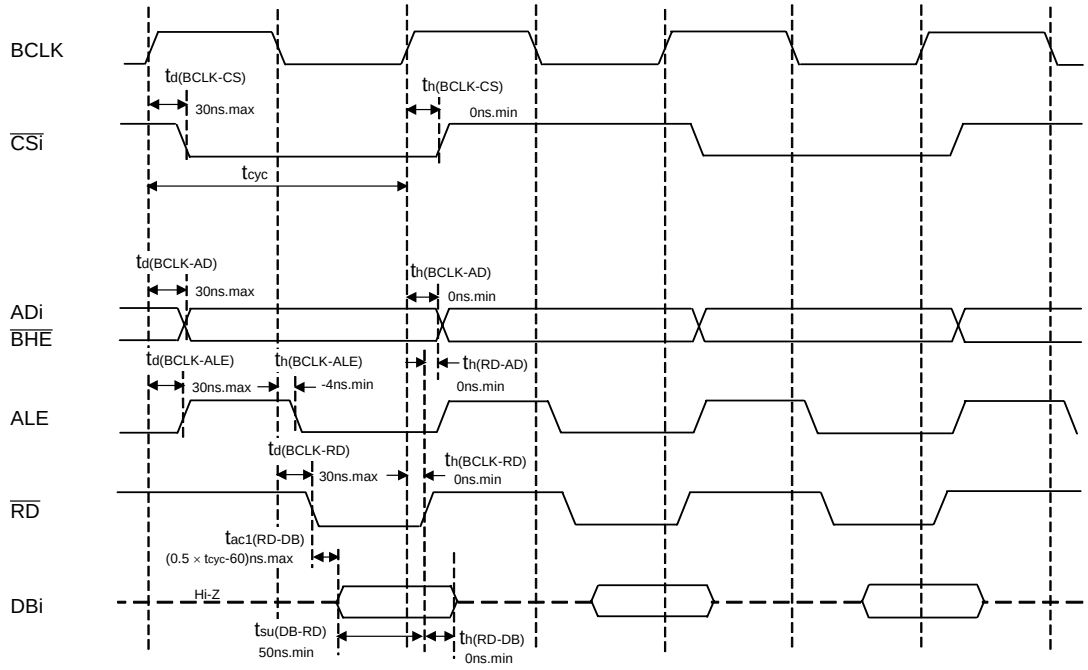
Measuring conditions :
· $V_{CC1}=V_{CC2}=3V$
· Input timing voltage : Determined with $V_{IL}=0.6V$, $V_{IH}=2.4V$
· Output timing voltage : Determined with $V_{OL}=1.5V$, $V_{OH}=1.5V$

**Figure 5.11 Timing Diagram (3)**

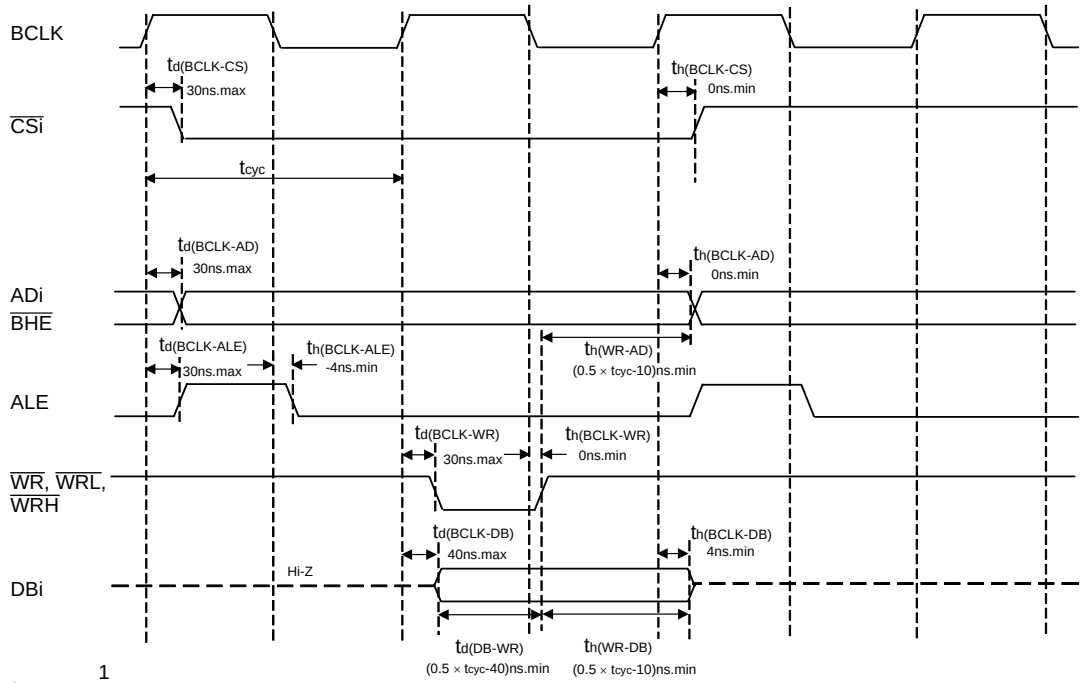
**Memory Expansion Mode, Microprocessor Mode**
**(**for setting with no wait**)**

$V_{CC1}=V_{CC2}=3V$

**Read timing**




**Write timing**




$$t_{cyc}=\frac{1}{f(BCLK)}$$

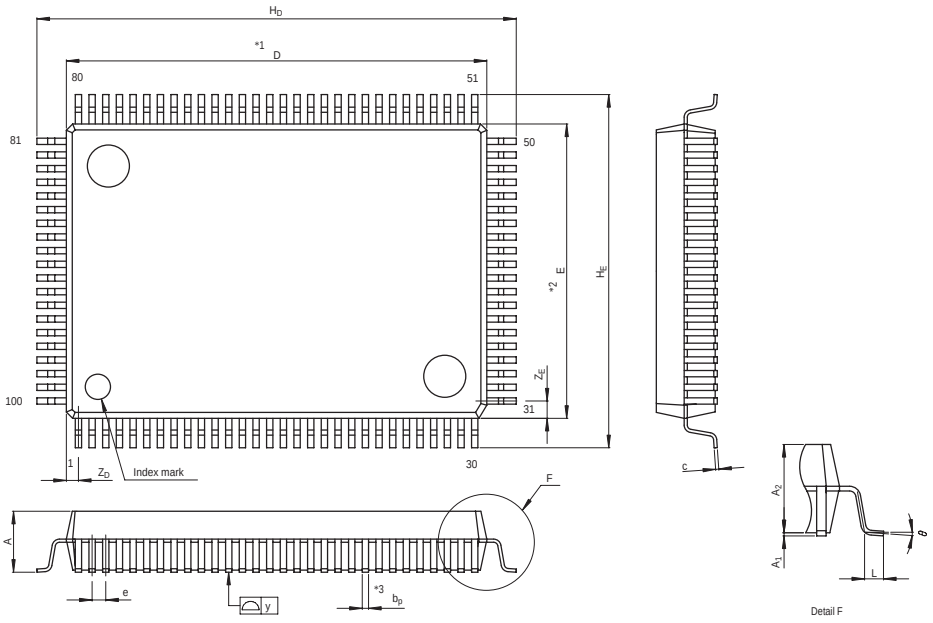
Measuring conditions
· $V_{CC1}=V_{CC2}=3V$
· Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
· Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

**Figure 5.12 Timing Diagram (4)**

# Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the "Packages" section of the Renesas Technology website.

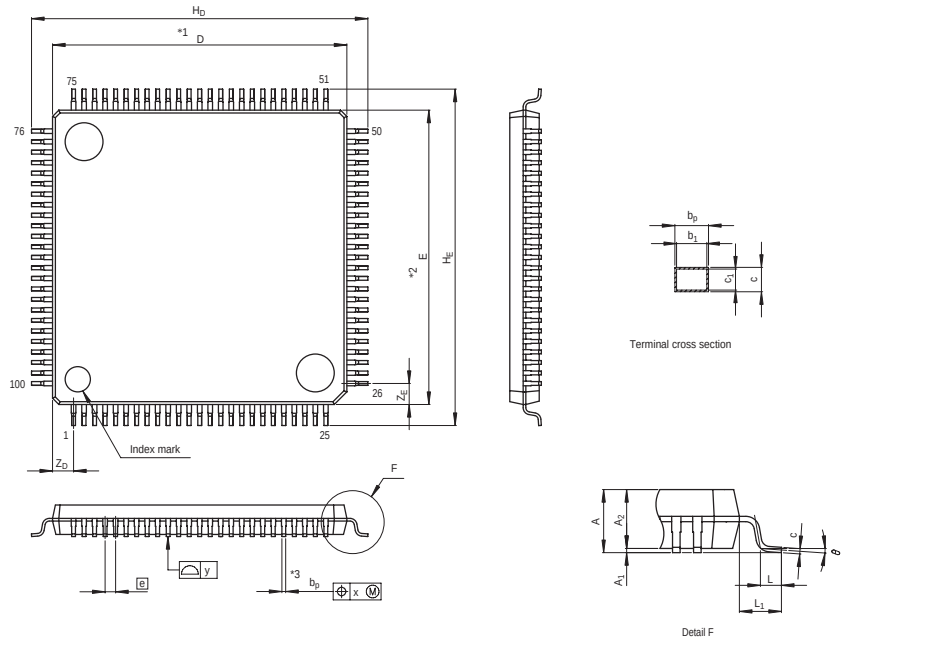
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-QFP100-14x20-0.65 | PRQP0100JB-A | 100P6S-A | 1.6g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 19.8 | 20.0 | 20.2 |
| E | 13.8 | 14.0 | 14.2 |
| $A_2$ | — | 2.8 | — |
| $H_D$ | 22.5 | 22.8 | 23.1 |
| $H_E$ | 16.5 | 16.8 | 17.1 |
| A | — | — | 3.05 |
| $A_1$ | 0 | 0.1 | 0.2 |
| $b_p$ | 0.25 | 0.3 | 0.4 |
| c | 0.13 | 0.15 | 0.2 |
| θ | 0° | — | 10° |
| e | 0.5 | 0.65 | 0.8 |
| y | — | — | 0.10 |
| $Z_D$ | — | 0.575 | — |
| $Z_E$ | — | 0.825 | — |
| L | 0.4 | 0.6 | 0.8 |

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP100-14x14-0.50 | PLQP0100KB-A | 100P6Q-A / FP-100U / FP-100UV | 0.6g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 15.8 | 16.0 | 16.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.25 |
| $b_1$ | — | 0.18 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $Z_D$ | — | 1.0 | — |
| $Z_E$ | — | 1.0 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

| REVISION HISTORY | M16C/30P Group Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 0.70 | Aug 26, 2004 | – | First Edition issued |
| 0.80 | Mar 18, 2005 | – | development support tools -> development tools |
| | | – | BCLK -> CPU clock |
| | | 2 | Table 1.1 Performance Outline of M16C/30P Group<br>Serial interface is revised. |
| | | 4 | Figure 1.2 Type., Memory Size, and Package is partly revised. |
| | | 8 | Table 1.4 Pin Detection (2) is partly revised. |
| | | 20 | Note 2 Table 5.3 A/D Conversion Characteristics is partly revised. |
| | | 21 | Symbol of Table 5.4 Power Supply Circuit Timing Characteristics is partly revised. |
| | | 22 | Table 5.5 Electrical Characteristics is revised. |
| | | 28 | Table 5.19 Electrical Characteristics is revised. |
| 1.00 | Sep 01, 2005 | 2 | Table 1.1 Performance Outline of M16C/30P Group is partly revised. |
| | | 4 | Table 1.2 Product List is partly revised. |
| | | | Figure 1.2 Type No., Memory Size, and Package is partly revised. |
| | | 5 | Figure 1.3 Pin Configuration is partly revised. |
| | | 6 | Figure 1.4 Pin Configuration is partly revised. |
| | | 7-8 | Tables 1.3 to 1.4 Pin Characteristics are added. |
| | | 9 | Table 1.5 Pin Description is revised. |
| | | 14 | 3. Memory is partly revised. |
| | | 15 | Table 4.1 SFR Information is partly revised. |
| | | 19 | Table 4.5 SFR Information is partly revised |
| | | 21 | Table 5.2 Recommended Operating Conditions is partly revised. |
| | | 22 | Table 5.3 A/D Conversion Characteristics is partly revised. |
| | | 25 | Note 1 is added in Table 5.6 External Clock Input (XIN input) |
| | | | Table 5.7 Memory Expansion Mode and Microprocessor Mode is added. |
| | | 28 | Table 5.20 Memory Expansion Mode and Microprocessor Modes (for setting with no wait) is added. |
| | | | Figure 5.2 Ports P0 to P10 Measurement Circuit is added. |
| | | 29 | Table 5.21 Memory Expansion Mode and Microprocessor Modes (for 1- to 3-wait setting and external area access) is added. |
| | | 32 | Figure 5.5 Timing Diagram (3) is added. |
| | | 33 | Figure 5.6 Timing Diagram (4) is added. |
| | | 34 | Figure 5.7 Timing Diagram (5) is added. |
| | | 36 | Note 1 to 4 are added in Table 5.23 External Clock Input (XIN input) |
| | | | Table 5.24 Memory Expansion Mode and Microprocessor Mode is added. |
| | | 39 | Table 5.37 Memory Expansion Mode and Microprocessor Modes (for setting with no wait) is added. |
| | | | Figure 5.8 Ports P0 to P10 Measurement Circuit is added. |
| | | 40 | Table 5.38 Memory Expansion Mode and Microprocessor Modes (for 1- to 3-wait setting and external area access) is added. |
| | | 43 | Figure 5.11 Timing Diagram (3) is added. |

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| | | 44 | Figure 5.12 Timing Diagram (4) is added. |
| | | 45 | Figure 5.13 Timing Diagram (5) is added. |
| 1.10 | Oct 01, 2005 | 2 | Table 1.1 Performance Outline of M16C/30P Group is partly revised. |
| | | 4 | Table 1.2 Product List is partly revised. |
| | | | Figure 1.2 Type No., Memory Size, and Package is partly revised. |
| | | 5 | Table 1.3 Product Code of Mask ROM version Version for M16C/30P is added. |
| | | | Figure 1.3 Marking Diagram of Mask ROM Version for M16C/30P is added. |
| | | 6 | Figure 1.4 Marking Diagram of ROM -less Version for M16C/30P is added. |
| | | 6 | Table 1.4 Product Code of ROM-less version for M16C/30P is added. |
| | | 16 | Figure 3.1 Memory Map is partly added. |
| | | 23 | Table 5.2 information is revised. |
| 1.11 | May 31, 2006 | 4 | 1.4 Product List information is revised. |
| | | | Table 1.2 Product List is partly revised. |
| | | 5 | Figure 1.2 Type No., Memory Size, and Package is partly added. |
| | | 7 | Table 1.4 Product Code of Flash Memory version and ROM-less version for M16C/30P is partly revised. |
| | | | Figure 1.4 Marking Diagram of Flash Memory version and ROM-less Version for M16C/30P (Top View) is partly added. |
| | | 17 | 3. Memory information is revised. |
| | | | Figure 3.1 Memory Map is partly revised. |
| | | 18 | Table 4.1 SFR Information(1) is partly revised. |
| | | 19 | Table 4.2 SFR Information(2) is partly added. |
| | | 23 | Table 5.1 Absolute Maximum Ratings information is revised. |
| | | 26 | Table 5.4 Flash Memory Version Electrical Characteristics is added. |
| | | | Table 5.5 Flash Memory Version Program / Erase Voltage and Read Operation Voltage Characteristics is added. |
| | | 28 | Table 5.7 Electrical Characteristics(1) is partly deleted. |
| | | 29 | Table 5.8 Electrical Characteristics (2) is partly revised. |
| | | 33 | Table 5.23 Memory Expansion and Microprocessor Modes NOTES 3 is partly revised. |
| | | 34 | Table 5.24 Memory Expansion and Microprocessor Modes NOTES 3 is partly revised. |
| | | 40 | Table 5.25 Electrical Characteristics (1) is partly deleted. |
| | | 41 | Table 5.26 Electrical Characteristics (2) is partly revised. |
| | | 45 | Table 5.41 Memory Expansion and Microprocessor Modes NOTES 3 is partly revised. |
| | | 46 | Table 5.42 Memory Expansion and Microprocessor Modes NOTES 3 is partly revised. |