Renesas - M30302SPFP#U3 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M16C/30
Core Size	16-Bit
Speed	16MHz
Connectivity	I²C, IEBus, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	87
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 18x10b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30302spfp-u3

1. Overview

The M16C/30P Group of single-chip microcomputers is built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and is packaged in a 100-pin plastic molded QFP.
These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed. In addition, these microcomputers contain a multiplier and DMAC which combined with fast instruction processing capability, make it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

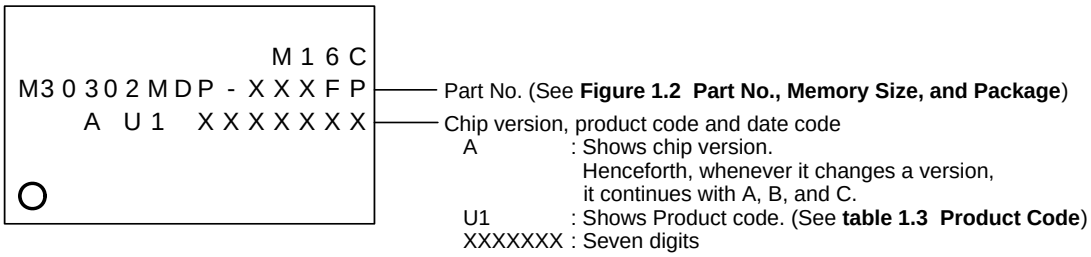
Audio, cameras, TV, home appliance, office/communications/portable/industrial equipment, etc.

Table 1.4 Product Code of MASK ROM version for M16C/30P

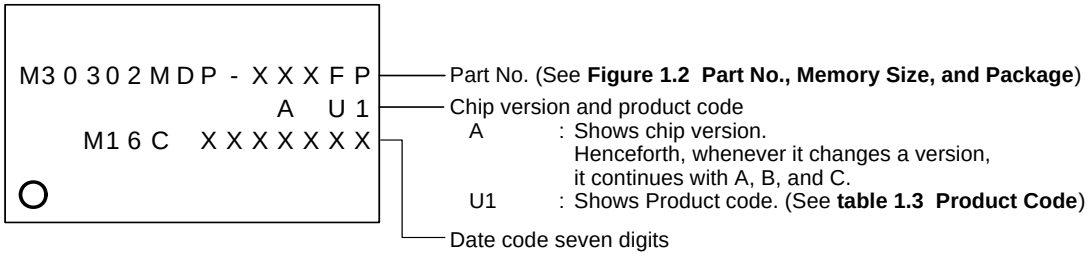
Product Code	Package	Operating Ambient Temperature
U1	Lead-free	-20°C to 85°C
U4		-40°C to 85°C

PRQP0100JB-A (100P6S-A)

1. Standard Renesas Mark

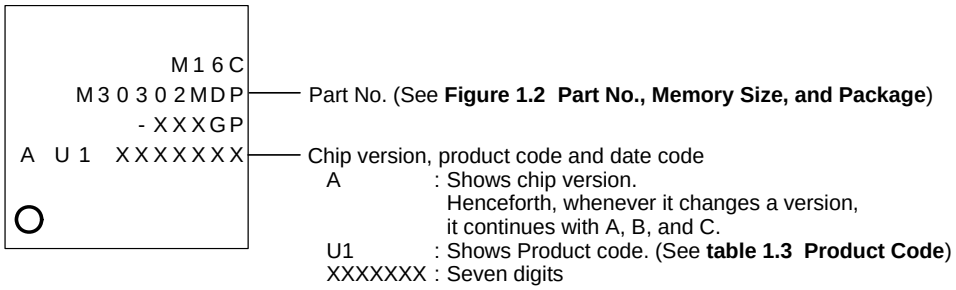


2. Customer's Parts Number + Renesas catalog name

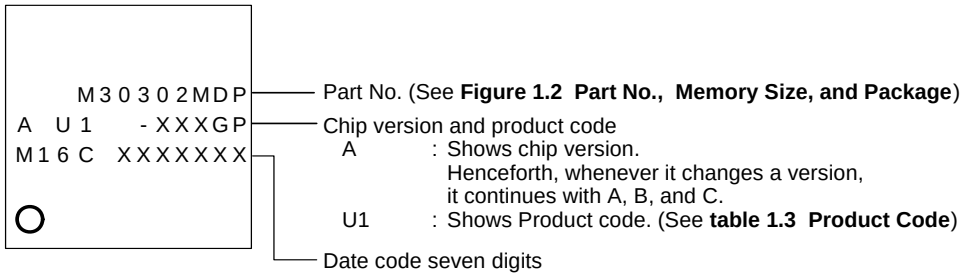


PLQP0100KB-A (100P6Q-A)

1. Standard Renesas Mark



2. Customer's Parts Number + Renesas catalog name



NOTES:
1. Refer to the **mark specification form** for details of the Mask ROM version marking.

Figure 1.3 Marking Diagram of Mask ROM Version for M16C/30P (Top View)

Table 1.6 Pin Characteristics (1)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
FP	GP							
1	99		P9_6				ANEX1	
2	100		P9_5				ANEX0	
3	1		P9_4					
4	2		P9_3					
5	3		P9_2		TB2IN			
6	4		P9_1		TB1IN			
7	5		P9_0		TB0IN			
8	6	BYTE						
9	7	CNVSS						
10	8	XCIN	P8_7					
11	9	XCOUT	P8_6					
12	10	$\overline{\text{RESET}}$						
13	11	XOUT						
14	12	VSS						
15	13	XIN						
16	14	VCC1						
17	15		P8_5	$\overline{\text{NMI}}$				
18	16		P8_4	$\overline{\text{INT2}}$				
19	17		P8_3	$\overline{\text{INT1}}$				
20	18		P8_2	$\overline{\text{INT0}}$				
21	19		P8_1					
22	20		P8_0					
23	21		P7_7					
24	22		P7_6					
25	23		P7_5		TA2IN			
26	24		P7_4		TA2OUT			
27	25		P7_3		TA1IN	$\overline{\text{CTS2}}/\overline{\text{RTS2}}$		
28	26		P7_2		TA1OUT	CLK2		
29	27		P7_1		TA0IN	RXD2/SCL2		
30	28		P7_0		TA0OUT	TXD2/SDA2		
31	29		P6_7			TXD1/SDA1		
32	30		P6_6			RXD1/SCL1		
33	31		P6_5			CLK1		
34	32		P6_4			$\overline{\text{CTS1}}/\overline{\text{RTS1}}/\overline{\text{CTS0}}$/CLKS1		
35	33		P6_3			TXD0/SDA0		
36	34		P6_2			RXD0/SCL0		
37	35		P6_1			CLK0		
38	36		P6_0			$\overline{\text{CTS0}}/\overline{\text{RTS0}}$		
39	37		P5_7					$\overline{\text{RDY}}$/CLKOUT
40	38		P5_6					ALE
41	39		P5_5					$\overline{\text{HOLD}}$
42	40		P5_4					$\overline{\text{HLDA}}$
43	41		P5_3					BCLK
44	42		P5_2					$\overline{\text{RD}}$
45	43		P5_1					$\overline{\text{WRH}}/\overline{\text{BHE}}$
46	44		P5_0					$\overline{\text{WRL}}/\overline{\text{WR}}$
47	45		P4_7					$\overline{\text{CS3}}$
48	46		P4_6					$\overline{\text{CS2}}$
49	47		P4_5					$\overline{\text{CS1}}$
50	48		P4_4					$\overline{\text{CS0}}$

1.6 Pin Description

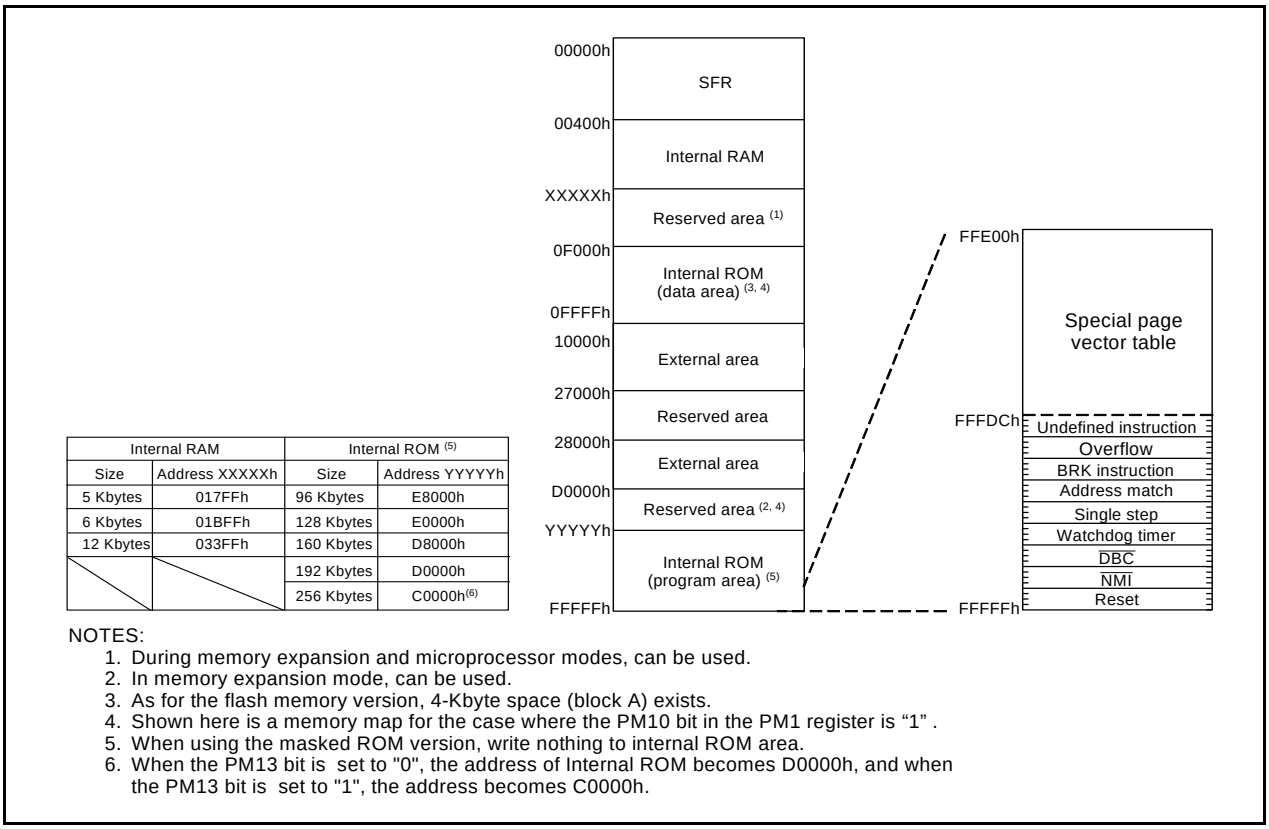
Table 1.8 Pin Description (1)

Signal Name	Pin Name	I/O Type	Description
Power supply input	VCC1, VCC2 VSS	I	Apply 2.7 to 5.5 V to the VCC1 and VCC2 pins and 0 V to the VSS pin. The VCC apply condition is that VCC1 = VCC2.
Analog power supply input	AVCC AVSS	I	Applies the power supply for the A/D converter. Connect the AVCC pin to VCC1. Connect the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	The microcomputer is in a reset state when applying “L” to the this pin.
CNVSS	CNVSS	I	Switches processor mode. Connect this pin to VSS to when after a reset to start up in single-chip mode. Connect this pin to VCC1 to start up in microprocessor mode.
External data bus width select input	BYTE	I	Switches the data bus in external memory space. The data bus is 16 bits long when the this pin is held "L" and 8 bits long when the this pin is held "H". Set it to either one. Connect this pin to VSS when an single-chip mode.
Bus control pins	D0 to D7	I/O	Inputs and outputs data (D0 to D7) when these pins are set as the separate bus.
	D8 to D15	I/O	Inputs and outputs data (D8 to D15) when external 16-bit data bus is set as the separate bus.
	A0 to A19	O	Output address bits (A0 to A19).
	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	Output $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ signals. $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ are chip-select signals to specify an external space.
	$\overline{\text{WRL}}$/$\overline{\text{WR}}$ $\overline{\text{WRH}}$/$\overline{\text{BHE}}$ $\overline{\text{RD}}$	O	Output $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, ($\overline{\text{WR}}$, $\overline{\text{BHE}}$), $\overline{\text{RD}}$ signals. $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ or $\overline{\text{BHE}}$ and $\overline{\text{WR}}$ can be switched by program. • $\overline{\text{WRL}}$, $\overline{\text{WRH}}$ and $\overline{\text{RD}}$ are selected The $\overline{\text{WRL}}$ signal becomes "L" by writing data to an even address in an external memory space. The $\overline{\text{WRH}}$ signal becomes "L" by writing data to an odd address in an external memory space. The $\overline{\text{RD}}$ pin signal becomes "L" by reading data in an external memory space. • $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ are selected The $\overline{\text{WR}}$ signal becomes "L" by writing data in an external memory space. The $\overline{\text{RD}}$ signal becomes "L" by reading data in an external memory space. The $\overline{\text{BHE}}$ signal becomes "L" by accessing an odd address. Select $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ for an external 8-bit data bus.
	ALE	O	ALE is a signal to latch the address.
	$\overline{\text{HOLD}}$	I	While the $\overline{\text{HOLD}}$ pin is held "L", the microcomputer is placed in a hold state.
	$\overline{\text{HLDA}}$	O	In a hold state, $\overline{\text{HLDA}}$ outputs a "L" signal.
	$\overline{\text{RDY}}$	I	While applying a "L" signal to the $\overline{\text{RDY}}$ pin, the microcomputer is placed in a wait state.

I : Input O : Output I/O : Input and output

3. Memory

Figure 3.1 is a Memory Map of the M16C/30P group. The address space extends the 1 Mbyte from address 00000h to FFFFFh.
The internal ROM is allocated in a lower address direction beginning with address FFFFFh. For example, a 64-Kbyte internal ROM is allocated to the addresses from F0000h to FFFFFh.
The fixed interrupt vector table is allocated to the addresses from FFFDCh to FFFFFh. Therefore, store the start address of each interrupt routine here.
The internal RAM is allocated in an upper address direction beginning with address 00400h. For example, a 5-Kbyte internal RAM is allocated to the addresses from 00400h to 017FFh. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated. The SFR is allocated to the addresses from 00000h to 003FFh. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be used by users.
The special page vector table is allocated to the addresses from FFE00h to FFFDBh. This vector is used by the JMPS or JSRS instruction. For details, refer to the **M16C/60 and M16C/20 Series Software Manual**.



Internal RAM		Internal ROM (5)	
Size	Address XXXXXh	Size	Address YYYYYh
5 Kbytes	017FFh	96 Kbytes	E8000h
6 Kbytes	01BFFh	128 Kbytes	E0000h
12 Kbytes	033FFh	160 Kbytes	D8000h
		192 Kbytes	D0000h
		256 Kbytes	C0000h(6)

NOTES:
1. During memory expansion and microprocessor modes, can be used.
2. In memory expansion mode, can be used.
3. As for the flash memory version, 4-Kbyte space (block A) exists.
4. Shown here is a memory map for the case where the PM10 bit in the PM1 register is “1” .
5. When using the masked ROM version, write nothing to internal ROM area.
6. When the PM13 bit is set to "0", the address of Internal ROM becomes D0000h, and when the PM13 bit is set to "1", the address becomes C0000h.

Figure 3.1 Memory Map

4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.5 list the SFR information.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0 (2)	PM0	00000000b(CNVSS pin is "L") 00000011b(CNVSS pin is "H")
0005h	Processor Mode Register 1	PM1	00XXX0X0b
0006h	System Clock Control Register 0	CM0	01001000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Chip Select Control Register	CSR	00000001b
0009h	Address Match Interrupt Enable Register	AIER	XXXXXX00b
000Ah	Protect Register	PRCR	XX000000b
000Bh			
000Ch			
000Dh			
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00XXXXXXb
0010h 0011h 0012h	Address Match Interrupt Register 0	RMAD0	00h 00h X0h
0013h			
0014h 0015h 0016h	Address Match Interrupt Register 1	RMAD1	00h 00h X0h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch			
001Dh			
001Eh			
001Fh			
0020h 0021h 0022h	DMA0 Source Pointer	SAR0	XXh XXh XXh
0023h			
0024h 0025h 0026h	DMA0 Destination Pointer	DAR0	XXh XXh XXh
0027h			
0028h 0029h	DMA0 Transfer Counter	TCR0	XXh XXh
002Ah			
002Bh			
002Ch	DMA0 Control Register	DM0CON	00000X00b
002Dh			
002Eh			
002Fh			
0030h 0031h 0032h	DMA1 Source Pointer	SAR1	XXh XXh XXh
0033h			
0034h 0035h 0036h	DMA1 Destination Pointer	DAR1	XXh XXh XXh
0037h			
0038h 0039h	DMA1 Transfer Counter	TCR1	XXh XXh
003Ah			
003Bh			
003Ch	DMA1 Control Register	DM1CON	00000X00b
003Dh			
003Eh			
003Fh			

NOTES:
1. The blank areas are reserved and cannot be accessed by users.
2. The PM00 and PM01 bits do not change at software reset.

X : Nothing is mapped to this bit

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0340h			
0341h			
0342h			
0343h			
0344h			
0345h			
0346h			
0347h			
0348h			
0349h			
034Ah			
034Bh			
034Ch			
034Dh			
034Eh			
034Fh			
0350h			
0351h			
0352h			
0353h			
0354h			
0355h			
0356h			
0357h			
0358h			
0359h			
035Ah			
035Bh			
035Ch			
035Dh			
035Eh	Interrupt Factor Select Register 2	IFSR2A	00XXXXXXb
035Fh	Interrupt Factor Select Register	IFSR	00h
0360h			
0361h			
0362h			
0363h			
0364h			
0365h			
0366h			
0367h			
0368h			
0369h			
036Ah			
036Bh			
036Ch	UART0 Special Mode Register 4	U0SMR4	00h
036Dh	UART0 Special Mode Register 3	U0SMR3	000X0X0Xb
036Eh	UART0 Special Mode Register 2	U0SMR2	X0000000b
036Fh	UART0 Special Mode Register	U0SMR	X0000000b
0370h	UART1 Special Mode Register 4	U1SMR4	00h
0371h	UART1 Special Mode Register 3	U1SMR3	000X0X0Xb
0372h	UART1 Special Mode Register 2	U1SMR2	X0000000b
0373h	UART1 Special Mode Register	U1SMR	X0000000b
0374h	UART2 Special Mode Register 4	U2SMR4	00h
0375h	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
0376h	UART2 Special Mode Register 2	U2SMR2	X0000000b
0377h	UART2 Special Mode Register	U2SMR	X0000000b
0378h	UART2 Transmit/Receive Mode Register	U2MR	00h
0379h	UART2 Bit Rate Generator	U2BRG	XXh
037Ah 037Bh	UART2 Transmit Buffer Register	U2TB	XXh XXh
037Ch	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
037Dh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
037Eh 037Fh	UART2 Receive Buffer Register	U2RB	XXh XXh

NOTES:
1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Table 5.3 A/D Conversion Characteristics (1)

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		$V_{REF}=V_{CC}$				10	Bits
INL	Integral Non-Linearity Error	10bit	$V_{REF}=V_{CC}=5V$	AN0 to AN7 input, AN0_0 to AN0_7 input, ANEX0, ANEX1 input			±5	LSB
			$V_{REF}=V_{CC}=3.3V$	AN0 to AN7 input, AN0_0 to AN0_7 input, ANEX0, ANEX1 input			±7	LSB
		8bit	$V_{REF}=V_{CC}=5V, 3.3V$				±2	LSB
–	Absolute Accuracy	10bit	$V_{REF}=V_{CC}=5V$	AN0 to AN7 input, AN0_0 to AN0_7 input, ANEX0, ANEX1 input			±5	LSB
			$V_{REF}=V_{CC}=3.3V$	AN0 to AN7 input, AN0_0 to AN0_7 input, ANEX0, ANEX1 input			±7	LSB
		8bit	$V_{REF}=V_{CC}=5V, 3.3V$				±2	LSB
–	Tolerance Level Impedance					3		kΩ
DNL	Differential Non-Linearity Error						±2	LSB
–	Offset Error						±5	LSB
–	Gain Error						±5	LSB
R_{LADDER}	Ladder Resistance		$V_{REF}=V_{CC}$		10		40	kΩ
t_{CONV}	10-bit Conversion Time, Sample & Hold Function Available		$V_{REF}=V_{CC}=5V$, ϕAD=10MHz		3.3			µs
t_{CONV}	8-bit Conversion Time, Sample & Hold Function Available		$V_{REF}=V_{CC}=5V$, ϕAD=10MHz		2.8			µs
t_{SAMP}	Sampling Time				0.3			µs
V_{REF}	Reference Voltage				3.0		V_{CC}	V
V_{IA}	Analog Input Voltage				0		V_{REF}	V

NOTES:
1. Referenced to $V_{CC}=AV_{CC}=V_{REF}=3.3$ to 5.5V, $V_{SS}=AV_{SS}=0V$ at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified.
2. ϕAD frequency must be 10 MHz or less.
3. When sample & hold function is disabled, ϕAD frequency must be 250 kHz or more, in addition to the limitation in Note 2.
4. When sample & hold function is enabled, ϕAD frequency must be 1MHz or more, in addition to the limitation in Note 2.

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.11 External Clock Input (XIN input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	62.5		ns
$t_{w(H)}$	External Clock Input HIGH Pulse Width	25		ns
$t_{w(L)}$	External Clock Input LOW Pulse Width	25		ns
t_r	External Clock Rise Time		15	ns
t_f	External Clock Fall Time		15	ns

NOTES:
1. The condition is V_{CC1}=V_{CC2}=3.0 to 5.0V.

Table 5.12 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (for setting with no wait)		(NOTE 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (for setting with wait)		(NOTE 2)	ns
$t_{su(DB-RD)}$	Data Input Setup Time	40		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ Input Setup Time	30		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ Input Setup Time	40		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ Input Hold Time	0		ns

NOTES:
1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 45[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(BCLK)} - 45[ns]$$ n is "2" for 1-wait setting.

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.19 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on both edges)	80		ns

Table 5.20 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	200		ns

Table 5.21 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	200		ns

Table 5.22 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{\text{ADTRG}}$ Input Cycle Time	1000		ns
$t_{w(ADL)}$	$\overline{\text{ADTRG}}$ input LOW Pulse Width	125		ns

Table 5.23 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input HIGH Pulse Width	100		ns
$t_{w(CKL)}$	CLKi Input LOW Pulse Width	100		ns
$t_{d(C-Q)}$	TXDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TXDi Hold Time	0		ns
$t_{su(D-C)}$	RXDi Input Setup Time	70		ns
$t_{h(C-D)}$	RXDi Input Hold Time	90		ns

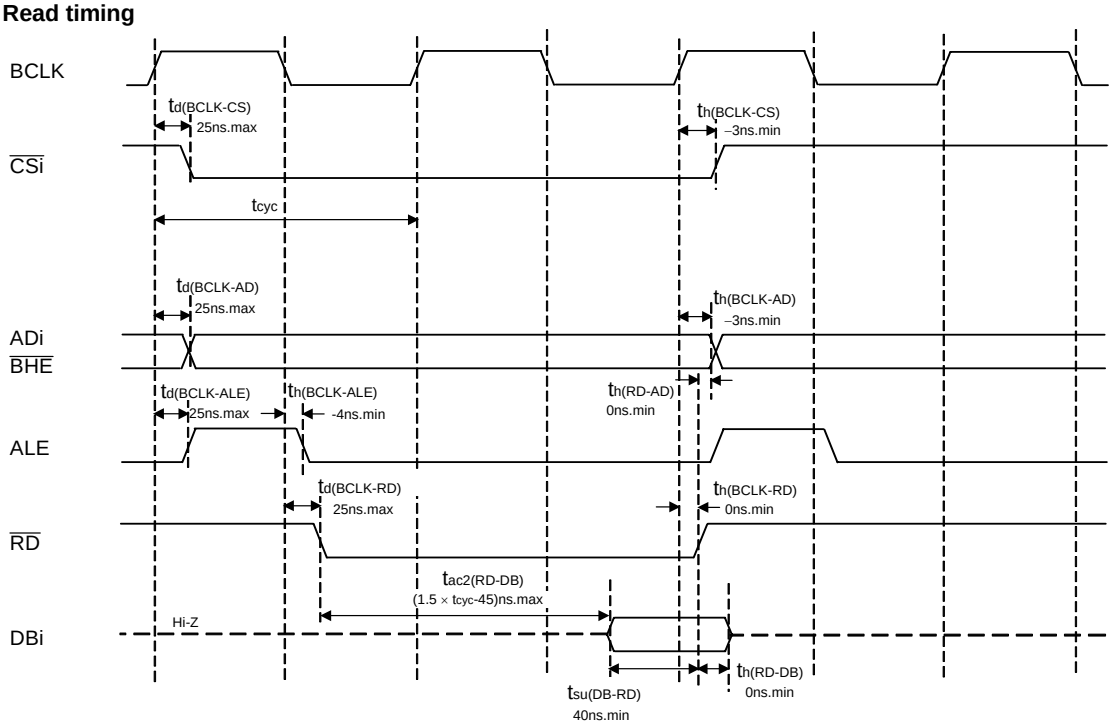
Table 5.24 External Interrupt $\overline{\text{INTi}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{\text{INTi}}$ Input HIGH Pulse Width	250		ns
$t_{w(INL)}$	$\overline{\text{INTi}}$ Input LOW Pulse Width	250		ns

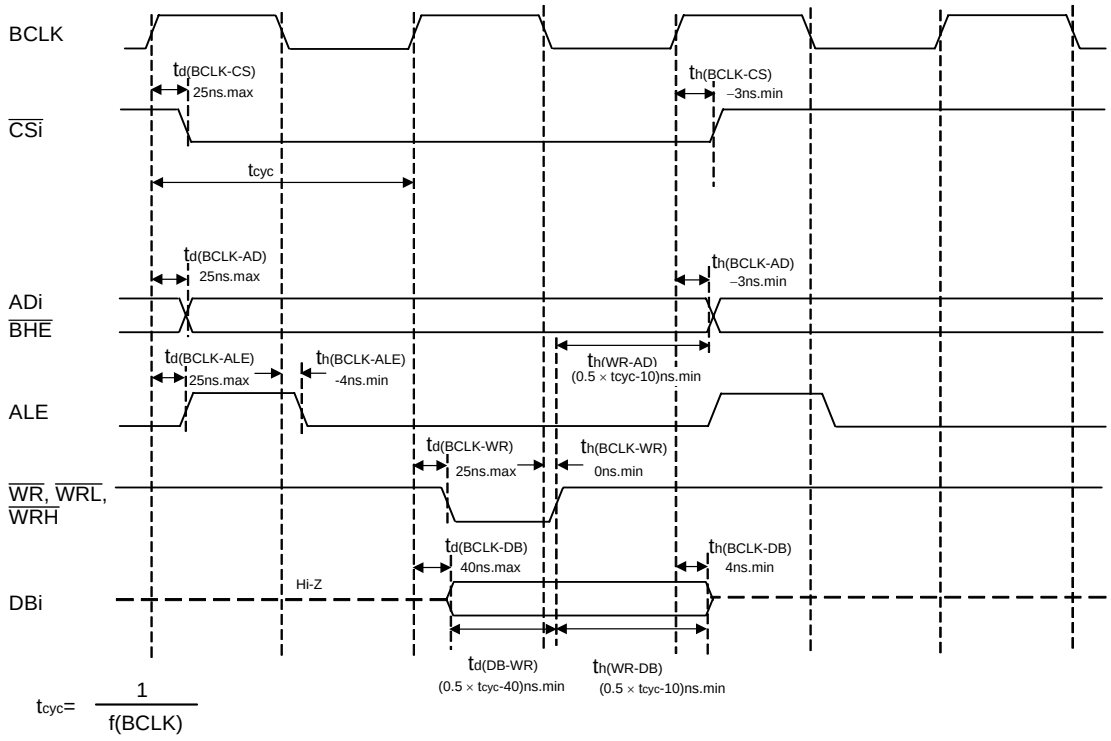
$V_{CC1}=V_{CC2}=5V$

Memory Expansion Mode, Microprocessor Mode
(for 1-wait setting and external area access**)**

Read timing



Write timing



$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
· Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

Figure 5.7 Timing Diagram (5)

Table 5.28 Electrical Characteristics (2) (1)

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
I_{CC}	Power Supply Current (V_{CC1}=V_{CC2}=2.7V to 3.6V)	In single-chip mode, the output pins are open and other pins are V_{SS}	Mask ROM	f(XIN)=10MHz No division		8	11	mA
			One Time Flash	f(XIN)=10MHz, No division		8	13	mA
			Flash Memory	f(XIN)=10MHz, No division		8	13	mA
			Flash Memory Program	f(XIN)=10MHz, VCC1=3.0V		12		mA
			One Time Flash Program	f(XIN)=10MHz, VCC1=3.0V		12		mA
			Flash Memory Erase	f(XIN)=10MHz, VCC1=3.0V		22		mA
			Mask ROM	f(XCIN)=32kHz Low power dissipation mode, ROM (3)		25		µA
			One Time Flash	f(XCIN)=32kHz Low power dissipation mode, RAM (3)		25		µA
				f(XCIN)=32kHz Low power dissipation mode, Flash Memory (3)		350		µA
			Flash Memory	f(XCIN)=32kHz Low power dissipation mode, RAM (3)		25		µA
				f(XCIN)=32kHz Low power dissipation mode, Flash Memory (3)		420		µA
			Mask ROM One Time Flash Flash Memory	f(XCIN)=32kHz Wait mode (2), Oscillation capability High		6.0		µA
				f(XCIN)=32kHz Wait mode (2), Oscillation capability Low		1.8		µA
				Stop mode Topr =25°C		0.7	3.0	µA

NOTES:
1. Referenced to V_{CC1}=V_{CC2}=2.7 to 3.3V, V_{SS} = 0V at T_{opr} = –20 to 85°C / –40 to 85°C, f(XIN)=10MHz unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.

$V_{CC1}=V_{CC2}=3V$

Timing Requirements

(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.29 External Clock Input (XIN input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	(NOTE 2)		ns
$t_{w(H)}$	External Clock Input HIGH Pulse Width	(NOTE 3)		ns
$t_{w(L)}$	External Clock Input LOW Pulse Width	(NOTE 3)		ns
t_r	External Clock Rise Time		(NOTE 4)	ns
t_f	External Clock Fall Time		(NOTE 4)	ns

NOTES:

1. The condition is V_{CC1}=V_{CC2}=2.7 to 3.0V.
2. Calculated according to the V_{CC1} voltage as follows:

$$\frac{10^{-6}}{20 \times V_{CC1} - 44} \text{ [ns]}$$

3. Calculated according to the V_{CC1} voltage as follows:

$$\frac{10^{-6}}{20 \times V_{CC1} - 44} \times 0.4 \text{ [ns]}$$

4. Calculated according to the V_{CC1} voltage as follows:

$$-10 \times V_{CC1} + 45 \text{ [ns]}$$

Table 5.30 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (for setting with no wait)		(NOTE 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (for setting with wait)		(NOTE 2)	ns
$t_{su(DB-RD)}$	Data Input Setup Time	50		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ Input Setup Time	40		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ Input Setup Time	50		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ Input Hold Time	0		ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 60 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(BCLK)} - 60 \text{ [ns]}$$ n is "2" for 1-wait setting.

$V_{CC1}=V_{CC2}=3V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.44 Memory Expansion and Microprocessor Modes (for 1 wait setting and external area access)

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See **Figure 5.8**		30	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address Output Hold Time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
$t_{d(BCLK-CS)}$	Chip Select Output Delay Time			30	ns
$t_{h(BCLK-CS)}$	Chip Select Output Hold Time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE Signal Output Delay Time			25	ns
$t_{h(BCLK-ALE)}$	ALE Signal Output Hold Time		-4		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			30	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		0		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			30	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(BCLK-DB)}$	Data Output Delay Time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data Output Hold Time (in relation to BCLK) (3)		4		ns
$t_{d(DB-WR)}$	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
th(WR-DB)	Data Output Hold Time (in relation to WR)(3)		(NOTE 2)		ns
$t_{d(BCLK-HLDA)}$	HLDA Output Delay Time			40	ns

NOTES:

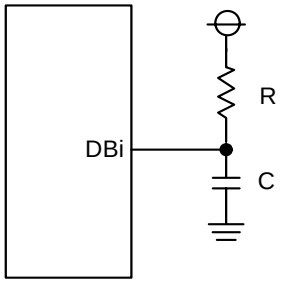
1. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5)\times 10^9}{f(BCLK)} - 40[ns]$$ n is “1” for 1-wait setting, f(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f(BCLK)} - 10[ns]$$

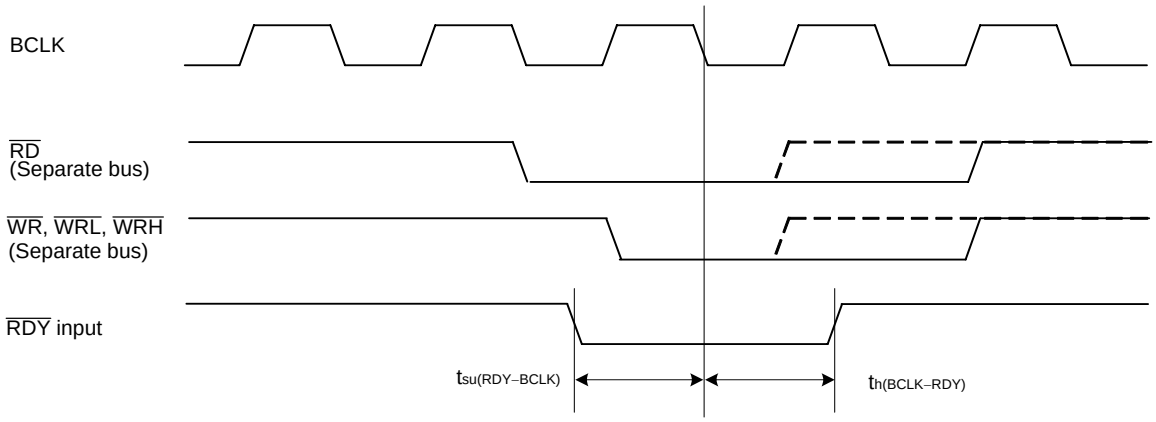
3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
   Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
   Hold time of data bus is expressed in
   $t = -CR \times \ln(1 - V_{OL} / V_{CC1})$
   by a circuit of the right figure.
   For example, when $V_{OL} = 0.2V_{CC1}$, C = 30pF, R = 1kΩ, hold time of output ”L” level is
   $t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC1} / V_{CC1})$
   = 6.7ns.



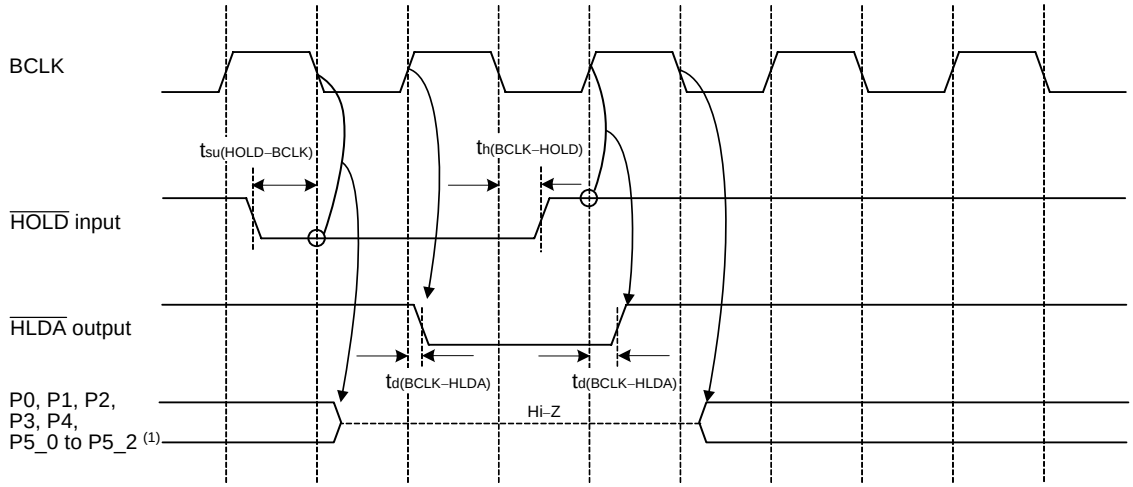
Memory Expansion Mode, Microprocessor Mode

$V_{CC1}=V_{CC2}=3V$

(Effective for setting with wait)



(Common to setting with wait and setting without wait)



NOTES:
1. These pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit in PM0 register.

Measuring conditions :
· $V_{CC1}=V_{CC2}=3V$
· Input timing voltage : Determined with $V_{IL}=0.6V$, $V_{IH}=2.4V$
· Output timing voltage : Determined with $V_{OL}=1.5V$, $V_{OH}=1.5V$

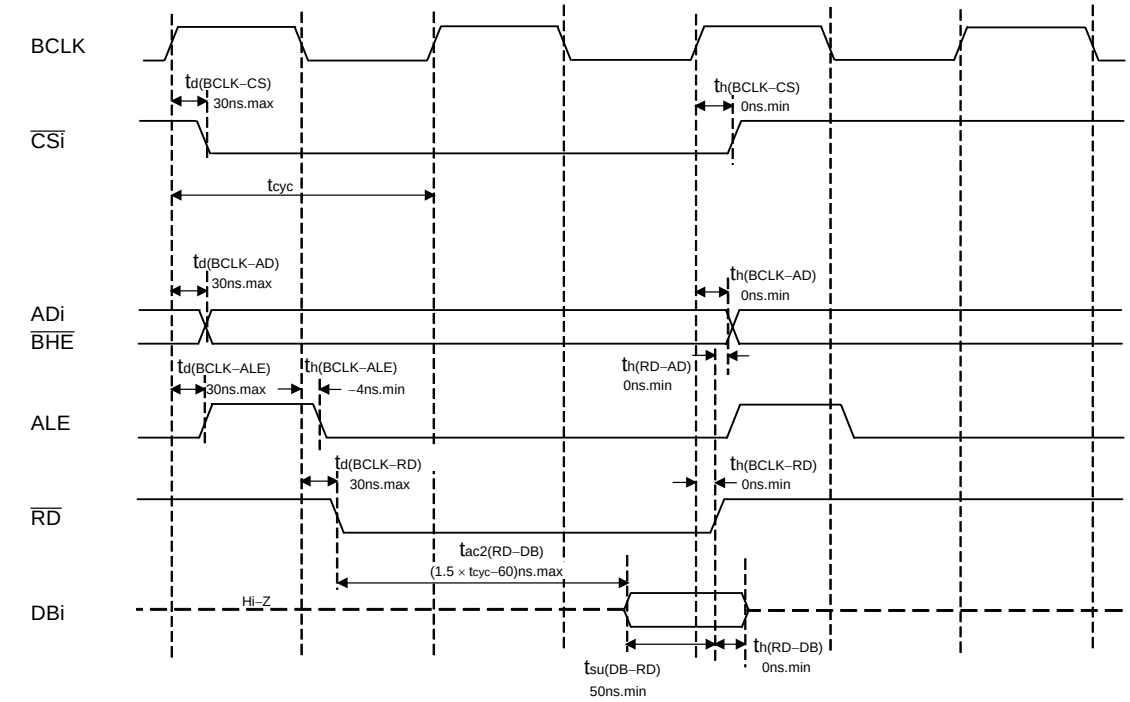
Figure 5.11 Timing Diagram (3)

Memory Expansion Mode, Microprocessor Mode

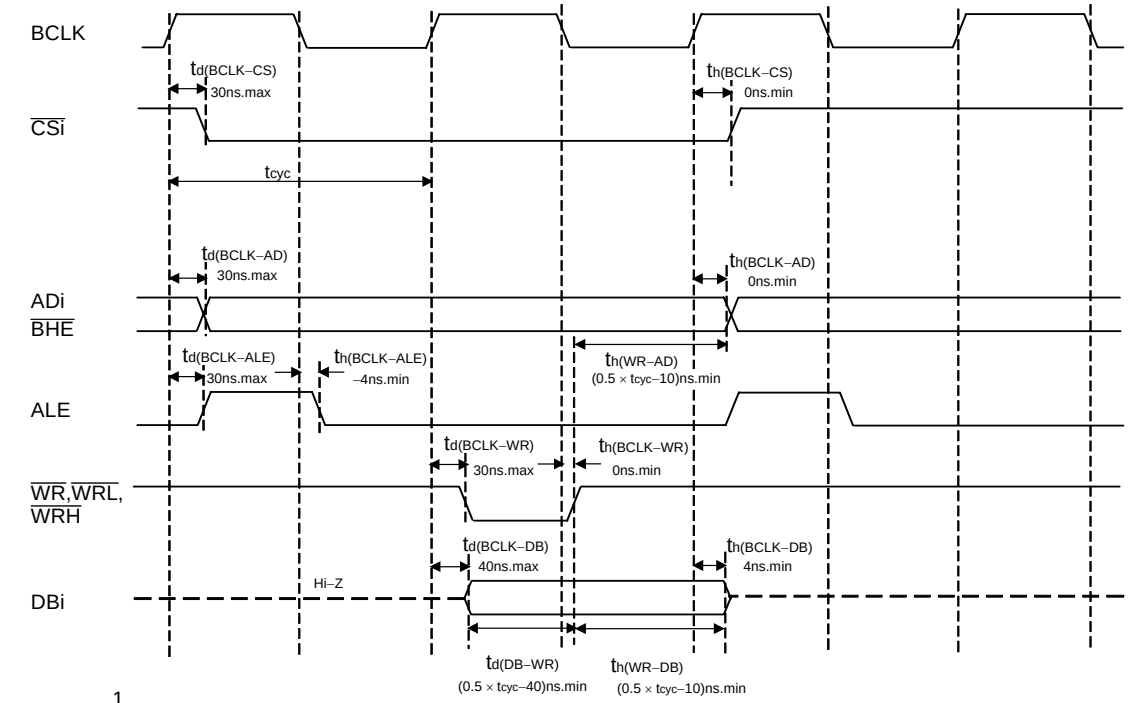
(for 1-wait setting and external area access)

$V_{CC1}=V_{CC2}=3V$

Read timing



Write timing



$$t_{cyc}=\frac{1}{f(BCLK)}$$

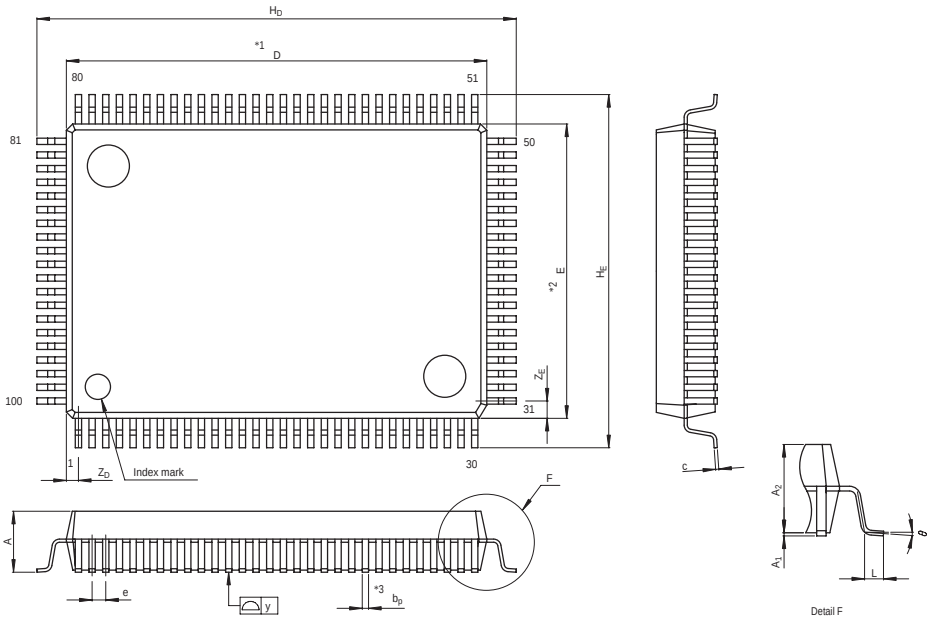
Measuring conditions
- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

Figure 5.13 Timing Diagram (5)

Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the "Packages" section of the Renesas Technology website.

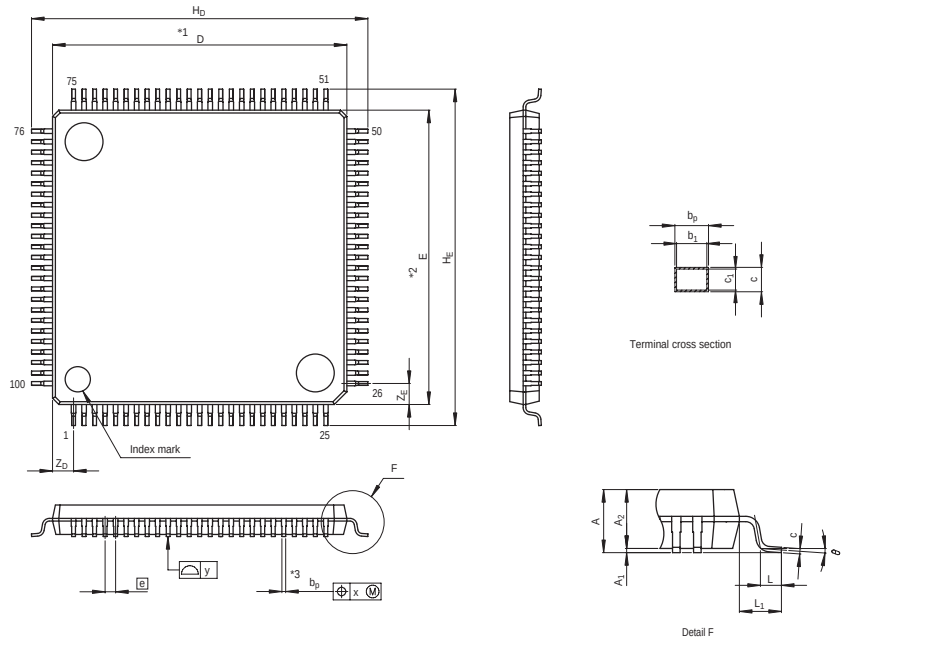
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x20-0.65	PRQP0100JB-A	100P6S-A	1.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	0.5	0.65	0.8
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.825	—
L	0.4	0.6	0.8

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

REVISION HISTORY	M16C/30P Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.70	Aug 26, 2004	–	First Edition issued
0.80	Mar 18, 2005	–	development support tools -> development tools
		–	BCLK -> CPU clock
		2	Table 1.1 Performance Outline of M16C/30P Group Serial interface is revised.
		4	Figure 1.2 Type., Memory Size, and Package is partly revised.
		8	Table 1.4 Pin Detection (2) is partly revised.
		20	Note 2 Table 5.3 A/D Conversion Characteristics is partly revised.
		21	Symbol of Table 5.4 Power Supply Circuit Timing Characteristics is partly revised.
		22	Table 5.5 Electrical Characteristics is revised.
		28	Table 5.19 Electrical Characteristics is revised.
1.00	Sep 01, 2005	2	Table 1.1 Performance Outline of M16C/30P Group is partly revised.
		4	Table 1.2 Product List is partly revised.
			Figure 1.2 Type No., Memory Size, and Package is partly revised.
		5	Figure 1.3 Pin Configuration is partly revised.
		6	Figure 1.4 Pin Configuration is partly revised.
		7-8	Tables 1.3 to 1.4 Pin Characteristics are added.
		9	Table 1.5 Pin Description is revised.
		14	3. Memory is partly revised.
		15	Table 4.1 SFR Information is partly revised.
		19	Table 4.5 SFR Information is partly revised
		21	Table 5.2 Recommended Operating Conditions is partly revised.
		22	Table 5.3 A/D Conversion Characteristics is partly revised.
		25	Note 1 is added in Table 5.6 External Clock Input (XIN input)
			Table 5.7 Memory Expansion Mode and Microprocessor Mode is added.
		28	Table 5.20 Memory Expansion Mode and Microprocessor Modes (for setting with no wait) is added.
			Figure 5.2 Ports P0 to P10 Measurement Circuit is added.
		29	Table 5.21 Memory Expansion Mode and Microprocessor Modes (for 1- to 3-wait setting and external area access) is added.
		32	Figure 5.5 Timing Diagram (3) is added.
		33	Figure 5.6 Timing Diagram (4) is added.
		34	Figure 5.7 Timing Diagram (5) is added.
		36	Note 1 to 4 are added in Table 5.23 External Clock Input (XIN input)
			Table 5.24 Memory Expansion Mode and Microprocessor Mode is added.
		39	Table 5.37 Memory Expansion Mode and Microprocessor Modes (for setting with no wait) is added.
			Figure 5.8 Ports P0 to P10 Measurement Circuit is added.
		40	Table 5.38 Memory Expansion Mode and Microprocessor Modes (for 1- to 3-wait setting and external area access) is added.
		43	Figure 5.11 Timing Diagram (3) is added.

Rev.	Date	Description	
		Page	Summary
		44	Figure 5.12 Timing Diagram (4) is added.
		45	Figure 5.13 Timing Diagram (5) is added.
1.10	Oct 01, 2005	2	Table 1.1 Performance Outline of M16C/30P Group is partly revised.
		4	Table 1.2 Product List is partly revised.
			Figure 1.2 Type No., Memory Size, and Package is partly revised.
		5	Table 1.3 Product Code of Mask ROM version Version for M16C/30P is added.
			Figure 1.3 Marking Diagram of Mask ROM Version for M16C/30P is added.
		6	Figure 1.4 Marking Diagram of ROM -less Version for M16C/30P is added.
		6	Table 1.4 Product Code of ROM-less version for M16C/30P is added.
		16	Figure 3.1 Memory Map is partly added.
		23	Table 5.2 information is revised.
1.11	May 31, 2006	4	1.4 Product List information is revised.
			Table 1.2 Product List is partly revised.
		5	Figure 1.2 Type No., Memory Size, and Package is partly added.
		7	Table 1.4 Product Code of Flash Memory version and ROM-less version for M16C/30P is partly revised.
			Figure 1.4 Marking Diagram of Flash Memory version and ROM-less Version for M16C/30P (Top View) is partly added.
		17	3. Memory information is revised.
			Figure 3.1 Memory Map is partly revised.
		18	Table 4.1 SFR Information(1) is partly revised.
		19	Table 4.2 SFR Information(2) is partly added.
		23	Table 5.1 Absolute Maximum Ratings information is revised.
		26	Table 5.4 Flash Memory Version Electrical Characteristics is added.
			Table 5.5 Flash Memory Version Program / Erase Voltage and Read Operation Voltage Characteristics is added.
		28	Table 5.7 Electrical Characteristics(1) is partly deleted.
		29	Table 5.8 Electrical Characteristics (2) is partly revised.
		33	Table 5.23 Memory Expansion and Microprocessor Modes NOTES 3 is partly revised.
		34	Table 5.24 Memory Expansion and Microprocessor Modes NOTES 3 is partly revised.
		40	Table 5.25 Electrical Characteristics (1) is partly deleted.
		41	Table 5.26 Electrical Characteristics (2) is partly revised.
		45	Table 5.41 Memory Expansion and Microprocessor Modes NOTES 3 is partly revised.
		46	Table 5.42 Memory Expansion and Microprocessor Modes NOTES 3 is partly revised.

REVISION HISTORY	M16C/30P Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.20	Oct 17, 2006	1	Note is partly deleted.
		2	Table 1.1 Performance Outline of M16C/30P Group is partly added.
		4	Table 1.2 Product List is partly revised.
		5	Figure 1.2 Type No., Memory Size, and Package is added.
		7	Table 1.4 Product Code of One Time Flash version, Flash Memory version, and ROM-less version for M16C/30P is partly added.
		17	Figure 3.1 Memory Map is partly added.
		19	Table 4.2 SFR Information (2) is partly added.
		23	Table 5.1 Absolute Maximum Ratings is partly added.
		27	Table 5.6 One Time Flash Version Electrical Characteristics and Table 5.7 One Time Flash Version Program Voltage and Read Operation Voltage Characteristics is added.
		30	Table 5.10 Electrical Characteristics (2) is partly added.
		42	Table 5.28 Electrical Characteristics (2) is partly added.
1.21	Nov 02 2006	7	Table 1.4 Product Code of One Time Flash version, Flash Memory version, and ROM-less version for M16C/30P is partly revised.
1.22	Mar 30, 2007	4	Table 1.2 Product List (1) is partly revised.
		5	Table 1.3 Product List (2) is partly revised.
		19	Table 4.2 SFR Information (2) is partly revised.