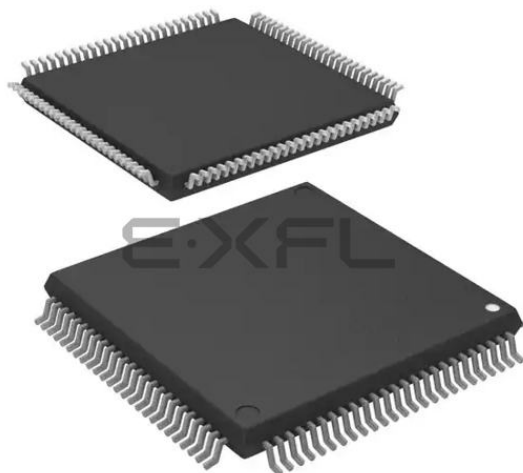




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Details

Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	16MHz
Connectivity	I ² C, IEBus, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 18x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30302sppg-u5

1.3 Block Diagram

Figure 1.1 is a M16C/30P Group Block Diagram.

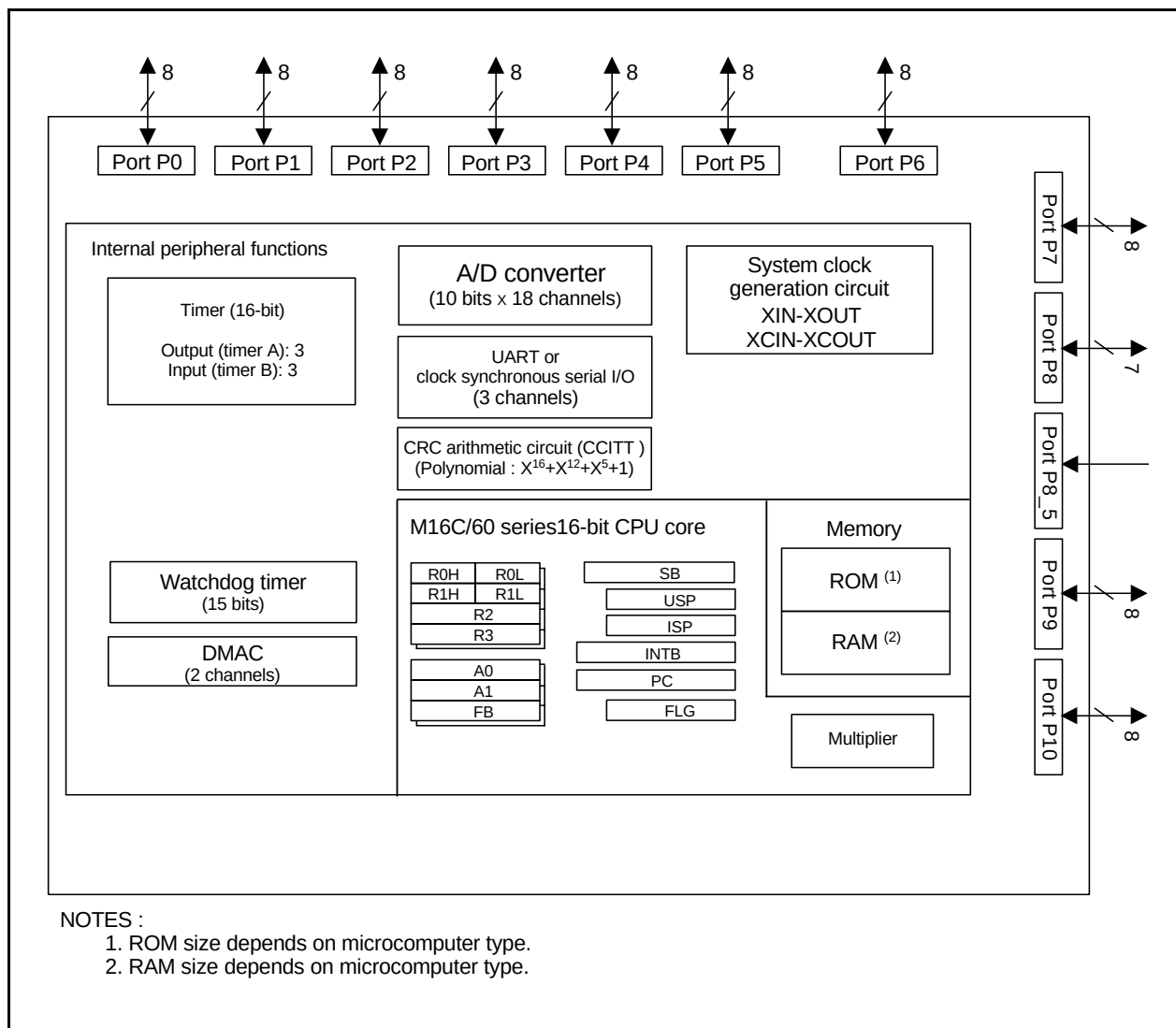


Figure 1.1 M16C/30P Group Block Diagram

Table 1.3 Product List (2)**As of March 2007**

Part No.	ROM Capacity	RAM Capacity	package code ⁽¹⁾	Remarks
M30302FAPFP	96 K + 4 Kbytes	5 Kbytes	PRQP0100JB-A	Flash memory version ⁽²⁾
M30302FAPGP			PLQP0100KB-A	
M30302FCPFP	128 K + 4 Kbytes		PRQP0100JB-A	
M30302FCPGP			PLQP0100KB-A	
M30302FEPFP	192 K + 4 Kbytes	6 Kbytes	PRQP0100JB-A	
M30302FEPGP			PLQP0100KB-A	
M30302SPFP	-	6 Kbytes	PRQP0100JB-A	ROM-less version
M30302SPGP			PLQP0100KB-A	

(D): Under development

(P): Under planning

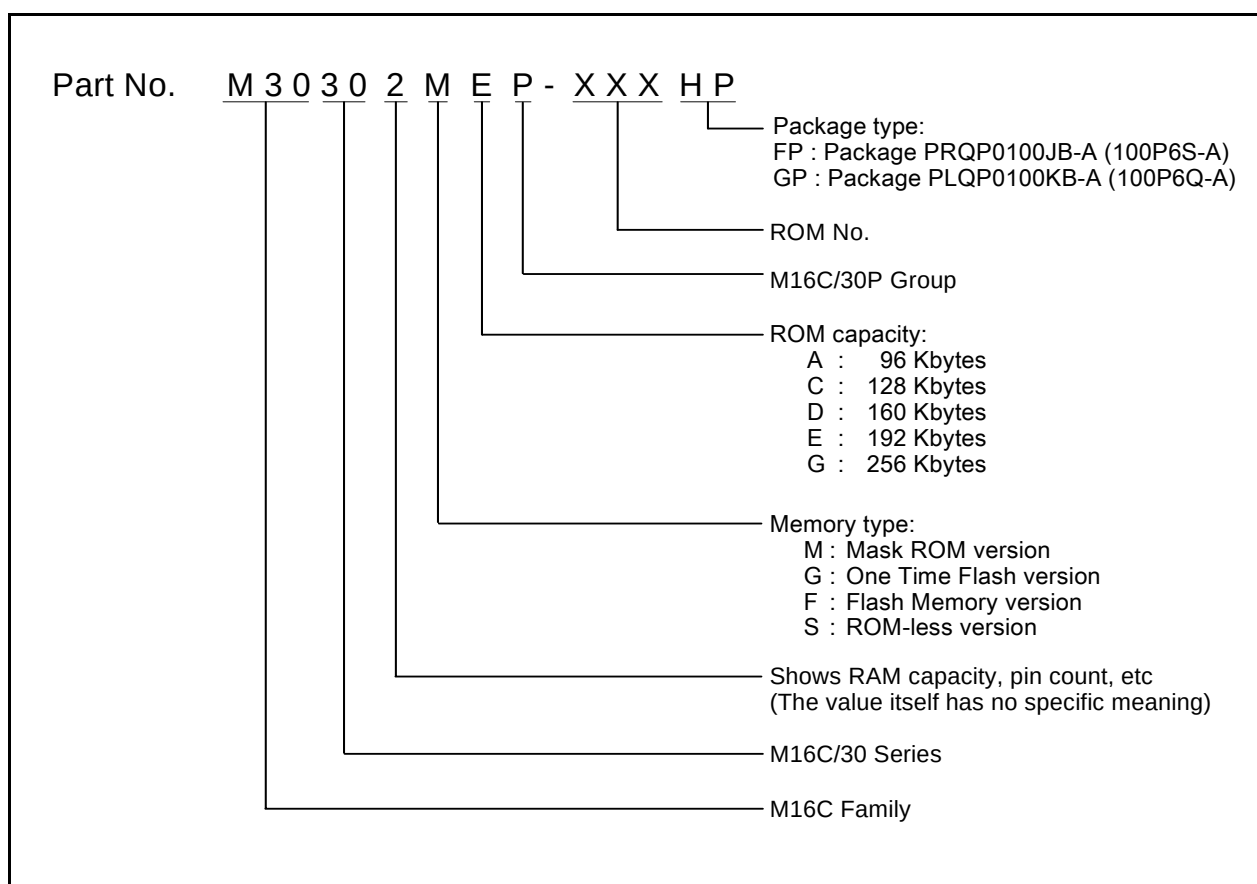
NOTES:

1. Previous package codes are as follows.

PRQP0100JB-A : 100P6S-A,

PLQP0100KB-A : 100P6Q-A

2. Block A (4-Kbytes space) is available in flash memory version.

**Figure 1.2 Part No., Memory Size, and Package**

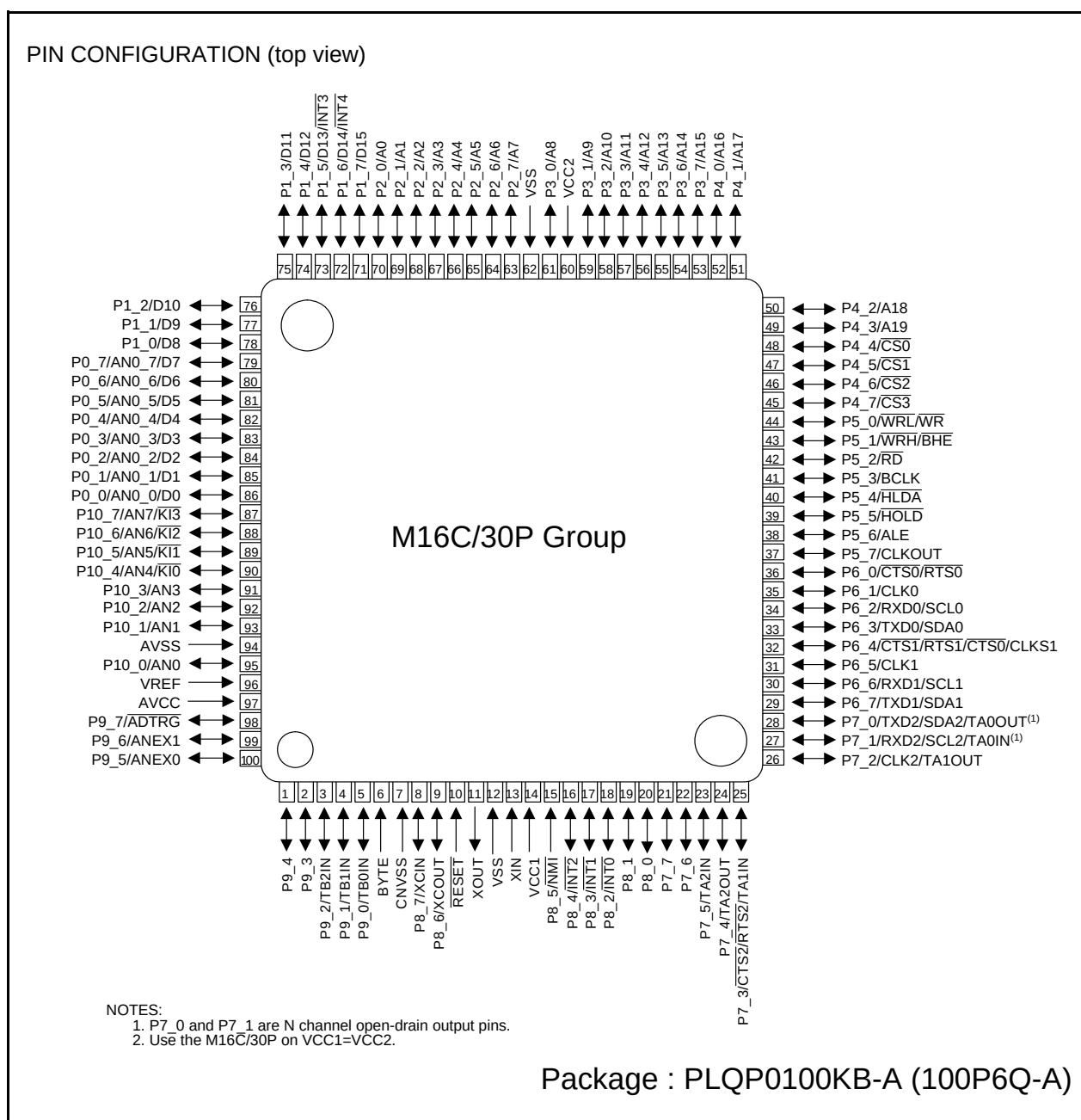


Figure 1.6 Pin Configuration (Top View)

Table 1.6 Pin Characteristics (1)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
FP	GP							
1	99		P9_6				ANEX1	
2	100		P9_5				ANEX0	
3	1		P9_4					
4	2		P9_3					
5	3		P9_2		TB2IN			
6	4		P9_1		TB1IN			
7	5		P9_0		TB0IN			
8	6	BYTE						
9	7	CNVSS						
10	8	XCIN	P8_7					
11	9	XCOUT	P8_6					
12	10	RESET						
13	11	XOUT						
14	12	VSS						
15	13	XIN						
16	14	VCC1						
17	15		P8_5	NMI				
18	16		P8_4	INT2				
19	17		P8_3	INT1				
20	18		P8_2	INT0				
21	19		P8_1					
22	20		P8_0					
23	21		P7_7					
24	22		P7_6					
25	23		P7_5		TA2IN			
26	24		P7_4		TA2OUT			
27	25		P7_3		TA1IN	CTS2/RTS2		
28	26		P7_2		TA1OUT	CLK2		
29	27		P7_1		TA0IN	RXD2/SCL2		
30	28		P7_0		TA0OUT	TXD2/SDA2		
31	29		P6_7			TXD1/SDA1		
32	30		P6_6			RXD1/SCL1		
33	31		P6_5			CLK1		
34	32		P6_4			CTS1/RTS1/CTS0/CLKS1		
35	33		P6_3			TXD0/SDA0		
36	34		P6_2			RXD0/SCL0		
37	35		P6_1			CLK0		
38	36		P6_0			CTS0/RTS0		
39	37		P5_7					RDY/CLKOUT
40	38		P5_6					ALE
41	39		P5_5					HOLD
42	40		P5_4					HLDA
43	41		P5_3					BCLK
44	42		P5_2					RD
45	43		P5_1					WRH/BHE
46	44		P5_0					WRL/WR
47	45		P4_7					CS3
48	46		P4_6					CS2
49	47		P4_5					CS1
50	48		P4_4					CS0

Table 1.7 Pin Characteristics (2)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
FP	GP							
51	49		P4_3					A19
52	50		P4_2					A18
53	51		P4_1					A17
54	52		P4_0					A16
55	53		P3_7					A15
56	54		P3_6					A14
57	55		P3_5					A13
58	56		P3_4					A12
59	57		P3_3					A11
60	58		P3_2					A10
61	59		P3_1					A9
62	60	VCC2						
63	61		P3_0					A8
64	62	VSS						
65	63		P2_7					A7
66	64		P2_6					A6
67	65		P2_5					A5
68	66		P2_4					A4
69	67		P2_3					A3
70	68		P2_2					A2
71	69		P2_1					A1
72	70		P2_0					A0
73	71		P1_7					D15
74	72		P1_6	INT4				D14
75	73		P1_5	INT3				D13
76	74		P1_4					D12
77	75		P1_3					D11
78	76		P1_2					D10
79	77		P1_1					D9
80	78		P1_0					D8
81	79		P0_7				AN0_7	D7
82	80		P0_6				AN0_6	D6
83	81		P0_5				AN0_5	D5
84	82		P0_4				AN0_4	D4
85	83		P0_3				AN0_3	D3
86	84		P0_2				AN0_2	D2
87	85		P0_1				AN0_1	D1
88	86		P0_0				AN0_0	D0
89	87		P10_7	KI3			AN7	
90	88		P10_6	KI2			AN6	
91	89		P10_5	KI1			AN5	
92	90		P10_4	KI0			AN4	
93	91		P10_3				AN3	
94	92		P10_2				AN2	
95	93		P10_1				AN1	
96	94	AVSS						
97	95		P10_0				AN0	
98	96	VREF						
99	97	AVCC						
100	98		P9_7				ADTRG	

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

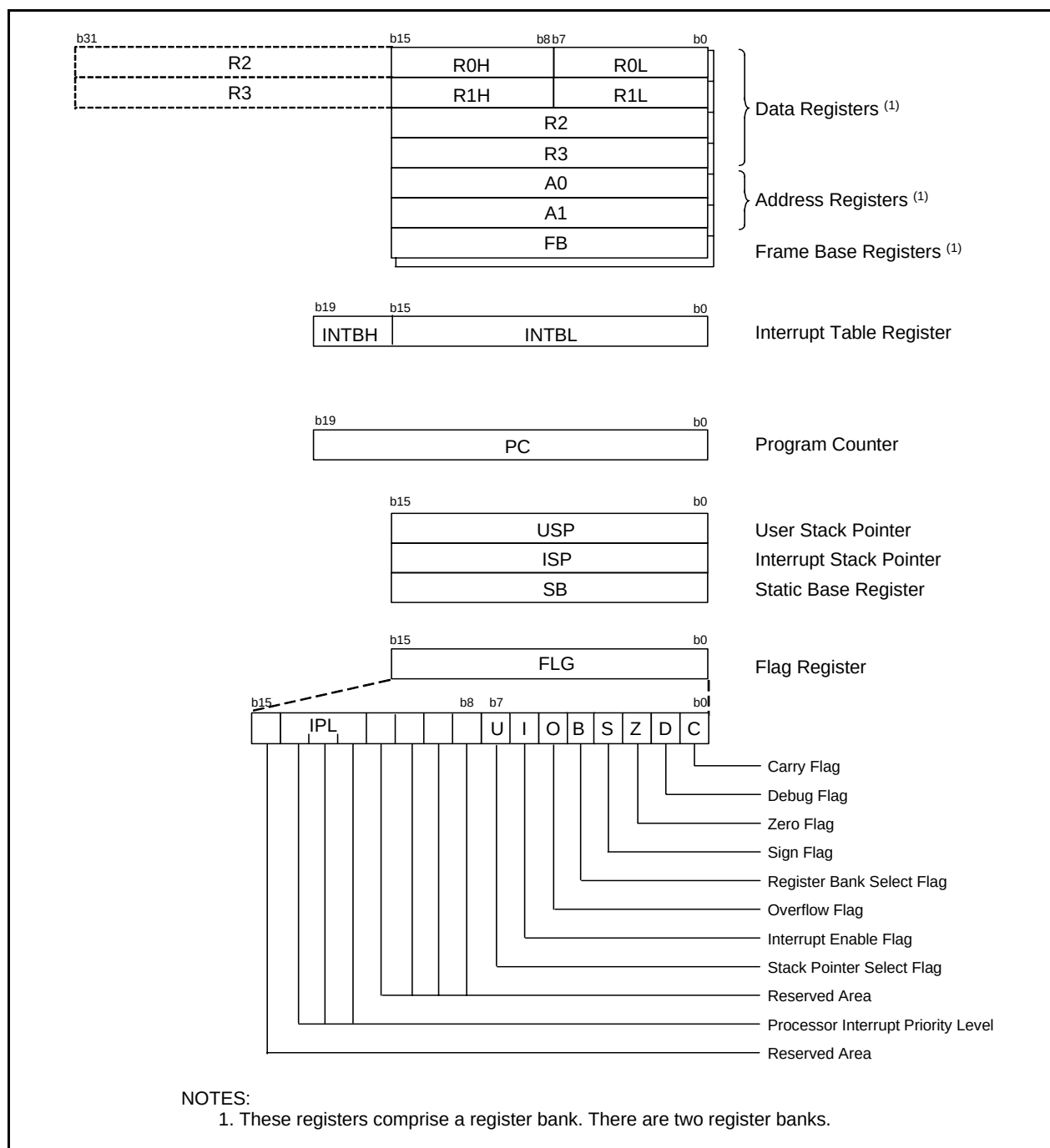


Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers.

R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

Table 4.3 SFR Information (3) ⁽¹⁾

Address	Register	Symbol	After Reset
0340h			
0341h			
0342h			
0343h			
0344h			
0345h			
0346h			
0347h			
0348h			
0349h			
034Ah			
034Bh			
034Ch			
034Dh			
034Eh			
034Fh			
0350h			
0351h			
0352h			
0353h			
0354h			
0355h			
0356h			
0357h			
0358h			
0359h			
035Ah			
035Bh			
035Ch			
035Dh			
035Eh	Interrupt Factor Select Register 2	IFSR2A	00XXXXXXb
035Fh	Interrupt Factor Select Register	IFSR	00h
0360h			
0361h			
0362h			
0363h			
0364h			
0365h			
0366h			
0367h			
0368h			
0369h			
036Ah			
036Bh			
036Ch	UART0 Special Mode Register 4	U0SMR4	00h
036Dh	UART0 Special Mode Register 3	U0SMR3	000X0X0Xb
036Eh	UART0 Special Mode Register 2	U0SMR2	X0000000b
036Fh	UART0 Special Mode Register	U0SMR	X0000000b
0370h	UART1 Special Mode Register 4	U1SMR4	00h
0371h	UART1 Special Mode Register 3	U1SMR3	000X0X0Xb
0372h	UART1 Special Mode Register 2	U1SMR2	X0000000b
0373h	UART1 Special Mode Register	U1SMR	X0000000b
0374h	UART2 Special Mode Register 4	U2SMR4	00h
0375h	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
0376h	UART2 Special Mode Register 2	U2SMR2	X0000000b
0377h	UART2 Special Mode Register	U2SMR	X0000000b
0378h	UART2 Transmit/Receive Mode Register	U2MR	00h
0379h	UART2 Bit Rate Generator	U2BRG	XXh
037Ah	UART2 Transmit Buffer Register	U2TB	XXh
037Bh			XXh
037Ch	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
037Dh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
037Eh	UART2 Receive Buffer Register	U2RB	XXh
037Fh			XXh

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Table 5.6 One Time Flash Version Electrical Characteristics ⁽¹⁾

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
—	Program Endurance			1	cycle
—	Word Program Time (V _{CC1} =5.0V)		50	500	μs
t _{PS}	One Time Flash Memory Circuit Stabilization Wait Time			15	μs
—	Data Hold Time ⁽⁴⁾	10			year

NOTES:

1. Referenced to V_{CC1}=4.5 to 5.5V, 3.0 to 3.6V at T_{opr} = 0 to 60 °C (U3, U5) unless otherwise specified.
2. T_{opr} = -40 to 85 °C (U3) / -20 to 85 °C (U5).

Table 5.7 One Time Flash Version Program Voltage and Read Operation Voltage Characteristics

Flash Program Voltage	Flash Read Operation Voltage
V _{CC1} = 3.3 ± 0.3 V or 5.0 ± 0.5 (T _{opr} = 0°C to 60°C)	V _{CC1} =2.7 to 5.5 V (T _{opr} = -40°C to 85°C (U3) -20°C to 85°C (U5))

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.11 External Clock Input (XIN input) ⁽¹⁾

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	62.5		ns
$t_{w(H)}$	External Clock Input HIGH Pulse Width	25		ns
$t_{w(L)}$	External Clock Input LOW Pulse Width	25		ns
t_r	External Clock Rise Time		15	ns
t_f	External Clock Fall Time		15	ns

NOTES:

1. The condition is $V_{CC1}=V_{CC2}=3.0$ to $5.0V$.

Table 5.12 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (for setting with no wait)		(NOTE 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (for setting with wait)		(NOTE 2)	ns
$t_{su(DB-RD)}$	Data Input Setup Time	40		ns
$t_{su(RDY-BCLK)}$	RDY Input Setup Time	30		ns
$t_{su(HOLD-BCLK)}$	HOLD Input Setup Time	40		ns
$t_h(RD-DB)$	Data Input Hold Time	0		ns
$t_h(BCLK-RDY)$	RDY Input Hold Time	0		ns
$t_h(BCLK-HOLD)$	HOLD Input Hold Time	0		ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 45[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(BCLK)} - 45[ns] \quad n \text{ is "2" for 1-wait setting.}$$

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.13 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiN Input Cycle Time	100		ns
$t_{w(TAH)}$	TAiN Input HIGH Pulse Width	40		ns
$t_{w(TAL)}$	TAiN Input LOW Pulse Width	40		ns

Table 5.14 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiN Input Cycle Time	400		ns
$t_{w(TAH)}$	TAiN Input HIGH Pulse Width	200		ns
$t_{w(TAL)}$	TAiN Input LOW Pulse Width	200		ns

Table 5.15 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiN Input Cycle Time	200		ns
$t_{w(TAH)}$	TAiN Input HIGH Pulse Width	100		ns
$t_{w(TAL)}$	TAiN Input LOW Pulse Width	100		ns

Table 5.16 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiN Input HIGH Pulse Width	100		ns
$t_{w(TAL)}$	TAiN Input LOW Pulse Width	100		ns

Table 5.17 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAiOUT Input HIGH Pulse Width	1000		ns
$t_{w(UPL)}$	TAiOUT Input LOW Pulse Width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

Table 5.18 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiN Input Cycle Time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT Input Setup Time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiN Input Setup Time	200		ns

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.19 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on both edges)	80		ns

Table 5.20 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	200		ns

Table 5.21 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	200		ns

Table 5.22 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input LOW Pulse Width	125		ns

Table 5.23 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input HIGH Pulse Width	100		ns
$t_{w(CKL)}$	CLKi Input LOW Pulse Width	100		ns
$t_{d(C-Q)}$	TXDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TXDi Hold Time	0		ns
$t_{su(D-C)}$	RXDi Input Setup Time	70		ns
$t_{h(C-D)}$	RXDi Input Hold Time	90		ns

Table 5.24 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input HIGH Pulse Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input LOW Pulse Width	250		ns

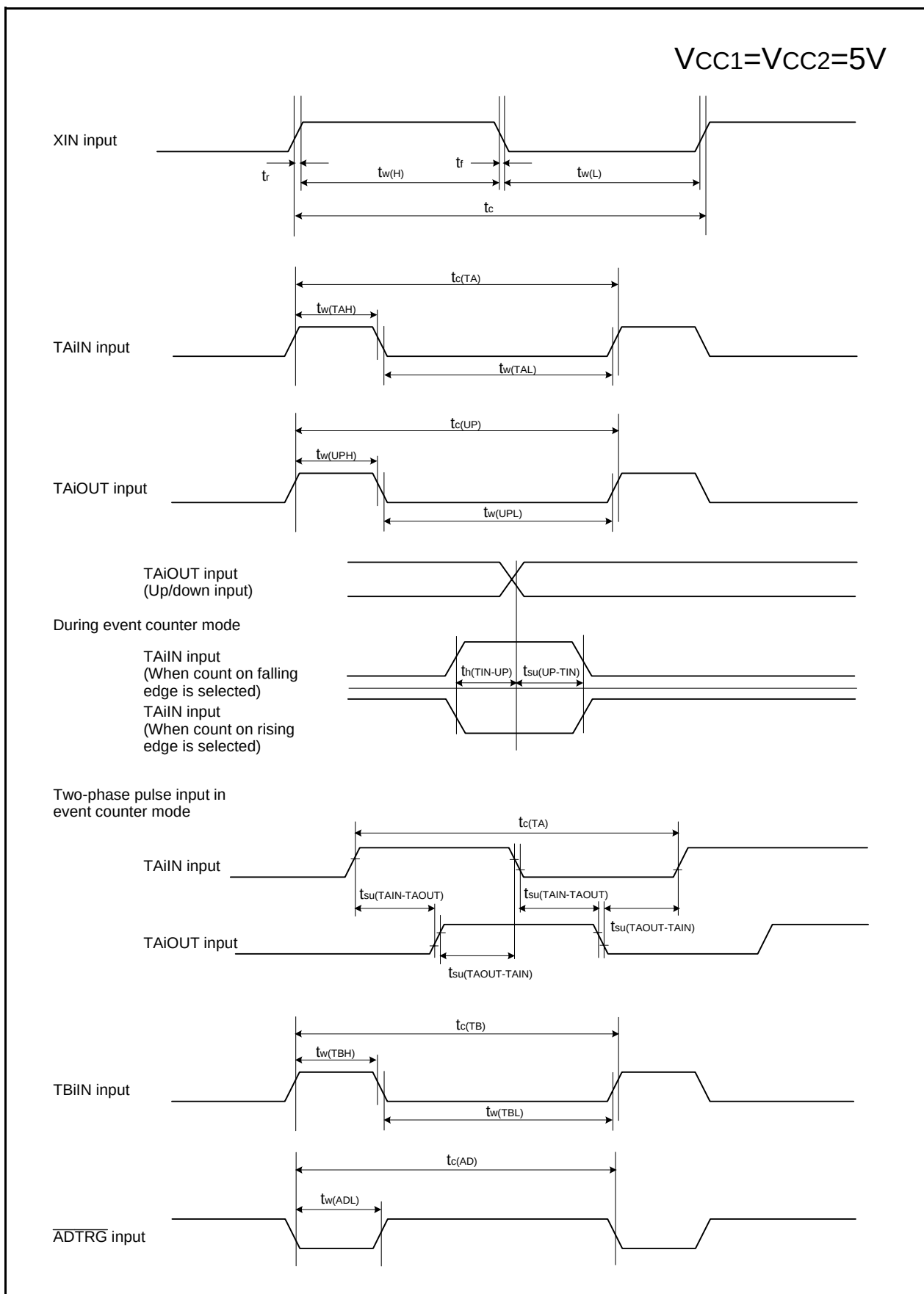
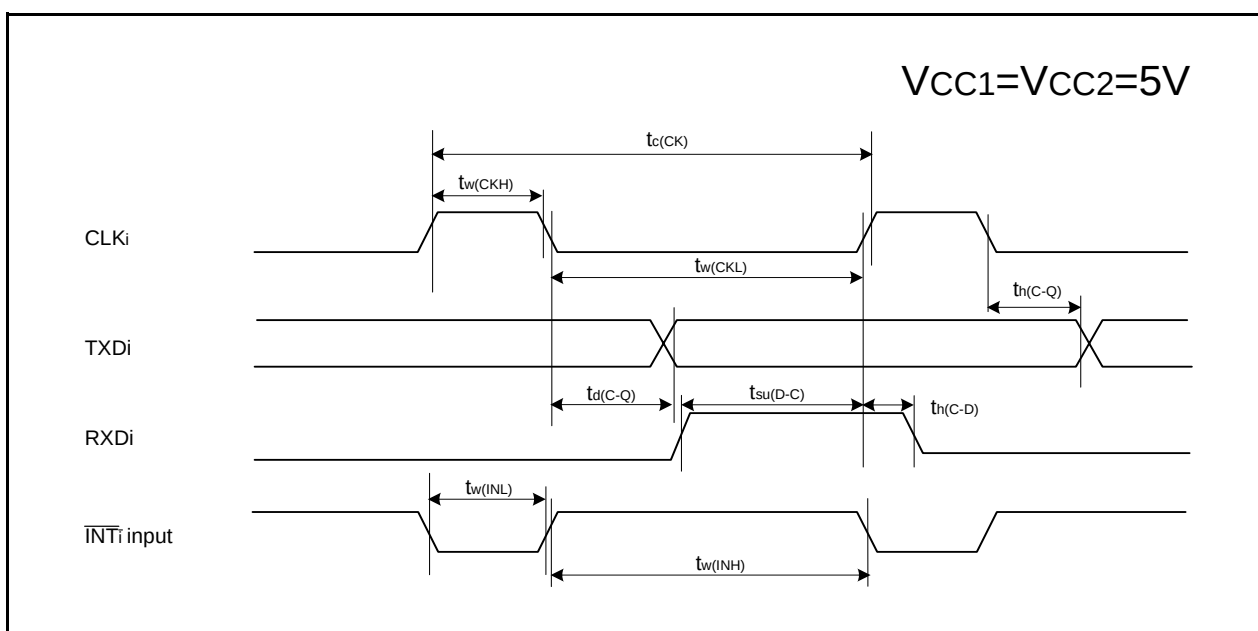


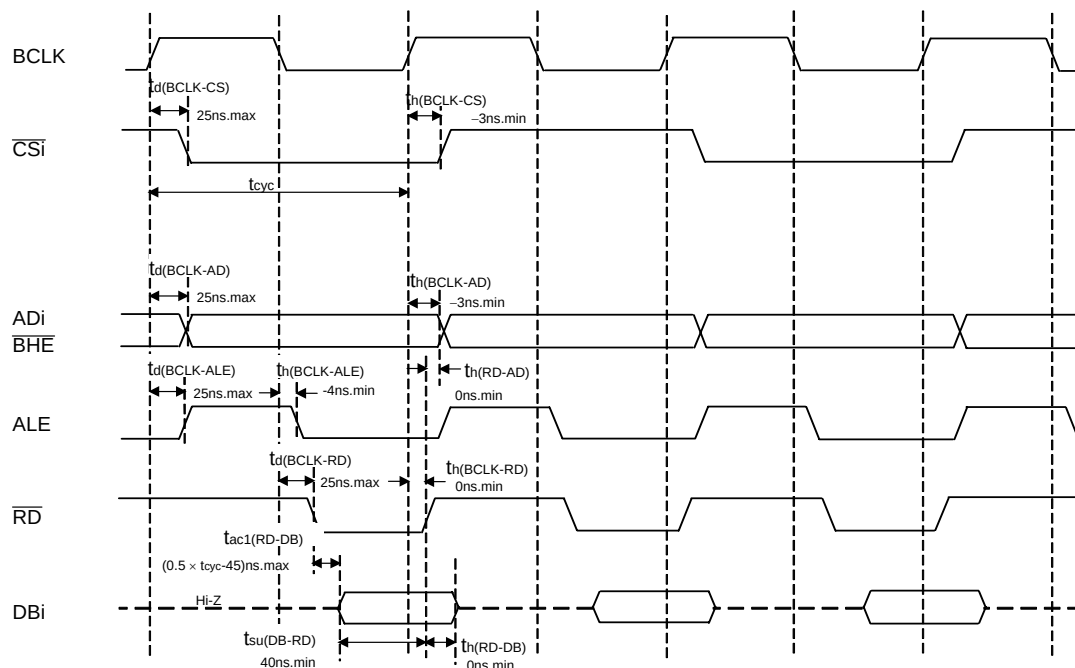
Figure 5.3 Timing Diagram (1)

**Figure 5.4 Timing Diagram (2)**

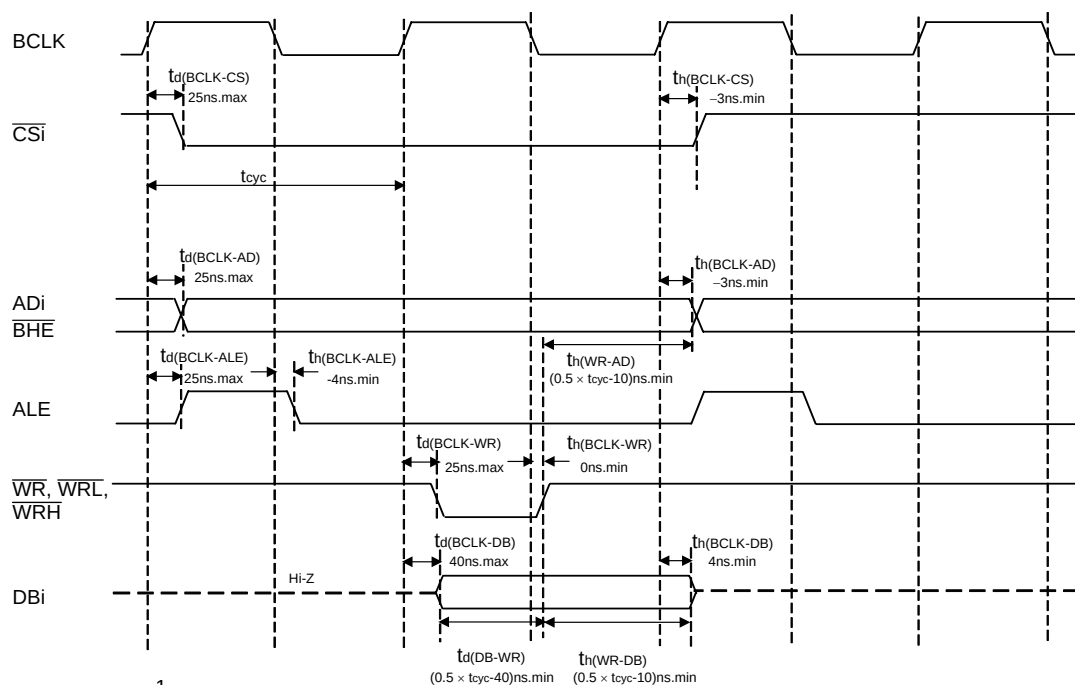
Memory Expansion Mode, Microprocessor Mode (For setting with no wait)

$V_{CC1}=V_{CC2}=5V$

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(\text{BCLK})}$$

Measuring conditions

- $V_{CC1}=V_{CC2}=5V$
- Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
- Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

Figure 5.6 Timing Diagram (4)

$$V_{CC1}=V_{CC2}=3V$$

Table 5.27 Electrical Characteristics (1) ⁽¹⁾

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	HIGH Output Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	I _{OH} =-1mA	V _{CC} -0.5		V _{CC}	V
V _{OH}	HIGH Output Voltage XOUT	HIGHPOWER	I _{OH} =-0.1mA	V _{CC} -0.5		V _{CC}	V
		LOWPOWER	I _{OH} =-50μA	V _{CC} -0.5		V _{CC}	V
	HIGH Output Voltage XCOUT	HIGHPOWER	With no load applied		2.5		V
		LOWPOWER	With no load applied		1.6		V
V _{OL}	LOW Output Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	I _{OL} =1mA			0.5	V
V _{OL}	LOW Output Voltage XOUT	HIGHPOWER	I _{OL} =0.1mA			0.5	V
		LOWPOWER	I _{OL} =50μA			0.5	V
	LOW Output Voltage XCOUT	HIGHPOWER	With no load applied		0		V
		LOWPOWER	With no load applied		0		V
V _{T+} -V _{T-}	Hysteresis	TA0IN to TA2IN, TB0IN to TB2IN, INT0 to INT4, NMI, ADTRG, CTS0 to CTS2, RXD0 to RXD2, CLK0 to CLK2, TA0OUT to TA2OUT, KI0 to KI3, SCL0 to SCL2, SDA0 to SDA2		0.2		0.8	V
V _{T+} -V _{T-}	Hysteresis	$\overline{\text{RESET}}$		0.2	(0.7)	1.8	V
I _{IH}	HIGH Input Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, $\overline{\text{RESET}}$, CNVSS, BYTE	V _I =3V			4.0	μA
I _{IL}	LOW Input Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, $\overline{\text{RESET}}$, CNVSS, BYTE	V _I =0V			-4.0	μA
R _{PULLUP}	Pull-Up Resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	V _I =0V	50	100	500	kΩ
R _{IXIN}	Feedback Resistance	XIN			3.0		MΩ
R _{IXCIN}	Feedback Resistance	XCIN			25		MΩ
V _{RAM}	RAM Retention Voltage		At stop mode	2.0			V

NOTES:

1. Referenced to V_{CC1} = V_{CC2} = 2.7 to 3.3V, V_{SS} = 0V at T_{opr} = -20 to 85°C / -40 to 85°C, f(XIN)=10MHz no wait unless otherwise specified.

$$V_{CC1}=V_{CC2}=3V$$

Timing Requirements

($V_{CC1} = V_{CC2} = 3V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.37 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on both edges)	120		ns

Table 5.38 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	600		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	300		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	300		ns

Table 5.39 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	600		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	300		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	300		ns

Table 5.40 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time	1500		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ Input LOW Pulse Width	200		ns

Table 5.41 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	300		ns
$t_{w(CKH)}$	CLKi Input HIGH Pulse Width	150		ns
$t_{w(CKL)}$	CLKi Input LOW Pulse Width	150		ns
$t_{d(C-Q)}$	TXDi Output Delay Time		160	ns
$t_{h(C-Q)}$	TXDi Hold Time	0		ns
$t_{su(D-C)}$	RXDi Input Setup Time	100		ns
$t_{h(C-D)}$	RXDi Input Hold Time	90		ns

Table 5.42 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input HIGH Pulse Width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ Input LOW Pulse Width	380		ns

$$V_{CC1}=V_{CC2}=3V$$

Switching Characteristics

($V_{CC1} = V_{CC2} = 3V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.44 Memory Expansion and Microprocessor Modes (for 1 wait setting and external area access)

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_d(BCLK-AD)$	Address Output Delay Time	See Figure 5.8		30	ns
$t_h(BCLK-AD)$	Address Output Hold Time (in relation to BCLK)		0		ns
$t_h(RD-AD)$	Address Output Hold Time (in relation to RD)		0		ns
$t_h(WR-AD)$	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
$t_d(BCLK-CS)$	Chip Select Output Delay Time			30	ns
$t_h(BCLK-CS)$	Chip Select Output Hold Time (in relation to BCLK)		0		ns
$t_d(BCLK-ALE)$	ALE Signal Output Delay Time			25	ns
$t_h(BCLK-ALE)$	ALE Signal Output Hold Time		-4		ns
$t_d(BCLK-RD)$	RD Signal Output Delay Time			30	ns
$t_h(BCLK-RD)$	RD Signal Output Hold Time		0		ns
$t_d(BCLK-WR)$	WR Signal Output Delay Time			30	ns
$t_h(BCLK-WR)$	WR Signal Output Hold Time		0		ns
$t_d(BCLK-DB)$	Data Output Delay Time (in relation to BCLK)			40	ns
$t_h(BCLK-DB)$	Data Output Hold Time (in relation to BCLK) ⁽³⁾		4		ns
$t_d(DB-WR)$	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
$t_h(WR-DB)$	Data Output Hold Time (in relation to WR) ⁽³⁾		(NOTE 2)		ns
$t_d(BCLK-HLDA)$	HLDA Output Delay Time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 40[ns] \quad n \text{ is "1" for 1-wait setting, } f(BCLK) \text{ is 12.5MHz or less.}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

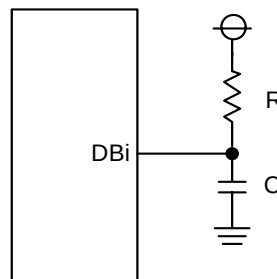
Hold time of data bus is expressed in

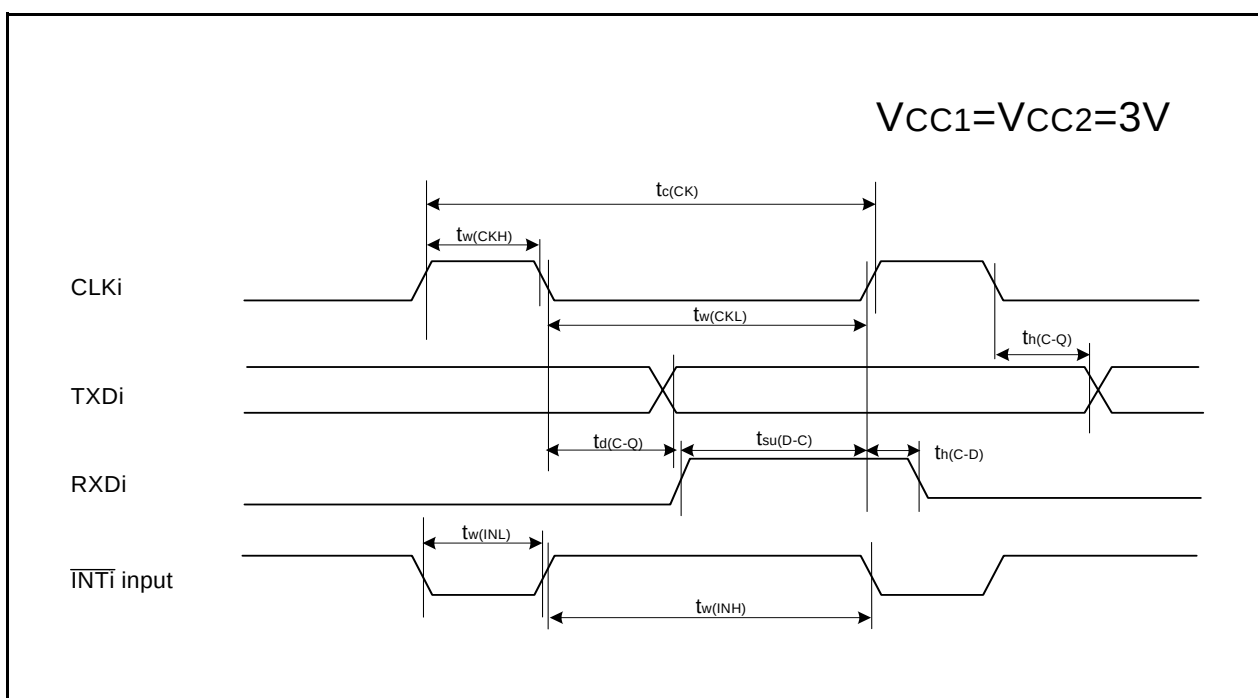
$$t = -CR \times \ln(1 - V_{OL} / V_{CC1})$$

by a circuit of the right figure.

For example, when $V_{OL} = 0.2V_{CC1}$, $C = 30pF$, $R = 1k\Omega$, hold time of output "L" level is

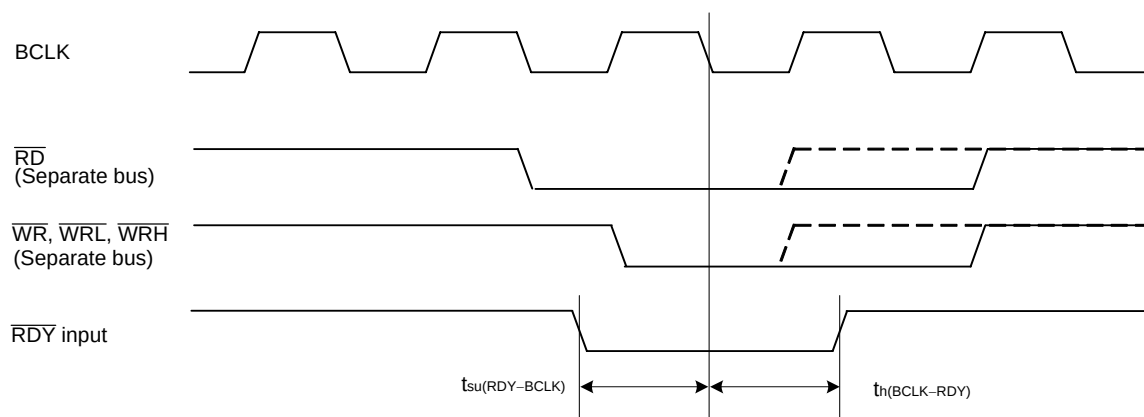
$$t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC1} / V_{CC1}) = 6.7ns.$$



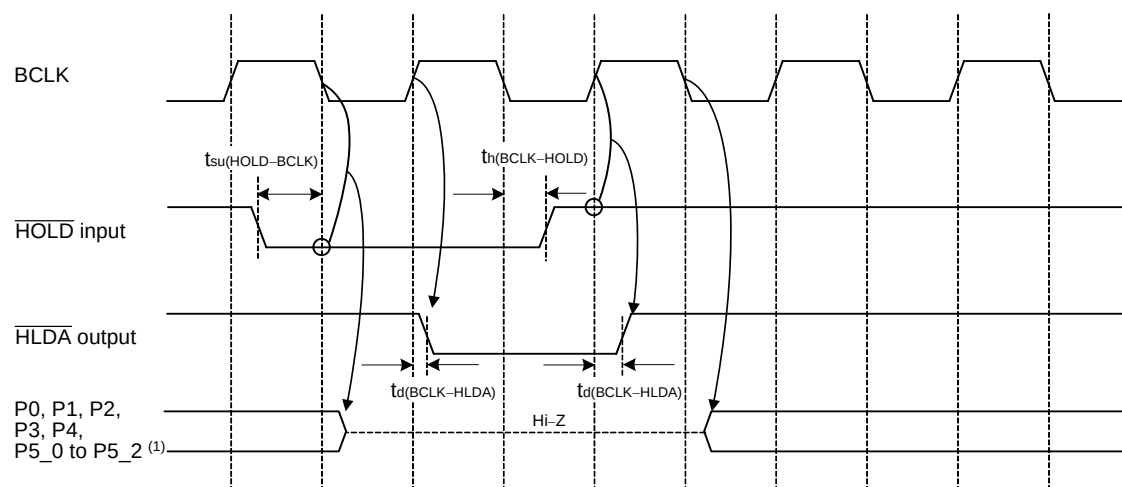
**Figure 5.10 Timing Diagram (2)**

Memory Expansion Mode, Microprocessor Mode $V_{CC1}=V_{CC2}=3V$

(Effective for setting with wait)



(Common to setting with wait and setting without wait)

**NOTES:**

1. These pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit in PM0 register.

Measuring conditions :

- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : Determined with $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : Determined with $V_{OL}=1.5V$, $V_{OH}=1.5V$

Figure 5.11 Timing Diagram (3)

REVISION HISTORY		M16C/30P Group Datasheet	
Rev.	Date	Description	
		Page	Summary
1.20	Oct 17, 2006	1	Note is partly deleted.
		2	Table 1.1 Performance Outline of M16C/30P Group is partly added.
		4	Table 1.2 Product List is partly revised.
		5	Figure 1.2 Type No., Memory Size, and Package is added.
		7	Table 1.4 Product Code of One Time Flash version, Flash Memory version, and ROM-less version for M16C/30P is partly added.
		17	Figure 3.1 Memory Map is partly added.
		19	Table 4.2 SFR Information (2) is partly added.
		23	Table 5.1 Absolute Maximum Ratings is partly added.
		27	Table 5.6 One Time Flash Version Electrical Characteristics and Table 5.7 One Time Flash Version Program Voltage and Read Operation Voltage Characteristics is added.
		30	Table 5.10 Electrical Characteristics (2) is partly added.
		42	Table 5.28 Electrical Characteristics (2) is partly added.
1.21	Nov 02 2006	7	Table 1.4 Product Code of One Time Flash version, Flash Memory version, and ROM-less version for M16C/30P is partly revised.
1.22	Mar 30, 2007	4	Table 1.2 Product List (1) is partly revised.
		5	Table 1.3 Product List (2) is partly revised.
		19	Table 4.2 SFR Information (2) is partly revised.