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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	20 MIPS
Connectivity	CANbus, I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Motor Control PWM, QEI, POR, PWM, WDT
Number of I/O	30
Program Memory Size	48KB (16K x 24)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic30f4011-20e-pt

The SA and SB bits are modified each time data passes through the adder/subtractor but can only be cleared by the user. When set, they indicate that the accumulator has overflowed its maximum range (bit 31 for 32-bit saturation or bit 39 for 40-bit saturation) and is saturated (if saturation is enabled). When saturation is not enabled, SA and SB default to bit 39 overflow and thus indicate that a catastrophic overflow has occurred. If the COVTE bit in the INTCON1 register is set, SA and SB bits generate an arithmetic warning trap when saturation is disabled.

The overflow and saturation Status bits can optionally be viewed in the STATUS register (SR) as the logical OR of OA and OB (in bit OAB) and the logical OR of SA and SB (in bit SAB). This allows programmers to check one bit in the STATUS register to determine if either accumulator has overflowed, or one bit to determine if either accumulator has saturated. This would be useful for complex number arithmetic which typically uses both the accumulators.

The device supports three Saturation and Overflow modes:

1. **Bit 39 Overflow and Saturation:**
When bit 39 overflow and saturation occurs, the saturation logic loads the maximally positive 9.31 (0x7FFFFFFF) or maximally negative 9.31 value (0x80000000) into the target accumulator. The SA or SB bit is set and remains set until cleared by the user. This is referred to as 'super saturation' and provides protection against erroneous data or unexpected algorithm problems (e.g., gain calculations).
2. **Bit 31 Overflow and Saturation:**
When bit 31 overflow and saturation occurs, the saturation logic then loads the maximally positive 1.31 value (0x007FFFFFFF) or maximally negative 1.31 value (0x00800000) into the target accumulator. The SA or SB bit is set and remains set until cleared by the user. When this Saturation mode is in effect, the guard bits are not used (so the OA, OB or OAB bits are never set).
3. **Bit 39 Catastrophic Overflow**
The bit 39 overflow Status bit from the adder is used to set the SA or SB bit, which remain set until cleared by the user. No saturation operation is performed and the accumulator is allowed to overflow (destroying its sign). If the COVTE bit in the INTCON1 register is set, a catastrophic overflow can initiate a trap exception.

2.4.2.2 Accumulator 'Write-Back'

The MAC class of instructions (with the exception of MPY, MPY.N, ED and EDAC) can optionally write a rounded version of the high word (bits 31 through 16) of the accumulator that is not targeted by the instruction into data space memory. The write is performed across the X bus into combined X and Y address space. The following addressing modes are supported:

1. **W13, Register Direct:**
The rounded contents of the non-target accumulator are written into W13 as a 1.15 fraction.
2. **[W13]+ = 2, Register Indirect with Post-Increment:**
The rounded contents of the non-target accumulator are written into the address pointed to by W13 as a 1.15 fraction. W13 is then incremented by 2 (for a word write).

2.4.2.3 Round Logic

The round logic is a combinational block, which performs a conventional (biased) or convergent (unbiased) round function during an accumulator write (store). The Round mode is determined by the state of the RND bit in the CORCON register. It generates a 16-bit, 1.15 data value which is passed to the data space write saturation logic. If rounding is not indicated by the instruction, a truncated 1.15 data value is stored and the least significant word is simply discarded.

Conventional rounding takes bit 15 of the accumulator, zero-extends it and adds it to the ACCxH word (bits 16 through 31 of the accumulator). If the ACCxL word (bits 0 through 15 of the accumulator) is between 0x8000 and 0xFFFF (0x8000 included), ACCxH is incremented. If ACCxL is between 0x0000 and 0x7FFF, ACCxH is left unchanged. A consequence of this algorithm is that over a succession of random rounding operations, the value tends to be biased slightly positive.

Convergent (or unbiased) rounding operates in the same manner as conventional rounding, except when ACCxL equals 0x8000. If this is the case, the LSb (bit 16 of the accumulator) of ACCxH is examined. If it is '1', ACCxH is incremented. If it is '0', ACCxH is not modified. Assuming that bit 16 is effectively random in nature, this scheme removes any rounding bias that may accumulate.

The SAC and SAC.R instructions store either a truncated (SAC) or rounded (SAC.R) version of the contents of the target accumulator to data memory, via the X bus (subject to data saturation, see **Section 2.4.2.4 "Data Space Write Saturation"**). Note that for the MAC class of instructions, the accumulator write-back operation functions in the same manner, addressing combined DSC (X and Y) data space through the X bus. For this class of instructions, the data is always subject to rounding.

3.0 MEMORY ORGANIZATION

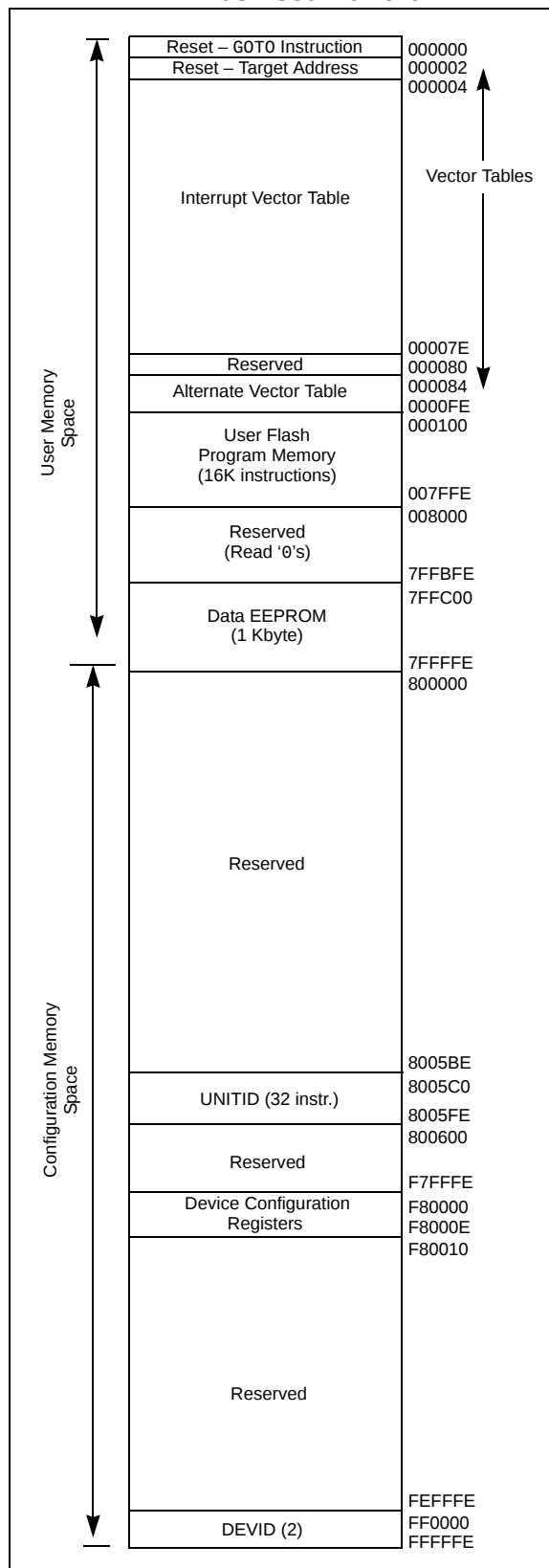
Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the “dsPIC30F Family Reference Manual” (DS70046). For more information on the device instruction set and programming, refer to the “16-bit MCU and DSC Reference Manual” (DS70157).

3.1 Program Address Space

The program address space is 4M instruction words. It is addressable by the 23-bit PC, table instruction Effective Address (EA) or data space EA, when program space is mapped into data space as defined by Table 3-1. Note that the program space address is incremented by two between successive program words in order to provide compatibility with data space addressing.

User program space access is restricted to the lower 4M instruction word address range (0x000000 to 0x7FFFFE) for all accesses other than TBLRD/TBLWT, which use TBLPAG<7> to determine user or configuration space access. In Table 3-1, read/write instructions, bit 23 allows access to the Device ID, the User ID and the Configuration bits; otherwise, bit 23 is always clear.

FIGURE 3-1: PROGRAM SPACE MEMORY MAP FOR dsPIC30F4011/4012



3.1.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

This architecture fetches 24-bit wide program memory. Consequently, instructions are always aligned. However, as the architecture is modified Harvard, data can also be present in program space.

There are two methods by which program space can be accessed; via special table instructions, or through the remapping of a 16K word program space page into the upper half of data space (see **Section 3.1.2 “Data Access From Program Memory Using Program Space Visibility”**). The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the least significant word (lsw) of any address within program space, without going through data space. The TBLRDH and TBLWTH instructions are the only method whereby the upper 8 bits of a program space word can be accessed as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two, 16-bit word-wide address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space which contains the least significant data word, and TBLRDH and TBLWTH access the space which contains the Most Significant Byte of data.

Figure 3-2 illustrates how the EA is created for table operations and data space accesses (PSV = 1). Here, P<23:0> refers to a program space word, whereas D<15:0> refers to a data space word.

A set of table instructions is provided to move byte or word-sized data to and from program space (see Figure 3-3 and Figure 3-4).

1. **TBLRDL** : Table Read Low
Word: Read the lsw of the program address; P<15:0> maps to D<15:0>.
Byte: Read one of the LSBs of the program address; P<7:0> maps to the destination byte when byte select = 0; P<15:8> maps to the destination byte when byte select = 1.
2. **TBLWTL** : Table Write Low (refer to **Section 6.0 “Flash Program Memory”** for details on Flash programming).
3. **TBLRDH** : Table Read High
Word: Read the msw of the program address; P<23:16> maps to D<7:0>; D<15:8> will always be = 0.
Byte: Read one of the MSBs of the program address; P<23:16> maps to the destination byte when byte select = 0; The destination byte will always be ‘0’ when byte select = 1.
4. **TBLWTH** : Table Write High (refer to **Section 6.0 “Flash Program Memory”** for details on Flash programming).

FIGURE 3-3: PROGRAM DATA TABLE ACCESS (LEAST SIGNIFICANT WORD)

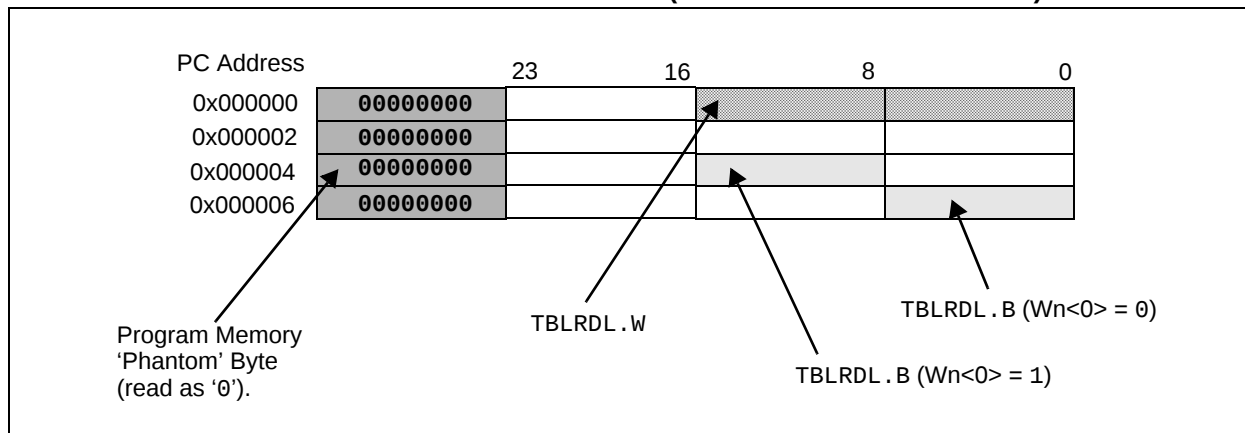
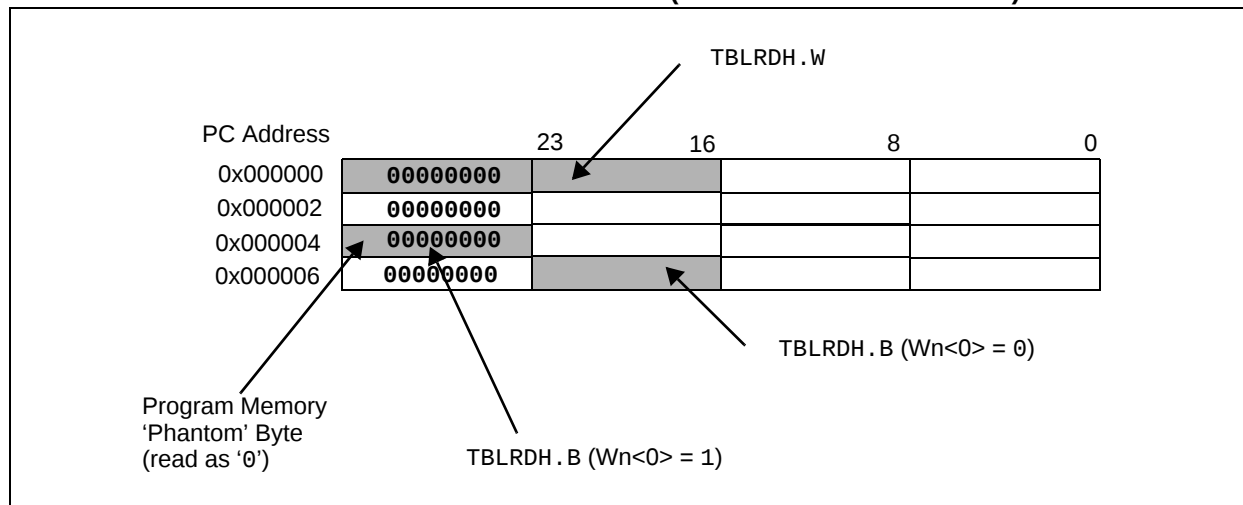


FIGURE 3-4: PROGRAM DATA TABLE ACCESS (MOST SIGNIFICANT BYTE)



3.1.2 DATA ACCESS FROM PROGRAM MEMORY USING PROGRAM SPACE VISIBILITY

The upper 32 Kbytes of data space may optionally be mapped into any 16K word program space page. This provides transparent access of stored constant data from X data space without the need to use special instructions (i.e., TBLRDL/H, TBLWTL/H instructions).

Program space access through the data space occurs if the MSb of the data space EA is set and program space visibility is enabled by setting the PSV bit in the Core Control register (CORCON). The functions of CORCON are discussed in **Section 2.4 “DSP Engine”**.

Data accesses to this area add an additional cycle to the instruction being executed, since two program memory fetches are required.

Note that the upper half of addressable data space is always part of the X data space. Therefore, when a DSP operation uses program space mapping to access this memory region, Y data space should typically contain state (variable) data for DSP operations, whereas X data space should typically contain coefficient (constant) data.

Although each data space address, 0x8000 and higher, maps directly into a corresponding program memory address (see Figure 3-5), only the lower 16 bits of the 24-bit program word are used to contain the data. The upper 8 bits should be programmed to force an illegal instruction to maintain machine robustness. For information on instruction encoding, refer to the *“16-bit MCU and DSC Programmer’s Reference Manual”* (DS70157).

Note that by incrementing the PC by 2 for each program memory word, the Least Significant 15 bits of data space addresses directly map to the Least Significant 15 bits in the corresponding program space addresses. The remaining bits are provided by the Program Space Visibility Page register, PSVPAG<7:0>, as shown in Figure 3-5.

Note: PSV access is temporarily disabled during table reads/writes.

For instructions that use PSV which are executed outside a REPEAT loop:

- The following instructions require one instruction cycle in addition to the specified execution time:
 - MAC class of instructions with data operand prefetch
 - MOV instructions
 - MOV.D instructions
- All other instructions require two instruction cycles in addition to the specified execution time of the instruction.

For instructions that use PSV which are executed inside a REPEAT loop:

- The following instances require two instruction cycles in addition to the specified execution time of the instruction:
 - Execution in the first iteration
 - Execution in the last iteration
 - Execution prior to exiting the loop due to an interrupt
 - Execution upon re-entering the loop after an interrupt is serviced
- Any other iteration of the REPEAT loop allows the instruction, accessing data using PSV, to execute in a single cycle.

4.2.3 MODULO ADDRESSING APPLICABILITY

Modulo Addressing can be applied to the Effective Address (EA) calculation associated with any W register. It is important to realize that the address boundaries check for addresses less than or greater than the upper (for incrementing buffers) and lower (for decrementing buffers) boundary addresses (not just equal to). Address changes may, therefore, jump beyond boundaries and still be adjusted correctly.

Note: The modulo corrected Effective Address is written back to the register only when Pre-Modify or Post-Modify Addressing mode is used to compute the Effective Address. When an address offset (e.g., [W7+W2]) is used, Modulo Addressing correction is performed, but the contents of the register remain unchanged.

4.3 Bit-Reversed Addressing

Bit-Reversed Addressing is intended to simplify data reordering for radix-2 FFT algorithms. It is supported by the X AGU for data writes only.

The modifier, which may be a constant value or register contents, is regarded as having its bit order reversed. The address source and destination are kept in normal order. Thus, the only operand requiring reversal is the modifier.

4.3.1 BIT-REVERSED ADDRESSING IMPLEMENTATION

Bit-Reversed Addressing is enabled when:

1. BWM (W register selection) in the MODCON register is any value other than 15 (the stack can not be accessed using Bit-Reversed Addressing) and
2. The BREN bit is set in the XBREV register and
3. The addressing mode used is Register Indirect with Pre-Increment or Post-Increment.

If the length of a bit-reversed buffer is $M = 2^N$ bytes, then the last 'N' bits of the data buffer start address must be zeros.

XB<14:0> is the Bit-Reversed Addressing modifier, or 'pivot point', which is typically a constant. In the case of an FFT computation, its value is equal to half of the FFT data buffer size.

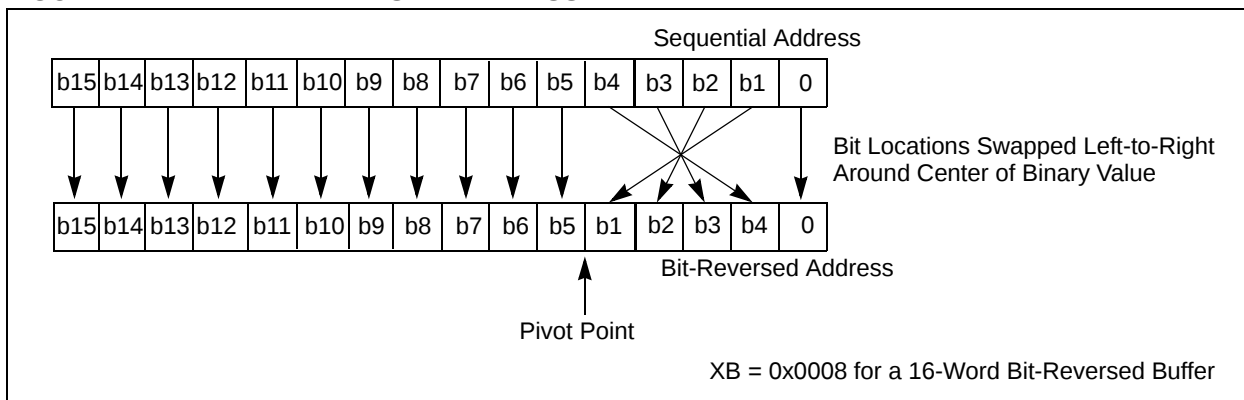
Note: All bit-reversed EA calculations assume word-sized data (LSb of every EA is always clear). The XB value is scaled accordingly to generate compatible (byte) addresses.

When enabled, Bit-Reversed Addressing is only executed for Register Indirect with Pre-Increment or Post-Increment Addressing mode and word-sized data writes. It will not function for any other addressing mode or for byte-sized data, and normal addresses will be generated instead. When Bit-Reversed Addressing is active, the W Address Pointer will always be added to the address modifier (XB) and the offset associated with the Register Indirect Addressing mode will be ignored. In addition, as word-sized data is a requirement, the LSb of the EA is ignored (and always clear).

Note: Modulo Addressing and Bit-Reversed Addressing should not be enabled together. In the event that the user attempts to do this, Bit-Reversed Addressing will assume priority when active for the X WAGU, and X WAGU Modulo Addressing will be disabled. However, Modulo Addressing will continue to function in the X RAGU.

If Bit-Reversed Addressing has already been enabled by setting the BREN bit (XBREV<15>), then a write to the XBREV register should not be immediately followed by an indirect read operation using the W register that has been designated as the Bit-Reversed Pointer.

FIGURE 4-2: BIT-REVERSED ADDRESS EXAMPLE



5.1 Interrupt Priority

The user-assignable Interrupt Priority (IP<2:0>) bits for each individual interrupt source are located in the Least Significant 3 bits of each nibble within the IPCx register(s). Bit 3 of each nibble is not used and is read as a '0'. These bits define the priority level assigned to a particular interrupt by the user.

Note: The user-assignable priority levels start at 0 as the lowest priority, and level 7 as the highest priority.

Since more than one interrupt request source may be assigned to a specific user-assigned priority level, a means is provided to assign priority within a given level. This method is called "Natural Order Priority".

Natural order priority is determined by the position of an interrupt in the vector table, and only affects interrupt operation when multiple interrupts with the same user-assigned priority become pending at the same time.

Table 5-1 lists the interrupt numbers and interrupt sources for the dsPIC DSCs and their associated vector numbers.

Note 1: The natural order priority scheme has 0 as the highest priority and 53 as the lowest priority.

2: The natural order priority number is the same as the INT number.

The ability for the user to assign every interrupt to one of seven priority levels implies that the user can assign a very high overall priority level to an interrupt with a low natural order priority. For example, the PLVD (Low-Voltage Detect) can be given a priority of 7. The INT0 (External Interrupt 0) may be assigned to priority level 1, thus giving it a very low effective priority.

TABLE 5-1: INTERRUPT VECTOR TABLE

INT Number	Vector Number	Interrupt Source
Highest Natural Order Priority		
0	8	INT0 – External Interrupt 0
1	9	IC1 – Input Capture 1
2	10	OC1 – Output Compare 1
3	11	T1 – Timer1
4	12	IC2 – Input Capture 2
5	13	OC2 – Output Compare 2
6	14	T2 – Timer2
7	15	T3 – Timer3
8	16	SPI1
9	17	U1RX – UART1 Receiver
10	18	U1TX – UART1 Transmitter
11	19	ADC – ADC Convert Done
12	20	NVM – NVM Write Complete
13	21	SI2C – I ² C™ Slave Interrupt
14	22	MI2C – I ² C Master Interrupt
15	23	Input Change Interrupt
16	24	INT1 – External Interrupt 1
17	25	IC7 – Input Capture 7
18	26	IC8 – Input Capture 8
19	27	OC3 – Output Compare 3
20	28	OC4 – Output Compare 4
21	29	T4 – Timer4
22	30	T5 – Timer5
23	31	INT2 – External Interrupt 2
24	32	U2RX – UART2 Receiver
25	33	U2TX – UART2 Transmitter
26	34	Reserved
27	35	C1 – Combined IRQ for CAN1
28	36	Reserved
29	37	Reserved
30	38	Reserved
31	39	Reserved
32	40	Reserved
33	41	Reserved
34	42	Reserved
35	43	Reserved
36	44	Reserved
37	45	Reserved
38	46	Reserved
39	47	PWM – PWM Period Match
40	48	QEI – QEI Interrupt
41	49	Reserved
42	50	Reserved
43	51	FLTA – PWM Fault A
44	52	Reserved
45-53	53-61	Reserved
Lowest Natural Order Priority		

9.0 TIMER1 MODULE

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the *dsPIC30F Family Reference Manual* (DS70046). For more information on the device instruction set and programming, refer to the *“16-bit MCU and DSC Reference Manual”* (DS70157).

This section describes the 16-bit general purpose Timer1 module and associated operational modes. Figure 9-1 depicts the simplified block diagram of the 16-bit Timer1 module.

Note: Timer1 is a 'Type A' timer. Please refer to the specifications for a Type A timer in **Section 24.0 “Electrical Characteristics”** of this document.

The following sections provide a detailed description, including setup and control registers, along with associated block diagrams for the operational modes of the timers.

The Timer1 module is a 16-bit timer which can serve as the time counter for the Real-Time Clock, or operate as a free-running, interval timer/counter. The 16-bit timer has the following modes:

- 16-bit Timer
- 16-bit Synchronous Counter
- 16-bit Asynchronous Counter

Further, the following operational characteristics are supported:

- Timer gate operation
- Selectable prescaler settings
- Timer operation during CPU Idle and Sleep modes
- Interrupt on 16-bit Period register match or falling edge of external gate signal

These operating modes are determined by setting the appropriate bit(s) in the 16-bit SFR, T1CON. Figure 9-1 presents a block diagram of the 16-bit timer module.

16-bit Timer Mode: In the 16-bit Timer mode, the timer increments on every instruction cycle up to a match value, preloaded into the Period register, PR1, then resets to 0 and continues to count.

When the CPU goes into the Idle mode, the timer will stop incrementing unless the TSIDL (T1CON<13>) bit = 0. If TSIDL = 1, the timer module logic will resume the incrementing sequence upon termination of the CPU Idle mode.

16-bit Synchronous Counter Mode: In the 16-bit Synchronous Counter mode, the timer increments on the rising edge of the applied external clock signal, which is synchronized with the internal phase clocks. The timer counts up to a match value preloaded in PR1, then resets to 0 and continues.

When the CPU goes into the Idle mode, the timer will stop incrementing unless the respective TSIDL bit = 0. If TSIDL = 1, the timer module logic will resume the incrementing sequence upon termination of the CPU Idle mode.

16-bit Asynchronous Counter Mode: In the 16-bit Asynchronous Counter mode, the timer increments on every rising edge of the applied external clock signal. The timer counts up to a match value preloaded in PR1, then resets to 0 and continues.

When the timer is configured for the Asynchronous mode of operation, and the CPU goes into the Idle mode, the timer will stop incrementing if TSIDL = 1.

TABLE 12-1: INPUT CAPTURE REGISTER MAP⁽¹⁾

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
IC1BUF	0140	Input 1 Capture Register																uuuu uuuu uuuu uuuu
IC1CON	0142	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>	ICOV	ICBNE	ICM<2:0>				0000 0000 0000 0000
IC2BUF	0144	Input 2 Capture Register																uuuu uuuu uuuu uuuu
IC2CON	0146	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>	ICOV	ICBNE	ICM<2:0>				0000 0000 0000 0000
IC7BUF	0158	Input 7 Capture Register																uuuu uuuu uuuu uuuu
IC7CON	015A	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>	ICOV	ICBNE	ICM<2:0>				0000 0000 0000 0000
IC8BUF	015C	Input 8 Capture Register																uuuu uuuu uuuu uuuu
IC8CON	015E	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>	ICOV	ICBNE	ICM<2:0>				0000 0000 0000 0000

Legend: u = uninitialized bit; — = unimplemented bit, read as '0'

Note 1: Refer to the "dsPIC30F Family Reference Manual" (DS70046) for descriptions of register bit fields.

14.3 Position Measurement Mode

There are two Measurement modes which are supported and are termed x2 and x4. These modes are selected by the QEIM<2:0> (QEICON<10:8>) mode select bits.

When control bits, QEIM<2:0> = 100 or 101, the x2 Measurement mode is selected and the QEI logic only looks at the Phase A input for the position counter increment rate. Every rising and falling edge of the Phase A signal causes the position counter to be incremented or decremented. The Phase B signal is still utilized for the determination of the counter direction just as in the x4 mode.

Within the x2 Measurement mode, there are two variations of how the position counter is reset:

1. Position counter reset by detection of index pulse, QEIM<2:0> = 100.
2. Position counter reset by match with MAXCNT, QEIM<2:0> = 101.

When control bits, QEIM<2:0> = 110 or 111, the x4 Measurement mode is selected and the QEI logic looks at both edges of the Phase A and Phase B input signals. Every edge of both signals causes the position counter to increment or decrement.

Within the x4 Measurement mode, there are two variations of how the position counter is reset:

1. Position counter reset by detection of index pulse, QEIM<2:0> = 110.
2. Position counter reset by match with MAXCNT, QEIM<2:0> = 111.

The x4 Measurement mode provides for finer resolution data (more position counts) for determining motor position.

14.4 Programmable Digital Noise Filters

The digital noise filter section is responsible for rejecting noise on the incoming quadrature signals. Schmitt Trigger inputs and a three-clock cycle delay filter combine to reject low-level noise and large, short duration, noise spikes that typically occur in noise prone applications, such as a motor system.

The filter ensures that the filtered output signal is not permitted to change until a stable value has been registered for three consecutive clock cycles.

For the QEA, QEB and INDX pins, the clock divide frequency for the digital filter is programmed by bits QECK<2:0> (DFLTCON<6:4>) and are derived from the base instruction cycle Tcy.

To enable the filter output for channels QEA, QEB and INDX, the QEOUT bit must be '1'. The filter network for all channels is disabled on POR and BOR.

14.5 Alternate 16-bit Timer/Counter

When the QEI module is not configured for the QEI mode, QEIM<2:0> = 001, the module can be configured as a simple 16-bit timer/counter. The setup and control of the auxiliary timer is accomplished through the QEICON SFR register. This timer functions identically to Timer1. The QEA pin is used as the timer clock input.

When configured as a timer, the POSCNT register serves as the Timer Count register and the MAXCNT register serves as the Period register. When a Timer/Period register match occurs, the QEI interrupt flag will be asserted.

The only exception between the general purpose timers and this timer is the added feature of external up/down input select. When the UPDN pin is asserted high, the timer will increment up. When the UPDN pin is asserted low, the timer will be decremented.

Note: Changing the operational mode (i.e., from QEI to timer or vice versa) will not affect the Timer/Position Count register contents.

The UPDN control/status bit (QEICON<11>) can be used to select the count direction state of the Timer register. When UPDN = 1, the timer will count up. When UPDN = 0, the timer will count down.

In addition, control bit, UPDN_SRC (QEICON<0>), determines whether the timer count direction state is based on the logic state written into the UPDN control/status bit (QEICON<11>) or the QEB pin state. When UPDN_SRC = 1, the timer count direction is controlled from the QEB pin. Likewise, when UPDN_SRC = 0, the timer count direction is controlled by the UPDN bit.

Note: This timer does not support the External Asynchronous Counter mode of operation. If using an external clock source, the clock will automatically be synchronized to the internal instruction cycle.

14.6 QEI Module Operation During CPU Sleep Mode

14.6.1 QEI OPERATION DURING CPU SLEEP MODE

The QEI module will be halted during the CPU Sleep mode.

14.6.2 TIMER OPERATION DURING CPU SLEEP MODE

During CPU Sleep mode, the timer will not operate because the internal clocks are disabled.

18.2 Enabling and Setting Up UART

18.2.1 ENABLING THE UART

The UART module is enabled by setting the UARTEN bit in the UxMODE register (where x = 1 or 2). Once enabled, the UxTX and UxRX pins are configured as an output and an input, respectively, overriding the TRIS and LATCH register bit settings for the corresponding I/O port pins. The UxTX pin is at logic '1' when no transmission is taking place.

18.2.2 DISABLING THE UART

The UART module is disabled by clearing the UARTEN bit in the UxMODE register. This is the default state after any Reset. If the UART is disabled, all I/O pins operate as port pins under the control of the LATCH and TRIS bits of the corresponding port pins.

Disabling the UART module resets the buffers to empty states. Any data characters in the buffers are lost and the baud rate counter is reset.

All error and status flags associated with the UART module are reset when the module is disabled. The URXDA, OERR, FERR, PERR, UTXEN, UTXBRK and UTXBF bits are cleared, whereas RIDLE and TRMT are set. Other control bits, including ADDEN, URXISEL<1:0>, UTXISEL, as well as the UxMODE and UxBRG registers, are not affected.

Clearing the UARTEN bit while the UART is active will abort all pending transmissions and receptions and reset the module as defined above. Re-enabling the UART will restart the UART in the same configuration.

18.2.3 ALTERNATE I/O

The alternate I/O function is enabled by setting the ALTIO bit (UxMODE<10>). If ALTIO = 1, the UxATX and UxARX pins (alternate transmit and alternate receive pins, respectively) are used by the UART module instead of the UxTX and UxRX pins. If ALTIO = 0, the UxTX and UxRX pins are used by the UART module.

18.2.4 SETTING UP DATA, PARITY AND STOP BIT SELECTIONS

Control bits, PDSEL<1:0> in the UxMODE register, are used to select the data length and parity used in the transmission. The data length may either be 8 bits with even, odd or no parity, or 9-bits with no parity.

The STSEL bit determines whether one or two Stop bits will be used during data transmission.

The default (power-on) setting of the UART is 8 bits, no parity and 1 Stop bit (typically represented as 8, N, 1).

18.3 Transmitting Data

18.3.1 TRANSMITTING IN 8-BIT DATA MODE

The following steps must be performed in order to transmit 8-bit data:

1. Set up the UART:
First, the data length, parity and number of Stop bits must be selected. Then, the transmit and receive interrupt enable and priority bits are set up in the UxMODE and UxSTA registers. Also, the appropriate baud rate value must be written to the UxBRG register.
2. Enable the UART by setting the UARTEN bit (UxMODE<15>).
3. Set the UTXEN bit (UxSTA<10>), thereby enabling a transmission.
4. Write the byte to be transmitted to the lower byte of UxTXREG. The value will be transferred to the Transmit Shift register (UxTSR) immediately and the serial bit stream will start shifting out during the next rising edge of the baud clock. Alternatively, the data byte may be written while UTXEN = 0, following which, the user may set UTXEN. This will cause the serial bit stream to begin immediately because the baud clock will start from a cleared state.
5. A transmit interrupt will be generated depending on the value of the interrupt control bit UTXISEL (UxSTA<15>).

18.3.2 TRANSMITTING IN 9-BIT DATA MODE

The sequence of steps involved in the transmission of 9-bit data is similar to 8-bit transmission, except that a 16-bit data word (of which the upper 7 bits are always clear) must be written to the UxTXREG register.

18.3.3 TRANSMIT BUFFER (UxTXB)

The transmit buffer is 9 bits wide and 4 characters deep. Including the Transmit Shift register (UxTSR), the user effectively has a 5-deep FIFO (First In First Out) buffer. The UTXBF Status bit (UxSTA<9>) indicates whether the transmit buffer is full.

If a user attempts to write to a full buffer, the new data will not be accepted into the FIFO, and no data shift will occur within the buffer. This enables recovery from a buffer overrun condition.

The FIFO is reset during any device Reset, but is not affected when the device enters or wakes up from a power-saving mode.

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NOTES:

20.4 Programming the Start of the Conversion Trigger

The conversion trigger terminates acquisition and starts the requested conversions.

The SSRC<2:0> bits select the source of the conversion trigger.

The SSRC bits provide for up to five alternate sources of conversion trigger.

When SSRC<2:0> = 000, the conversion trigger is under software control. Clearing the SAMP bit causes the conversion trigger.

When SSRC<2:0> = 111 (Auto-Start mode), the conversion trigger is under A/D clock control. The SAMC bits select the number of A/D clocks between the start of acquisition and the start of conversion. This provides the fastest conversion rates on multiple channels. SAMC must always be at least one clock cycle.

Other trigger sources can come from timer modules, motor control PWM module or external interrupts.

Note: To operate the ADC at the maximum specified conversion speed, the auto-convert trigger option should be selected (SSRC = 111) and the auto-sample time bits should be set to '1' TAD (SAMC = 00001). This configuration gives a total conversion period (sample + convert) of 13 TAD.

The use of any other conversion trigger results in additional TAD cycles to synchronize the external event to the ADC.

20.5 Aborting a Conversion

Clearing the ADON bit during a conversion aborts the current conversion and stops the sampling sequencing. The ADCBUFx is not updated with the partially completed A/D conversion sample. That is, the ADCBUFx will continue to contain the value of the last completed conversion (or the last value written to the ADCBUFx register).

If the clearing of the ADON bit coincides with an auto-start, the clearing has a higher priority.

After the A/D conversion is aborted, a 2 TAD wait is required before the next sampling may be started by setting the SAMP bit.

If sequential sampling is specified, the A/D continues at the next sample pulse, which corresponds with the next channel converted. If simultaneous sampling is specified, the A/D continues with the next multichannel group conversion sequence.

20.6 Selecting the A/D Conversion Clock

The A/D conversion requires 12 TAD. The source of the A/D conversion clock is software selected using a 6-bit counter. There are 64 possible options for TAD.

EQUATION 20-1: A/D CONVERSION CLOCK

$$TAD = T_{CY} * (0.5 * (ADCS<5:0> + 1))$$

$$ADCS<5:0> = 2 \frac{TAD}{T_{CY}} - 1$$

The internal RC oscillator is selected by setting the ADRC bit.

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time of 83.33 nsec (for VDD = 5V). Refer to **Section 24.0 "Electrical Characteristics"** for minimum TAD under other operating conditions.

Example 20-1 shows a sample calculation for the ADCS<5:0> bits, assuming a device operating speed of 30 MIPS.

EXAMPLE 20-1: A/D CONVERSION CLOCK CALCULATION

$$TAD = 154 \text{ nsec}$$

$$T_{CY} = 33 \text{ nsec (30 MIPS)}$$

$$ADCS<5:0> = 2 \frac{TAD}{T_{CY}} - 1$$

$$= 2 \cdot \frac{154 \text{ nsec}}{33 \text{ nsec}} - 1$$

$$= 8.33$$

Therefore,
Set ADCS<5:0> = 9

$$\text{Actual } TAD = \frac{T_{CY}}{2} (ADCS<5:0> + 1)$$

$$= \frac{33 \text{ nsec}}{2} (9 + 1)$$

$$= 165 \text{ nsec}$$

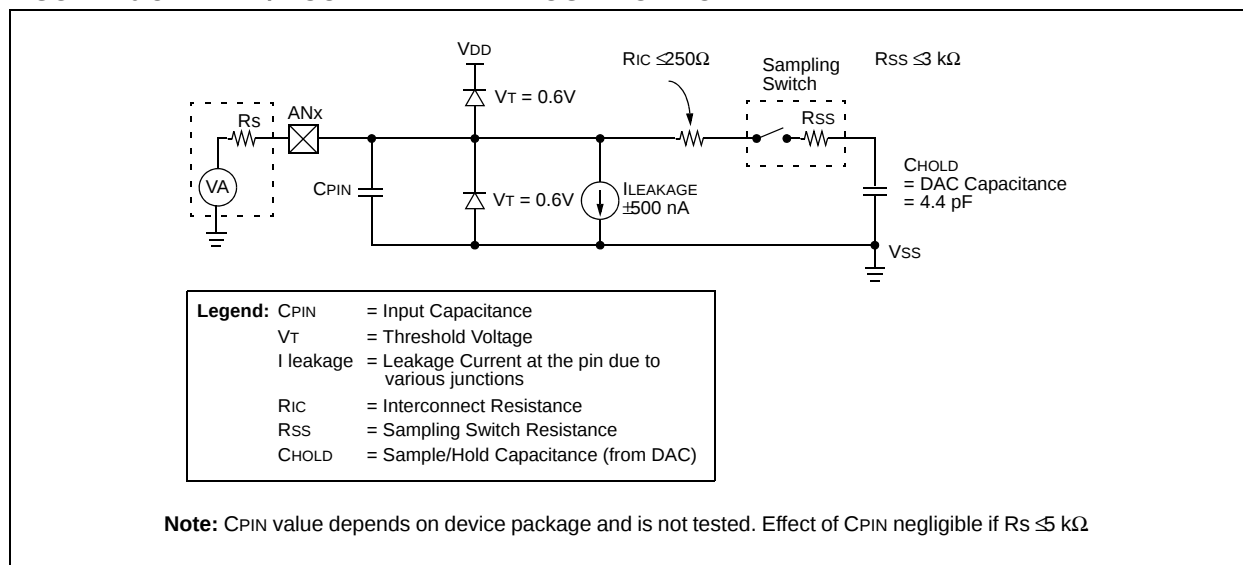
20.8 A/D Acquisition Requirements

The analog input model of the 10-bit ADC is shown in Figure 20-3. The total sampling time for the ADC is a function of the internal amplifier settling time, device V_{DD} and the holding capacitor charge time.

For the ADC to meet its specified accuracy, the charge holding capacitor (C_{HOLD}) must be allowed to fully charge to the voltage level on the analog input pin. The source impedance (R_S), the interconnect impedance (R_{IC}) and the internal sampling switch (R_{SS}) impedance combine to directly affect the time required to charge the capacitor C_{HOLD} . The combined impedance of the analog sources must therefore be small enough to fully charge the holding capacitor within the chosen sample time. To minimize the effects of pin leakage currents on the accuracy of the ADC, the maximum recommended source impedance, R_S , is 5 k Ω . After the analog input channel is selected (changed), this sampling function must be completed prior to starting the conversion. The internal holding capacitor will be in a discharged state prior to each sample operation.

The user must allow at least 1 T_{AD} period of sampling time, T_{SAMP} , between conversions to allow each sample to be acquired. This sample time may be controlled manually in software by setting/clearing the SAMP bit, or it may be automatically controlled by the ADC. In an automatic configuration, the user must allow enough time between conversion triggers so that the minimum sample time can be satisfied. Refer to **Section 24.0 “Electrical Characteristics”** for T_{AD} and sample time requirements.

FIGURE 20-3: A/D CONVERTER ANALOG INPUT MODEL



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NOTES:

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Table 21-5 lists the Reset conditions for the RCON Register. Since the control bits within the RCON register are R/W, the information in the table implies that all the bits are negated prior to the action specified in the condition column.

TABLE 21-5: INITIALIZATION CONDITION FOR RCON REGISTER, CASE 1

Condition	Program Counter	TRAPR	IOPUWR	EXTR	SWR	WDTO	IDLE	SLEEP	POR	BOR
Power-on Reset	0x000000	0	0	0	0	0	0	0	1	1
Brown-out Reset	0x000000	0	0	0	0	0	0	0	0	1
MCLR Reset during normal operation	0x000000	0	0	1	0	0	0	0	0	0
Software Reset during normal operation	0x000000	0	0	0	1	0	0	0	0	0
MCLR Reset during Sleep	0x000000	0	0	1	0	0	0	1	0	0
MCLR Reset during Idle	0x000000	0	0	1	0	0	1	0	0	0
WDT Time-out Reset	0x000000	0	0	0	0	1	0	0	0	0
WDT Wake-up	PC + 2	0	0	0	0	1	0	1	0	0
Interrupt Wake-up from Sleep	PC + 2 ⁽¹⁾	0	0	0	0	0	0	1	0	0
Clock Failure Trap	0x000004	0	0	0	0	0	0	0	0	0
Trap Reset	0x000000	1	0	0	0	0	0	0	0	0
Illegal Operation Trap	0x000000	0	1	0	0	0	0	0	0	0

Note 1: When the wake-up is due to an enabled interrupt, the PC is loaded with the corresponding interrupt vector.

Table 21-6 lists a second example of the bit conditions for the RCON register. In this case, it is not assumed that the user has set/cleared specific bits prior to action specified in the condition column.

TABLE 21-6: INITIALIZATION CONDITION FOR RCON REGISTER, CASE 2

Condition	Program Counter	TRAPR	IOPUWR	EXTR	SWR	WDTO	IDLE	SLEEP	POR	BOR
Power-on Reset	0x000000	0	0	0	0	0	0	0	1	1
Brown-out Reset	0x000000	u	u	u	u	u	u	u	0	1
MCLR Reset during normal operation	0x000000	u	u	1	0	0	0	0	u	u
Software Reset during normal operation	0x000000	u	u	0	1	0	0	0	u	u
MCLR Reset during Sleep	0x000000	u	u	1	u	0	0	1	u	u
MCLR Reset during Idle	0x000000	u	u	1	u	0	1	0	u	u
WDT Time-out Reset	0x000000	u	u	0	0	1	0	0	u	u
WDT Wake-up	PC + 2	u	u	u	u	1	u	1	u	u
Interrupt Wake-up from Sleep	PC + 2 ⁽¹⁾	u	u	u	u	u	u	1	u	u
Clock Failure Trap	0x000004	u	u	u	u	u	u	u	u	u
Trap Reset	0x000000	1	u	u	u	u	u	u	u	u
Illegal Operation Reset	0x000000	u	1	u	u	u	u	u	u	u

Legend: u = unchanged

Note 1: When the wake-up is due to an enabled interrupt, the PC is loaded with the corresponding interrupt vector.

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TABLE 22-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of words	# of cycles	Status Flags Affected
66	RRNC	RRNC f	f = Rotate Right (No Carry) f	1	1	N, Z
		RRNC f, WREG	WREG = Rotate Right (No Carry) f	1	1	N, Z
		RRNC ws, wd	Wd = Rotate Right (No Carry) Ws	1	1	N, Z
67	SAC	SAC Acc, #Slit4, Wdo	Store Accumulator	1	1	None
		SAC.R Acc, #Slit4, Wdo	Store Rounded Accumulator	1	1	None
68	SE	SE ws, Wnd	Wnd = sign-extended Ws	1	1	C, N, Z
69	SETM	SETM f	f = 0xFFFF	1	1	None
		SETM WREG	WREG = 0xFFFF	1	1	None
		SETM ws	Ws = 0xFFFF	1	1	None
70	SFTAC	SFTAC Acc, Wn	Arithmetic Shift Accumulator by (Wn)	1	1	OA, OB, OAB, SA, SB, SAB
		SFTAC Acc, #Slit6	Arithmetic Shift Accumulator by Slit6	1	1	OA, OB, OAB, SA, SB, SAB
71	SL	SL f	f = Left Shift f	1	1	C, N, OV, Z
		SL f, WREG	WREG = Left Shift f	1	1	C, N, OV, Z
		SL ws, wd	Wd = Left Shift Ws	1	1	C, N, OV, Z
		SL wb, Wns, Wnd	Wnd = Left Shift Wb by Wns	1	1	N, Z
		SL wb, #lit5, Wnd	Wnd = Left Shift Wb by lit5	1	1	N, Z
72	SUB	SUB Acc	Subtract Accumulators	1	1	OA, OB, OAB, SA, SB, SAB
		SUB f	f = f – WREG	1	1	C, DC, N, OV, Z
		SUB f, WREG	WREG = f – WREG	1	1	C, DC, N, OV, Z
		SUB #lit10, Wn	Wn = Wn – lit10	1	1	C, DC, N, OV, Z
		SUB wb, ws, wd	Wd = Wb – Ws	1	1	C, DC, N, OV, Z
		SUB wb, #lit5, wd	Wd = Wb – lit5	1	1	C, DC, N, OV, Z
73	SUBB	SUBB f	f = f – WREG – ($\overline{C}$)	1	1	C, DC, N, OV, Z
		SUBB f, WREG	WREG = f – WREG – ($\overline{C}$)	1	1	C, DC, N, OV, Z
		SUBB #lit10, Wn	Wn = Wn – lit10 – ($\overline{C}$)	1	1	C, DC, N, OV, Z
		SUBB wb, ws, wd	Wd = Wb – Ws – ($\overline{C}$)	1	1	C, DC, N, OV, Z
		SUBB wb, #lit5, wd	Wd = Wb – lit5 – ($\overline{C}$)	1	1	C, DC, N, OV, Z
74	SUBR	SUBR f	f = WREG – f	1	1	C, DC, N, OV, Z
		SUBR f, WREG	WREG = WREG – f	1	1	C, DC, N, OV, Z
		SUBR wb, ws, wd	Wd = Ws – Wb	1	1	C, DC, N, OV, Z
		SUBR wb, #lit5, wd	Wd = lit5 – Wb	1	1	C, DC, N, OV, Z
75	SUBBR	SUBBR f	f = WREG – f – ($\overline{C}$)	1	1	C, DC, N, OV, Z
		SUBBR f, WREG	WREG = WREG – f – ($\overline{C}$)	1	1	C, DC, N, OV, Z
		SUBBR wb, ws, wd	Wd = Ws – Wb – ($\overline{C}$)	1	1	C, DC, N, OV, Z
		SUBBR wb, #lit5, wd	Wd = lit5 – Wb – ($\overline{C}$)	1	1	C, DC, N, OV, Z
76	SWAP	SWAP.b wn	Wn = nibble swap Wn	1	1	None
		SWAP wn	Wn = byte swap Wn	1	1	None
77	TBLRDH	TBLRDH ws, wd	Read Prog<23:16> to Wd<7:0>	1	2	None
78	TBLRDL	TBLRDL ws, wd	Read Prog<15:0> to Wd	1	2	None
79	TBLWTH	TBLWTH ws, wd	Write Ws<7:0> to Prog<23:16>	1	2	None
80	TBLWTL	TBLWTL ws, wd	Write Ws to Prog<15:0>	1	2	None
81	ULNK	ULNK	Unlink Frame Pointer	1	1	None
82	XOR	XOR f	f = f .XOR. WREG	1	1	N, Z
		XOR f, WREG	WREG = f .XOR. WREG	1	1	N, Z
		XOR #lit10, Wn	Wd = lit10 .XOR. Wd	1	1	N, Z
		XOR wb, ws, wd	Wd = Wb .XOR. Ws	1	1	N, Z
		XOR wb, #lit5, wd	Wd = Wb .XOR. lit5	1	1	N, Z
83	ZE	ZE ws, Wnd	Wnd = Zero-Extend Ws	1	1	C, N, Z

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TABLE 24-17: AC CHARACTERISTICS: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
Internal FRC Accuracy @ FRC Freq. = 7.37 MHz ⁽¹⁾							
OS63	FRC	—	—	±2.00	%	-40°C ≤TA ≤+85°C	VDD = 3.0-5.5V
		—	—	±5.00	%	-40°C ≤TA ≤+125°C	VDD = 3.0-5.5V

Note 1: Frequency calibrated at 7.372 MHz ±2%, 25°C and 5V. TUN<3:0> bits can be used to compensate for temperature drift.

TABLE 24-18: AC CHARACTERISTICS: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended				
Param No.	Characteristic	Min	Typ	Max	Units	Conditions
LPRC @ Freq. = 512 kHz ⁽¹⁾						
OS65A		-50	—	+50	%	VDD = 5.0V, ±10%
OS65B		-60	—	+60	%	VDD = 3.3V, ±10%
OS65C		-70	—	+70	%	VDD = 2.5V

Note 1: Change of LPRC frequency as VDD changes.

FIGURE 24-16: SPI MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS

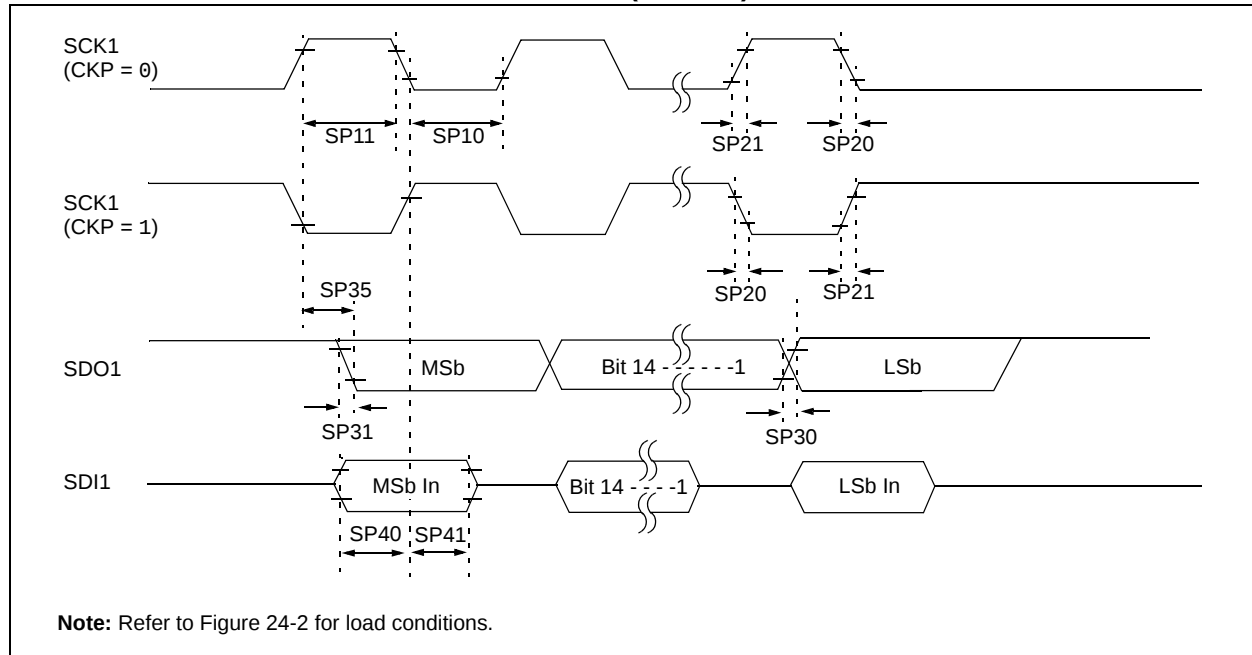


TABLE 24-32: SPI MASTER MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ ⁽²⁾	Max	Units	Conditions
SP10	TscL	SCK1 Output Low Time ⁽³⁾	Tcy/2	—	—	ns	
SP11	TscH	SCK1 Output High Time ⁽³⁾	Tcy/2	—	—	ns	
SP20	TscF	SCK1 Output Fall Time ⁽⁴⁾	—	—	—	ns	See parameter DO32
SP21	TscR	SCK1 Output Rise Time ⁽⁴⁾	—	—	—	ns	See parameter DO31
SP30	TdoF	SDO1 Data Output Fall Time ⁽⁴⁾	—	—	—	ns	See parameter DO32
SP31	TdoR	SDO1 Data Output Rise Time ⁽⁴⁾	—	—	—	ns	See parameter DO31
SP35	Tsch2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	—	30	ns	
SP40	TdiV2sch, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCK1 is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI pins.

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FIGURE 24-17: SPI MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS

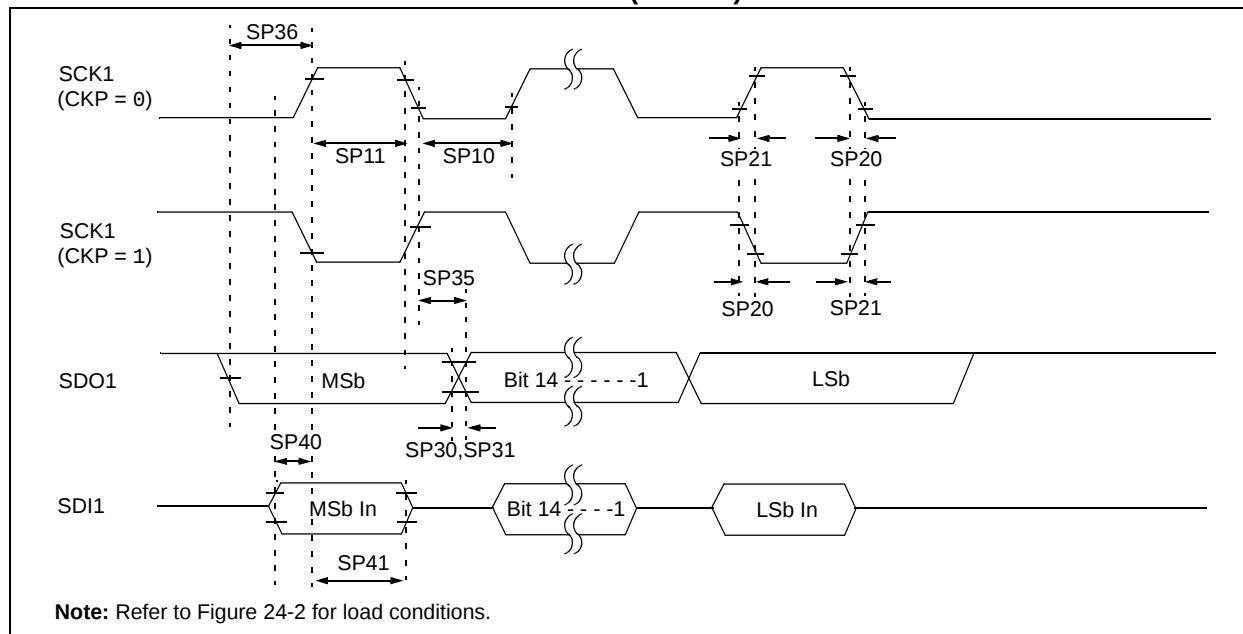


TABLE 24-33: SPI MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ ⁽²⁾	Max	Units	Conditions
SP10	TscL	SCK1 Output Low Time ⁽³⁾	Tcy/2	—	—	ns	
SP11	TscH	SCK1 Output High Time ⁽³⁾	Tcy/2	—	—	ns	
SP20	TscF	SCK1 Output Fall Time ⁽⁴⁾	—	—	—	ns	See parameter DO32
SP21	TscR	SCK1 Output Rise Time ⁽⁴⁾	—	—	—	ns	See parameter DO31
SP30	TdoF	SDO1 Data Output Fall Time ⁽⁴⁾	—	—	—	ns	See parameter DO32
SP31	TdoR	SDO1 Data Output Rise Time ⁽⁴⁾	—	—	—	ns	See parameter DO31
SP35	Tsch2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	—	30	ns	
SP36	TdoV2sc, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	

- Note 1:** These parameters are characterized but not tested in manufacturing.
- Note 2:** Data in "Typ" column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- Note 3:** The minimum clock period for SCK1 is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.
- Note 4:** Assumes 50 pF load on all SPI pins.

FIGURE 24-26: 10-BIT HIGH-SPEED A/D CONVERSION TIMING CHARACTERISTICS
(CHPS<1:0> = 01, SIMSAM = 0, ASAM = 1, SSRC<2:0> = 111, SAMC<4:0> = 00001)

