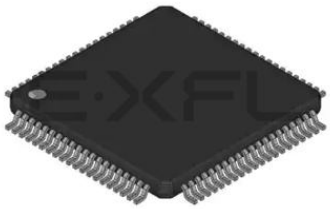
# Infineon Technologies - XC2336A72F80LAAHXUMA1 Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | C166SV2 |
| Core Size | 16/32-Bit |
| Speed | 80MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI |
| Peripherals | I²S, POR, PWM, WDT |
| Number of I/O | 40 |
| Program Memory Size | 576KB (576K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 50K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 9x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | PG-LQFP-64-13 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xc2336a72f80laahxuma1 |

**16/32-Bit Single-Chip Microcontroller with 32-Bit Performance**

**XC233xA (XC2000 Family)**

# 1 Summary of Features

For a quick overview and easy reference, the features of the XC233xA are summarized here.

- High-performance CPU with five-stage pipeline and MPU
  - 12.5 ns instruction cycle at 80 MHz CPU clock (single-cycle execution)
  - One-cycle 32-bit addition and subtraction with 40-bit result
  - One-cycle multiplication (16 × 16 bit)
  - Background division (32 / 16 bit) in 21 cycles
  - One-cycle multiply-and-accumulate (MAC) instructions
  - Enhanced Boolean bit manipulation facilities
  - Zero-cycle jump execution
  - Additional instructions to support HLL and operating systems
  - Register-based design with multiple variable register banks
  - Fast context switching support with two additional local register banks
  - 16 Mbytes total linear address space for code and data
  - 1024 Bytes on-chip special function register area (C166 Family compatible)
  - Integrated Memory Protection Unit (MPU)
- Interrupt system with 16 priority levels for up to 96 sources
  - Selectable external inputs for interrupt generation and wake-up
  - Fastest sample-rate 12.5 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- Hardware CRC-Checker with Programmable Polynomial to Supervise On-Chip Memory Areas
- On-chip memory modules
  - 8 Kbytes on-chip stand-by RAM (SBRAM)
  - 2 Kbytes on-chip dual-port RAM (DPRAM)
  - Up to 16 Kbytes on-chip data SRAM (DSRAM)
  - Up to 32 Kbytes on-chip program/data SRAM (PSRAM)
  - Up to 576 Kbytes on-chip program memory (Flash memory)
  - Memory content protection through Error Correction Code (ECC)
- On-Chip Peripheral Modules
  - Multi-functional general purpose timer unit with 5 timers
  - 16-channel general purpose capture/compare unit (CAPCOM2)
  - Two capture/compare units for flexible PWM signal generation (CCU6x)

The XC233xA types are offered with several SRAM memory sizes. **Figure 1** shows the allocation rules for PSRAM and DSRAM. Note that the rules differ:

- PSRAM allocation starts from the **lower** address
- DSRAM allocation starts from the **higher** address

For example 8 Kbytes of PSRAM will be allocated at E0’0000h-E0’1FFFh and 8 Kbytes of DSRAM will be at 00’C000h-00’DFFFh.

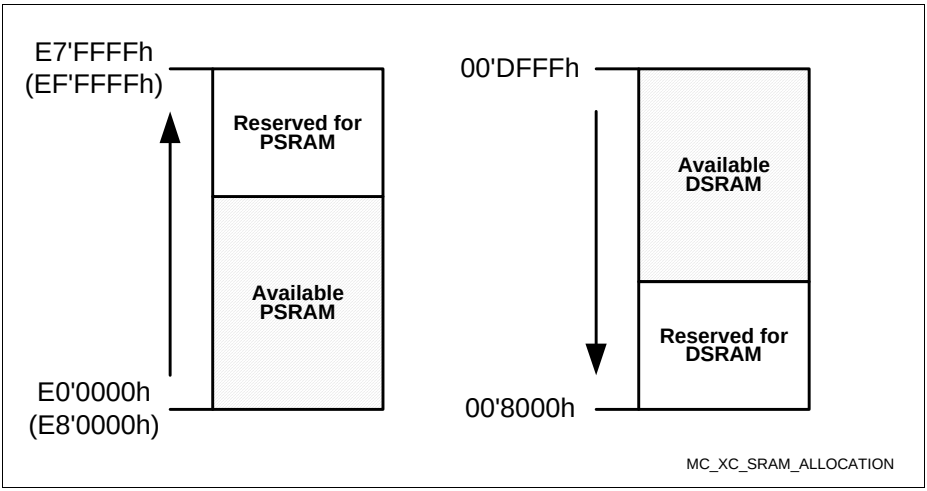


**Figure 1 SRAM Allocation**

# 2 General Device Information

The XC233xA series (16/32-Bit Single-Chip Microcontroller with 32-Bit Performance) is a part of the Infineon XC2000 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 80 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

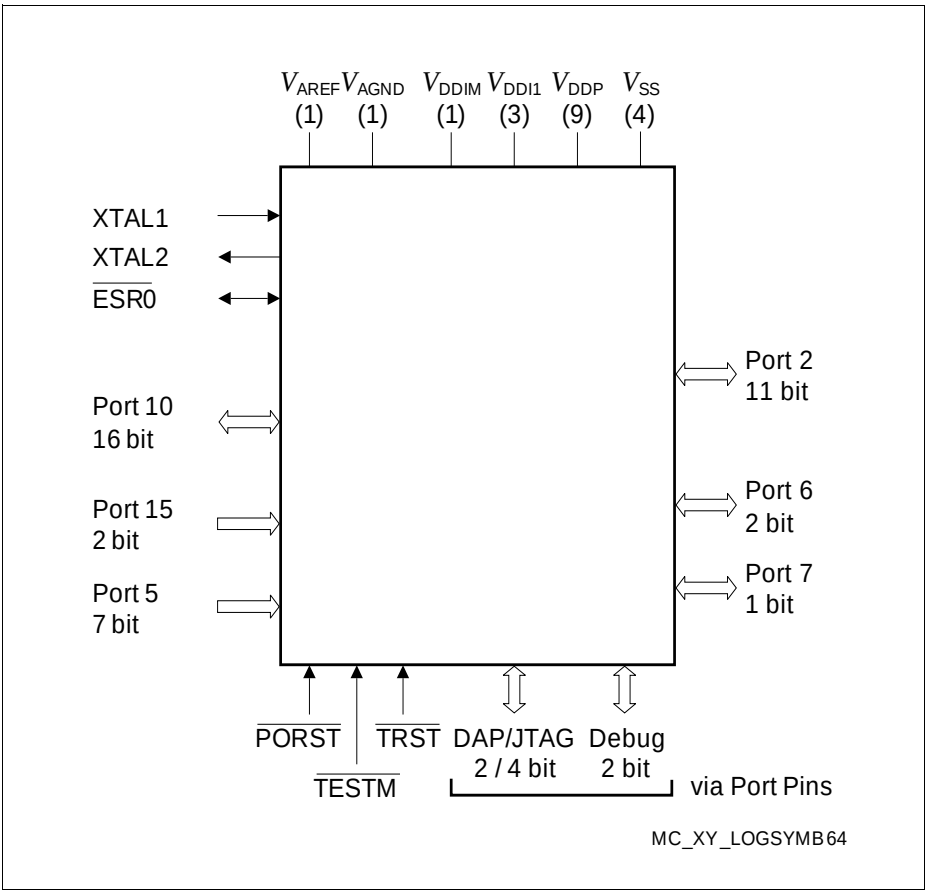


**Figure 2 XC233xA Logic Symbol**

### Key to Pin Definitions

- **Ctrl.**: The output signal for a port pin is selected by bit field PC in the associated register Px_IOCRy. Output O0 is selected by setting the respective bit field PC to $1x00_B$, output O1 is selected by $1x01_B$, etc.
  Output signal OH is controlled by hardware.
- **Type**: Indicates the pad type and its power supply domain (A, B, M, 1).
  - St: Standard pad
  - Sp: Special pad e.g. XTALx
  - DP: Double pad - can be used as standard or high speed pad
  - In: Input only pad
  - PS: Power supply pad

**Table 6 Pin Definitions and Functions**

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 3 | $\overline{\text{TESTM}}$ | I | In/B | **Testmode Enable**<br>Enables factory test modes, must be held HIGH for normal operation (connect to $V_{DDPB}$).<br>An internal pull-up device will hold this pin high when nothing is driving it. |
| 4 | $\overline{\text{TRST}}$ | I | In/B | **Test-System Reset Input**<br>For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XC233xA's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system.<br>An internal pull-down device will hold this pin low when nothing is driving it. |
| 5 | P7.0 | O0 / I | St/B | **Bit 0 of Port 7, General Purpose Input/Output** |
| | T3OUT | O1 | St/B | **GPT12E Timer T3 Toggle Latch Output** |
| | T6OUT | O2 | St/B | **GPT12E Timer T6 Toggle Latch Output** |
| | TDO_A | OH / IH | St/B | **JTAG Test Data Output / DAP1 Input/Output**<br>If DAP pos. 0 or 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it. |
| | ESR2_1 | I | St/B | **ESR2 Trigger Input 1** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 20 | P5.8 | I | In/A | **Bit 8 of Port 5, General Purpose Input** |
| | ADC0_CH8 | I | In/A | **Analog Input Channel 8 for ADC0** |
| | ADC1_CH8 | I | In/A | **Analog Input Channel 8 for ADC1** |
| | CCU6x_T12HRC | I | In/A | **External Run Control Input for T12 of CCU60/1** |
| | CCU6x_T13HRC | I | In/A | **External Run Control Input for T13 of CCU60/1** |
| 21 | P5.10 | I | In/A | **Bit 10 of Port 5, General Purpose Input** |
| | ADC0_CH10 | I | In/A | **Analog Input Channel 10 for ADC0** |
| | ADC1_CH10 | I | In/A | **Analog Input Channel 10 for ADC1** |
| | $\overline{\text{BRKIN\_A}}$ | I | In/A | **OCDS Break Signal Input** |
| | CCU61_T13HRA | I | In/A | **External Run Control Input for T13 of CCU61** |
| 22 | P5.13 | I | In/A | **Bit 13 of Port 5, General Purpose Input** |
| | ADC0_CH13 | I | In/A | **Analog Input Channel 13 for ADC0** |
| 23 | P5.15 | I | In/A | **Bit 15 of Port 5, General Purpose Input** |
| | ADC0_CH15 | I | In/A | **Analog Input Channel 15 for ADC0** |
| 25 | P2.0 | O0 / I | St/B | **Bit 0 of Port 2, General Purpose Input/Output** |
| | RxDC0C | I | St/B | **CAN Node 0 Receive Data Input** |
| | T5INB | I | St/B | **GPT12E Timer T5 Count/Gate Input** |
| 26 | P2.1 | O0 / I | St/B | **Bit 1 of Port 2, General Purpose Input/Output** |
| | TxDC0 | O1 | St/B | **CAN Node 0 Transmit Data Output** |
| | T5EUDB | I | St/B | **GPT12E Timer T5 External Up/Down Control Input** |
| | ESR1_5 | I | St/B | **ESR1 Trigger Input 5** |
| 27 | P2.2 | O0 / I | St/B | **Bit 2 of Port 2, General Purpose Input/Output** |
| | TxDC1 | O1 | St/B | **CAN Node 1 Transmit Data Output** |
| | ESR2_5 | I | St/B | **ESR2 Trigger Input 5** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 38 | P10.0 | O0 / I | St/B | **Bit 0 of Port 10, General Purpose Input/Output** |
| | U0C1_DOUT | O1 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | CCU60_CC60 | O2 | St/B | **CCU60 Channel 0 Output** |
| | CCU60_CC60INA | I | St/B | **CCU60 Channel 0 Input** |
| | ESR1_2 | I | St/B | **ESR1 Trigger Input 2** |
| | U0C0_DX0A | I | St/B | **USIC0 Channel 0 Shift Data Input** |
| | U0C1_DX0A | I | St/B | **USIC0 Channel 1 Shift Data Input** |
| 39 | P10.1 | O0 / I | St/B | **Bit 1 of Port 10, General Purpose Input/Output** |
| | U0C0_DOUT | O1 | St/B | **USIC0 Channel 0 Shift Data Output** |
| | CCU60_CC61 | O2 | St/B | **CCU60 Channel 1 Output** |
| | CCU60_CC61INA | I | St/B | **CCU60 Channel 1 Input** |
| | U0C0_DX1A | I | St/B | **USIC0 Channel 0 Shift Clock Input** |
| | U0C0_DX0B | I | St/B | **USIC0 Channel 0 Shift Data Input** |
| 40 | P10.2 | O0 / I | St/B | **Bit 2 of Port 10, General Purpose Input/Output** |
| | U0C0_SCLKOUT | O1 | St/B | **USIC0 Channel 0 Shift Clock Output** |
| | CCU60_CC62 | O2 | St/B | **CCU60 Channel 2 Output** |
| | CCU60_CC62INA | I | St/B | **CCU60 Channel 2 Input** |
| | U0C0_DX1B | I | St/B | **USIC0 Channel 0 Shift Clock Input** |
| 42 | P2.10 | O0 / I | St/B | **Bit 10 of Port 2, General Purpose Input/Output** |
| | U0C1_DOUT | O1 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | U0C0_SELO3 | O2 | St/B | **USIC0 Channel 0 Select/Control 3 Output** |
| | CC2_CC23 | O3 / I | St/B | **CAPCOM2 CC23IO Capture Inp./ Compare Out.** |
| | U0C1_DX0E | I | St/B | **USIC0 Channel 1 Shift Data Input** |
| | CAPINA | I | St/B | **GPT12E Register CAPREL Capture Input** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 58 | P10.14 | O0 / I | St/B | **Bit 14 of Port 10, General Purpose Input/Output** |
| | U1C0_SELO 1 | O1 | St/B | **USIC1 Channel 0 Select/Control 1 Output** |
| | U0C1_DOUT | O2 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | ESR2_2 | I | St/B | **ESR2 Trigger Input 2** |
| | U0C1_DX0C | I | St/B | **USIC0 Channel 1 Shift Data Input** |
| 59 | P10.15 | O0 / I | St/B | **Bit 15 of Port 10, General Purpose Input/Output** |
| | U1C0_SELO 2 | O1 | St/B | **USIC1 Channel 0 Select/Control 2 Output** |
| | U0C1_DOUT | O2 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | U1C0_DOUT | O3 | St/B | **USIC1 Channel 0 Shift Data Output** |
| | U0C1_DX1C | I | St/B | **USIC0 Channel 1 Shift Clock Input** |
| 60 | XTAL2 | O | Sp/M | **Crystal Oscillator Amplifier Output** |
| 61 | XTAL1 | I | Sp/M | **Crystal Oscillator Amplifier Input**<br>To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Voltages on XTAL1 must comply to the core supply voltage $V_{DDIM}$. |
| | ESR2_9 | I | St/B | **ESR2 Trigger Input 9** |
| 62 | $\overline{\text{PORST}}$ | I | In/B | **Power On Reset Input**<br>A low level at this pin resets the XC233xA completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns.<br>An internal pull-up device will hold this pin high when nothing is driving it. |
| 63 | $\overline{\text{ESR0}}$ | O0 / I | St/B | **External Service Request 0**<br>After power-up, $\overline{\text{ESR0}}$ operates as open-drain bidirectional reset with a weak pull-up. |
| | U1C0_DX0E | I | St/B | **USIC1 Channel 0 Shift Data Input** |
| | U1C0_DX2B | I | St/B | **USIC1 Channel 0 Shift Control Input** |

## 3.5 Interrupt System

The architecture of the XC233xA supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Where in a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XC233xA has eight PEC channels, each whith fast interrupt-driven data transfer capabilities.

With a minimum interrupt response time of 7/11[1)] CPU clocks, the XC233xA can react quickly to the occurrence of non-deterministic events.

### Interrupt Nodes and Source Selection

The interrupt system provides 96 physical nodes with separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bit field. Most interrupt sources are assigned to a dedicated node. A particular subset of interrupt sources shares a set of nodes. The source selection can be programmed using the interrupt source selection (ISSR) registers.

### External Request Unit (ERU)

A dedicated External Request Unit (ERU) is provided to route and preprocess selected on-chip peripheral and external interrupt requests. The ERU features 4 programmable input channels with event trigger logic (ETL) a routing matrix and 4 output gating units (OGU). The ETL features rising edge, falling edge, or both edges event detection. The OGU combines the detected interrupt events and provides filtering capabilities depending on a programmable pattern match or miss.

### Trap Processing

The XC233xA provides efficient mechanisms to identify and process exceptions or error conditions that arise during run-time, the so-called ‘Hardware Traps’. A hardware trap causes an immediate system reaction similar to a standard interrupt service (branching

1) Depending if the jump cache is used or not.

## 3.7 Capture/Compare Unit (CAPCOM2)

The CAPCOM2 unit supports generation and control of timing sequences on up to 16 channels with a maximum resolution of one system clock cycle (eight cycles in staggered mode). The CAPCOM2 unit is typically used to handle high-speed I/O tasks such as pulse and waveform generation, pulse width modulation (PWM), digital to analog (D/A) conversion, software timing, or time recording with respect to external events.

Two 16-bit timers (T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range or variation for the timer period and resolution and allows precise adjustments to the application-specific requirements. In addition, an external count input allows event scheduling for the capture/compare registers relative to external events.

The capture/compare register array contains 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer and programmed for capture or compare function.
All registers have each one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘captured’) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

**Table 9 Compare Modes**

| Compare Modes | Function |
|---|---|
| Mode 0 | Interrupt-only compare mode;<br>Several compare interrupts per timer period are possible |
| Mode 1 | Pin toggles on each compare match;<br>Several compare events per timer period are possible |

## 3.13 MultiCAN Module

The MultiCAN module contains independently operating CAN nodes with Full-CAN functionality which are able to exchange Data and Remote Frames using a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to set up a FIFO buffer.

*Note: The number of CAN nodes and message objects depends on the selected device type.*

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to its own message object list and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

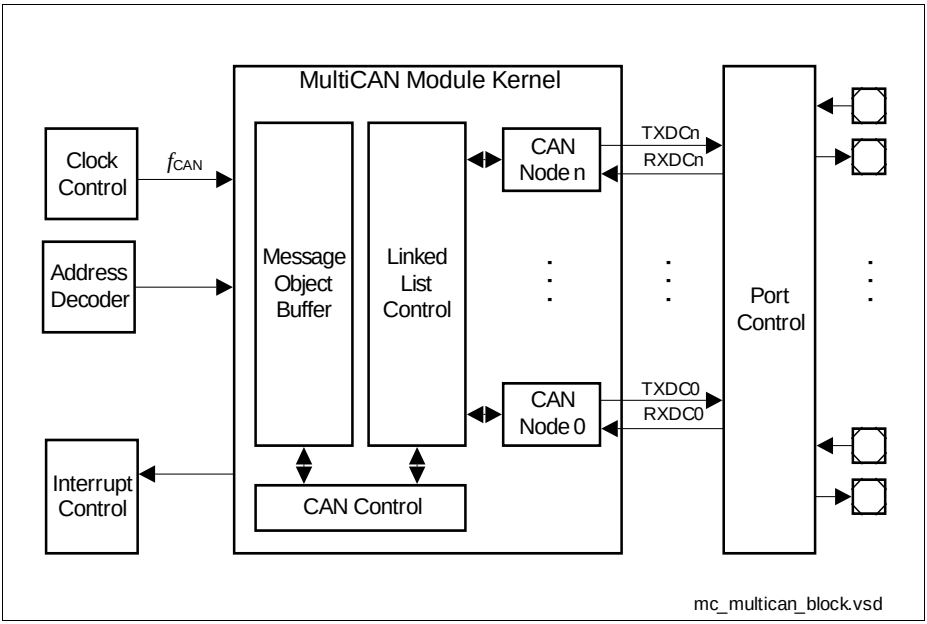


**Figure 12 Block Diagram of MultiCAN Module**

## 3.18 Instruction Set Summary

Table 11 lists the instructions of the XC233xA.
The addressing modes that can be used with a specific instruction, the function of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **“Instruction Set Manual”**.

This document also provides a detailed description of each instruction.

**Table 11 Instruction Set Summary**

| Mnemonic | Description | Bytes |
|---|---|---|
| ADD(B) | Add word (byte) operands | 2 / 4 |
| ADDC(B) | Add word (byte) operands with Carry | 2 / 4 |
| SUB(B) | Subtract word (byte) operands | 2 / 4 |
| SUBC(B) | Subtract word (byte) operands with Carry | 2 / 4 |
| MUL(U) | (Un)Signed multiply direct GPR by direct GPR (16- × 16-bit) | 2 |
| DIV(U) | (Un)Signed divide register MDL by direct GPR (16-/16-bit) | 2 |
| DIVL(U) | (Un)Signed long divide reg. MD by direct GPR (32-/16-bit) | 2 |
| CPL(B) | Complement direct word (byte) GPR | 2 |
| NEG(B) | Negate direct word (byte) GPR | 2 |
| AND(B) | Bitwise AND, (word/byte operands) | 2 / 4 |
| OR(B) | Bitwise OR, (word/byte operands) | 2 / 4 |
| XOR(B) | Bitwise exclusive OR, (word/byte operands) | 2 / 4 |
| BCLR/BSET | Clear/Set direct bit | 2 |
| BMOV(N) | Move (negated) direct bit to direct bit | 4 |
| BAND/BOR/BXOR | AND/OR/XOR direct bit with direct bit | 4 |
| BCMP | Compare direct bit to direct bit | 4 |
| BFLDH/BFLDL | Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data | 4 |
| CMP(B) | Compare word (byte) operands | 2 / 4 |
| CMPD1/2 | Compare word data to GPR and decrement GPR by 1/2 | 2 / 4 |
| CMPI1/2 | Compare word data to GPR and increment GPR by 1/2 | 2 / 4 |
| PRIOR | Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR | 2 |
| SHL/SHR | Shift left/right direct word GPR | 2 |

**Table 11 Instruction Set Summary** (cont'd)

| Mnemonic | Description | Bytes |
|---|---|---|
| ROL/ROR | Rotate left/right direct word GPR | 2 |
| ASHR | Arithmetic (sign bit) shift right direct word GPR | 2 |
| MOV(B) | Move word (byte) data | 2 / 4 |
| MOVBS/Z | Move byte operand to word op. with sign/zero extension | 2 / 4 |
| JMPA/I/R | Jump absolute/indirect/relative if condition is met | 4 |
| JMPS | Jump absolute to a code segment | 4 |
| JB(C) | Jump relative if direct bit is set (and clear bit) | 4 |
| JNB(S) | Jump relative if direct bit is not set (and set bit) | 4 |
| CALLA/I/R | Call absolute/indirect/relative subroutine if condition is met | 4 |
| CALLS | Call absolute subroutine in any code segment | 4 |
| PCALL | Push direct word register onto system stack and call absolute subroutine | 4 |
| TRAP | Call interrupt service routine via immediate trap number | 2 |
| PUSH/POP | Push/pop direct word register onto/from system stack | 2 |
| SCXT | Push direct word register onto system stack and update register with word operand | 4 |
| RET(P) | Return from intra-segment subroutine (and pop direct word register from system stack) | 2 |
| RETS | Return from inter-segment subroutine | 2 |
| RETI | Return from interrupt service subroutine | 2 |
| SBRK | Software Break | 2 |
| SRST | Software Reset | 4 |
| IDLE | Enter Idle Mode | 4 |
| PWRDN | Unused instruction[1)] | 4 |
| SRVWDT | Service Watchdog Timer | 4 |
| DISWDT/ENWDT | Disable/Enable Watchdog Timer | 4 |
| EINIT | End-of-Initialization Register Lock | 4 |
| ATOMIC | Begin ATOMIC sequence | 2 |
| EXTR | Begin EXTended Register sequence | 2 |
| EXTP(R) | Begin EXTended Page (and Register) sequence | 2 / 4 |
| EXTS(R) | Begin EXTended Segment (and Register) sequence | 2 / 4 |

### 4.2.1 DC Parameters

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current $I_{OV}$.

*Note: Operating Conditions apply.*

**Table 14** is valid under the following conditions:
$V_{DDP} \geq 4.5$ V; $V_{DDPtyp} = 5$ V; $V_{DDP} \leq 5.5$ V

**Table 14 DC Characteristics for Upper Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Pin capacitance (digital inputs/outputs). To be doubled for double bond pins.[1)] | $C_{IO}$ CC | – | – | 10 | pF | not subject to production test |
| Input Hysteresis[2)] | HYS CC | 0.11 x $V_{DDP}$ | – | – | V | $R_S$ = 0 Ohm |
| Absolute input leakage current on pins of analog ports[3)] | $\|I_{OZ1}\|$ CC | – | 10 | 200 | nA | $V_{IN} > 0$ V; $V_{IN} < V_{DDP}$ |
| Absolute input leakage current for all other pins. To be doubled for double bond pins.[3)1)4)] | $\|I_{OZ2}\|$ CC | – | 0.2 | 5 | µA | $T_J \leq 110$ °C; $V_{IN} < V_{DDP}$; $V_{IN} > V_{SS}$ |
| | | – | 0.2 | 15 | µA | $T_J \leq 150$ °C; $V_{IN} < V_{DDP}$; $V_{IN} > V_{SS}$ |
| Pull Level Force Current[5)] | $\|I_{PLF}\|$ SR | 250 | – | – | µA | [6)] |
| Pull Level Keep Current[7)] | $\|I_{PLK}\|$ SR | – | – | 30 | µA | [6)] |
| Input high voltage (all except XTAL1) | $V_{IH}$ SR | 0.7 x $V_{DDP}$ | – | $V_{DDP}$ + 0.3 | V | |
| Input low voltage (all except XTAL1) | $V_{IL}$ SR | -0.3 | – | 0.3 x $V_{DDP}$ | V | |
| Output High voltage[8)] | $V_{OH}$ CC | $V_{DDP}$ - 1.0 | – | – | V | $I_{OH} \geq I_{OHmax}$ |
| | | $V_{DDP}$ - 0.4 | – | – | V | $I_{OH} \geq I_{OHnom}$[9)] |

**Table 14 DC Characteristics for Upper Voltage Range** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output Low Voltage[8] | $V_{OL}$ CC | – | – | 1.0 | V | $I_{OL} \le I_{OLmax}$ |
| | | – | – | 0.4 | V | $I_{OL} \le I_{OLnom}$ [9] |

1) Because each double bond pin is connected to two pads (standard pad and high-speed pad), it has twice the normal value. For a list of affected pins refer to the pin definitions table in chapter 2.

2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

3) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{IN} < V_{SS}$) or supply ripple ($V_{IN} > V_{DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current ($I_{INJ}$) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor $K_{OV}$.

4) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature ($T_J$ = junction temperature [°C]): $I_{OZ} = 0.05 \times e^{(1.5 + 0.028 \times TJ>)}$ [µA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 µA. Leakage derating depending on voltage level (DV = $V_{DDP}$ - $V_{PIN}$ [V]): $I_{OZ} = I_{OZtempmax}$ - (1.6 x DV) (µA]. This voltage derating formula is an approximation which applies for maximum temperature.

5) Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \le V_{ILmax}$ for a pullup; $V_{PIN} \ge V_{IHmin}$ for a pulldown.

6) These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.

7) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \ge V_{IHmin}$ for a pullup; $V_{PIN} \le V_{ILmax}$ for a pulldown.

8) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.

9) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL}$->$V_{SS}$, $V_{OH}$->$V_{DDP}$). However, only the levels for nominal output currents are verified.

2) The pad supply voltage pins ($V_{DDPB}$) provide the input current for the on-chip EVVRs and the current consumed by the pin output drivers. A small current is consumed because the drivers input stages are switched.
   In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to 3 + 0.6 x $f_{SYS}$.
3) Please consider the additional conditions described in section "Active Mode Power Supply Current".

### Active Mode Power Supply Current

The actual power supply current in active mode not only depends on the system frequency but also on the configuration of the XC233xA's subsystem.

Besides the power consumed by the device logic the power supply pins also provide the current that flows through the pin output drivers.
A small current is consumed because the drivers' input stages are switched.

The IO power domains can be supplied separately. Power domain A ($V_{DDPA}$) supplies the A/D converters and Port 6. Power domain B ($V_{DDPB}$) supplies the on-chip EVVRs and all other ports.
During operation domain A draws a maximum current of 1.5 mA for each active A/D converter module from $V_{DDPA}$.

In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to (3 + 0.6×$f_{SYS}$) mA.

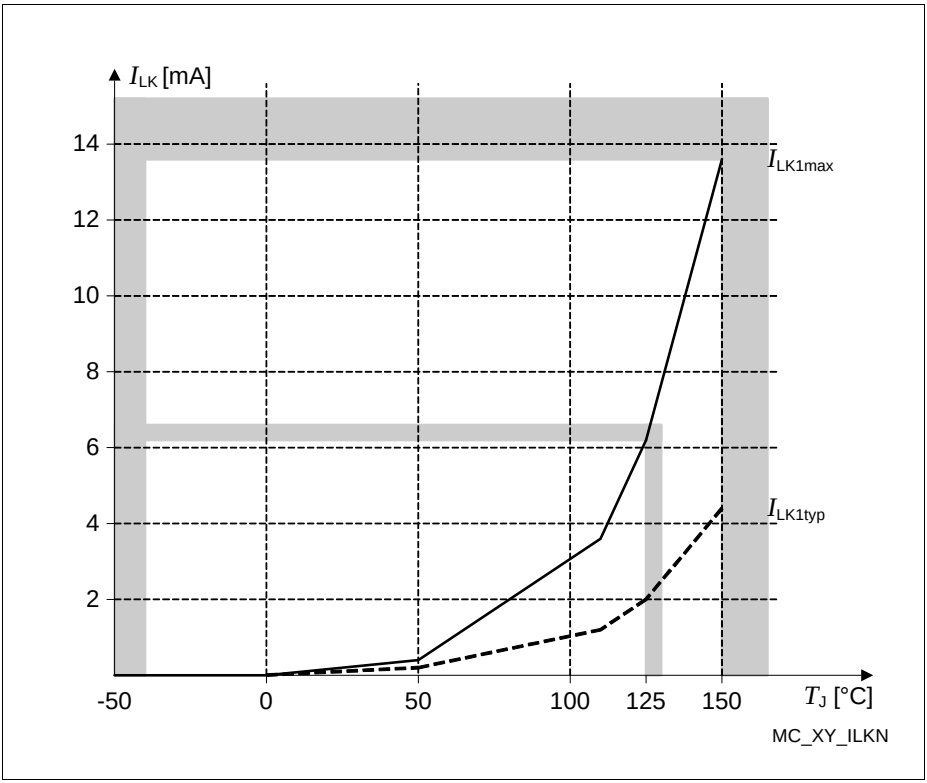


**Figure 15 Leakage Supply Current as a Function of Temperature**

**Table 23 Flash Parameters** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Number of erase cycles | $N_{Er}$ SR | – | – | 15 000 | cycles | $t_{RET}$ ≥ 5 years; Valid for up to 64 user-selected sectors (data storage) |
| | | – | – | 1 000 | cycles | $t_{RET}$ ≥ 20 years |

1) All Flash module(s) can be erased/programmed while code is executed and/or data is read from only one Flash module or from PSRAM. The Flash module that delivers code/data can, of course, not be erased/programmed.
2) Flash module 3 can be erased/programmed while code is executed and/or data is read from any other Flash module.
3) Value of IMB_IMBCTRL.WSFLASH.
4) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This increases the stated durations noticably only at extremely low system clock frequencies.

Access to the XC233xA Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.

### 4.6.4 Pad Properties

The output pad drivers of the XC233xA can operate in several user-selectable modes. Strong driver mode allows controlling external components requiring higher currents such as power bridges or LEDs. Reducing the driving power of an output pad reduces electromagnetic emissions (EME). In strong driver mode, selecting a slower edge reduces EME.

The dynamic behavior, i.e. the rise time and fall time, depends on the applied external capacitance that must be charged and discharged. Timing values are given for a capacitance of 20 pF, unless otherwise noted.

In general, the performance of a pad driver depends on the available supply voltage $V_{DDP}$. The following table lists the pad parameters.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

*Note: Operating Conditions apply.*

**Table 29 USIC SSC Master Mode Timing for Lower Voltage Range** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Receive data input setup time to SCLKOUT receive edge | $t_4$ SR | 40 | – | – | ns | |
| Data input DX0 hold time from SCLKOUT receive edge | $t_5$ SR | -5 | – | – | ns | |

1) $t_{SYS} = 1 / f_{SYS}$

**Table 30 USIC SSC Slave Mode Timing for Upper Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Select input DX2 setup to first clock input DX1 transmit edge[1)] | $t_{10}$ SR | 7 | – | – | ns | |
| Select input DX2 hold after last clock input DX1 receive edge[1)] | $t_{11}$ SR | 7 | – | – | ns | |
| Receive data input setup time to shift clock receive edge[1)] | $t_{12}$ SR | 7 | – | – | ns | |
| Data input DX0 hold time from clock input DX1 receive edge[1)] | $t_{13}$ SR | 5 | – | – | ns | |
| Data output DOUT valid time | $t_{14}$ CC | 7 | – | 33 | ns | |

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

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