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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | STM8 |
| Core Size | 8-Bit |
| Speed | 24MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 38 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 1.5K x 8 |
| RAM Size | 6K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.95V ~ 5.5V |
| Data Converters | A/D 10x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s207c8t3 |

# List of tables

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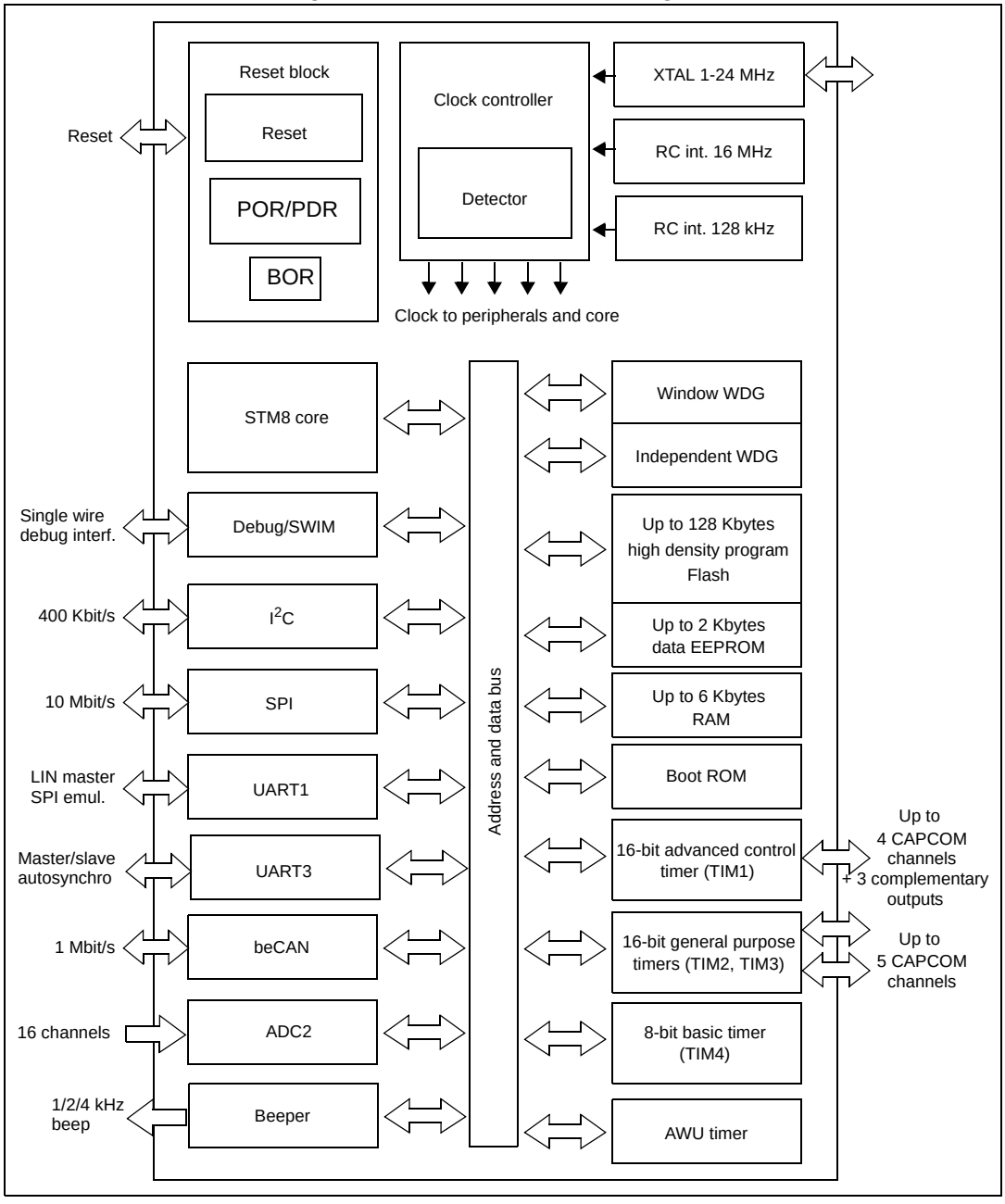
# 1 Introduction

This datasheet contains the description of the STM8S20xxx features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8S microcontroller memory, registers and peripherals, please refer to the STM8S microcontroller family reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8S Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

# 3 Block diagram

**Figure 1. STM8S20xxx block diagram**




1. Legend:
ADC: Analog-to-digital converter
beCAN: Controller area network
BOR: Brownout reset
I²C: Inter-integrated circuit multimaster interface
Independent WDG: Independent watchdog
POR/PDR: Power on reset / power down reset
SPI: Serial peripheral interface
SWIM: Single wire interface module
UART: Universal asynchronous receiver transmitter
Window WDG: Window watchdog

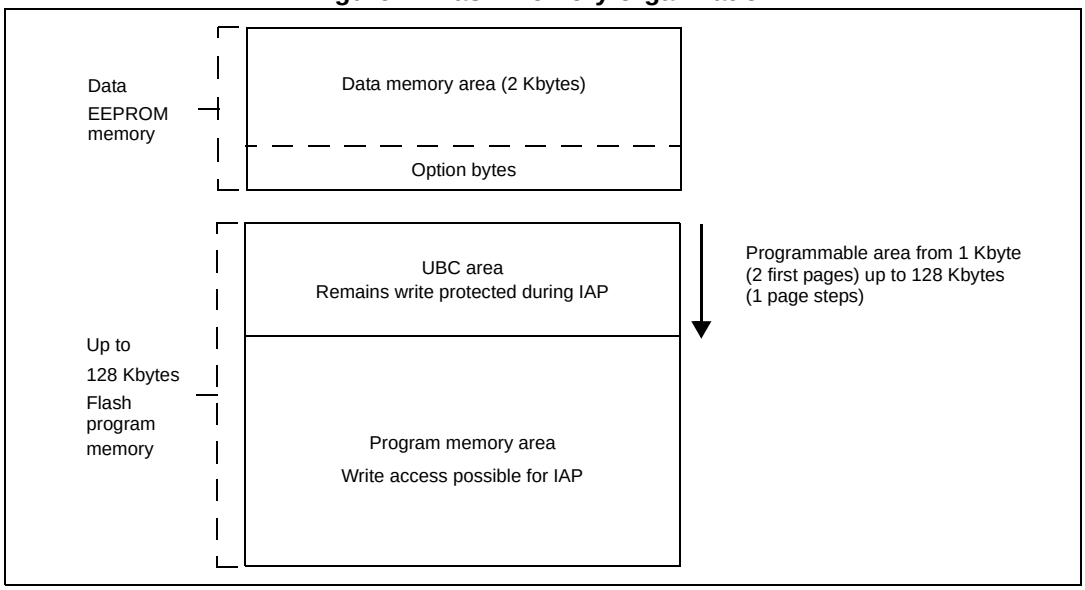
The size of the UBC is programmable through the UBC option byte (*Table 13.*), in increments of 1 page (512 bytes) by programming the UBC option byte in ICP mode.

This divides the program memory into two areas:

- Main program memory: Up to 128 Kbytes minus UBC
- User-specific boot code (UBC): Configurable up to 128 Kbytes

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

**Figure 2. Flash memory organization**




## Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

## 4.6 Power management

For efficient power management, the application can be put in one of four different low-power modes. You can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- ***Wait mode***: In this mode, the CPU is stopped, but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.
- ***Active halt mode with regulator on***: In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in active halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- ***Active halt mode with regulator off:*** This mode is the same as active halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.
- ***Halt mode***: In this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

## 4.7 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

Activation of the watchdog timers is controlled by option bytes or by software. Once activated, the watchdogs cannot be disabled by the user program without performing a reset.

### Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application perfectly.

The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout: At 16 MHz CPU clock the time-out period can be adjusted between 75 µs up to 64 ms.
2. Refresh out of window: The downcounter is refreshed before its value is lower than the one stored in the window register.

### 4.14.4 I²C

- I²C master features:
  - Clock generation
  - Start and stop generation
- I²C slave features:
  - Programmable I²C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz)
  - Fast speed (up to 400 kHz)

### 4.14.5 beCAN

The beCAN controller (basic enhanced CAN), interfaces the CAN network and supports the CAN protocol version 2.0A and B. It has been designed to manage a high number of incoming messages efficiently with a minimum CPU load.

For safety-critical applications the beCAN controller provides all hardware functions to support the CAN time triggered communication option (TTCAN).

The maximum transmission speed is 1 Mbit.

#### Transmission

- Three transmit mailboxes
- Configurable transmit priority by identifier or order request
- Time stamp on SOF transmission

#### Reception

- 8-, 11- and 29-bit ID
- One receive FIFO (3 messages deep)
- Software-efficient mailbox mapping at a unique address space
- FMI (filter match index) stored with message
- Configurable FIFO overrun
- Time stamp on SOF reception
- Six filter banks, 2 x 32 bytes (scalable to 4 x 16-bit) each, enabling various masking configurations, such as 12 filters for 29-bit ID or 48 filters for 11-bit ID
- Filtering modes:
  - Mask mode permitting ID range filtering
  - ID list mode
- Time triggered communication option
  - Disable automatic retransmission mode
  - 16-bit free running timer
  - Configurable timer resolution
  - Time stamp sent in last two data bytes

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 50CC | CLK | CLK_HSITRIMR | HSI clock calibration trimming register | 0x00 |
| 0x00 50CD | | CLK_SWIMCCR | SWIM clock control register | 0bXXXX XXX0 |
| 0x00 50CE to 0x00 50D0 | Reserved area (3 bytes) | | | |
| 0x00 50D1 | WWDG | WWDG_CR | WWDG control register | 0x7F |
| 0x00 50D2 | | WWDG_WR | WWDR window register | 0x7F |
| 0x00 50D3 to 0x00 50DF | Reserved area (13 bytes) | | | |
| 0x00 50E0 | IWDG | IWDG_KR | IWDG key register | 0xXX(2) |
| 0x00 50E1 | | IWDG_PR | IWDG prescaler register | 0x00 |
| 0x00 50E2 | | IWDG_RLR | IWDG reload register | 0xFF |
| 0x00 50E3 to 0x00 50EF | Reserved area (13 bytes) | | | |
| 0x00 50F0 | AWU | AWU_CSR1 | AWU control/status register 1 | 0x00 |
| 0x00 50F1 | | AWU_APR | AWU asynchronous prescaler buffer register | 0x3F |
| 0x00 50F2 | | AWU_TBR | AWU timebase selection register | 0x00 |
| 0x00 50F3 | BEEP | BEEP_CSR | BEEP control/status register | 0x1F |
| 0x00 50F4 to 0x00 50FF | Reserved area (12 bytes) | | | |
| 0x00 5200 | SPI | SPI_CR1 | SPI control register 1 | 0x00 |
| 0x00 5201 | | SPI_CR2 | SPI control register 2 | 0x00 |
| 0x00 5202 | | SPI_ICR | SPI interrupt control register | 0x00 |
| 0x00 5203 | | SPI_SR | SPI status register | 0x02 |
| 0x00 5204 | | SPI_DR | SPI data register | 0x00 |
| 0x00 5205 | | SPI_CRCPR | SPI CRC polynomial register | 0x07 |
| 0x00 5206 | | SPI_RXCRCR | SPI Rx CRC register | 0xFF |
| 0x00 5207 | | SPI_TXCRCR | SPI Tx CRC register | 0xFF |
| 0x00 5208 to 0x00 520F | Reserved area (8 bytes) | | | |
| 0x00 5210 | $I^2C$ | I2C_CR1 | $I^2C$ control register 1 | 0x00 |
| 0x00 5211 | | I2C_CR2 | $I^2C$ control register 2 | 0x00 |
| 0x00 5212 | | I2C_FREQR | $I^2C$ frequency register | 0x00 |
| 0x00 5213 | | I2C_OARL | $I^2C$ own address register low | 0x00 |
| 0x00 5214 | | I2C_OARH | $I^2C$ own address register high | 0x00 |
| 0x00 5215 | | Reserved | | |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5216 | I²C | I2C_DR | I²C data register | 0x00 |
| 0x00 5217 | | I2C_SR1 | I²C status register 1 | 0x00 |
| 0x00 5218 | | I2C_SR2 | I²C status register 2 | 0x00 |
| 0x00 5219 | | I2C_SR3 | I²C status register 3 | 0x00 |
| 0x00 521A | | I2C_ITR | I²C interrupt control register | 0x00 |
| 0x00 521B | | I2C_CCRL | I²C clock control register low | 0x00 |
| 0x00 521C | | I2C_CCRH | I²C clock control register high | 0x00 |
| 0x00 521D | | I2C_TRISER | I²C TRISE register | 0x02 |
| 0x00 521E to 0x00 522F | Reserved area (18 bytes) | | | |
| 0x00 5230 | UART1 | UART1_SR | UART1 status register | 0xC0 |
| 0x00 5231 | | UART1_DR | UART1 data register | 0xXX |
| 0x00 5232 | | UART1_BRR1 | UART1 baud rate register 1 | 0x00 |
| 0x00 5233 | | UART1_BRR2 | UART1 baud rate register 2 | 0x00 |
| 0x00 5234 | | UART1_CR1 | UART1 control register 1 | 0x00 |
| 0x00 5235 | | UART1_CR2 | UART1 control register 2 | 0x00 |
| 0x00 5236 | | UART1_CR3 | UART1 control register 3 | 0x00 |
| 0x00 5237 | | UART1_CR4 | UART1 control register 4 | 0x00 |
| 0x00 5238 | | UART1_CR5 | UART1 control register 5 | 0x00 |
| 0x00 5239 | | UART1_GTR | UART1 guard time register | 0x00 |
| 0x00 523A | | UART1_PSCR | UART1 prescaler register | 0x00 |
| 0x00 523B to 0x00 523F | Reserved area (5 bytes) | | | |
| 0x00 5240 | UART3 | UART3_SR | UART3 status register | C0h |
| 0x00 5241 | | UART3_DR | UART3 data register | 0xXX |
| 0x00 5242 | | UART3_BRR1 | UART3 baud rate register 1 | 0x00 |
| 0x00 5243 | | UART3_BRR2 | UART3 baud rate register 2 | 0x00 |
| 0x00 5244 | | UART3_CR1 | UART3 control register 1 | 0x00 |
| 0x00 5245 | | UART3_CR2 | UART3 control register 2 | 0x00 |
| 0x00 5246 | | UART3_CR3 | UART3 control register 3 | 0x00 |
| 0x00 5247 | | UART3_CR4 | UART3 control register 4 | 0x00 |
| 0x00 5248 | | Reserved | | |
| 0x00 5249 | | UART3_CR6 | UART3 control register 6 | 0x00 |
| 0x00 524A to 0x00 524F | Reserved area (6 bytes) | | | |

### Total current consumption in active halt mode

**Table 24. Total current consumption in active halt mode at $V_{DD}$ = 5 V, $T_A$ -40 to 85° C**

| Symbol | Parameter | Conditions | | | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|---|
| | | Main voltage regulator (MVR)(2) | Flash mode(3) | Clock source | | | |
| $I_{DD(AH)}$ | Supply current in active halt mode | On | Operating mode | HSE crystal oscillator (16 MHz) | 1000 | | µA |
| | | | | LSI RC oscillator (128 kHz) | 200 | 260 | |
| | | | Power-down mode | HSE crystal oscillator (16 MHz) | 940 | | |
| | | | | LSI RC oscillator (128 kHz) | 140 | | |
| | | Off | Operating mode | LSI RC oscillator 128 kHz) | 68 | | |
| | | | Power-down mode | | 11 | 45 | |

1. Data based on characterization results, not tested in production.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

**Table 25. Total current consumption in active halt mode at $V_{DD}$ = 3.3 V**

| Symbol | Parameter | Conditions | | | Typ(1) | Unit |
|---|---|---|---|---|---|---|
| | | Main voltage regulator (MVR)(2) | Flash mode(3) | Clock source | | |
| $I_{DD(AH)}$ | Supply current in active halt mode | On | Operating mode | HSE crystal osc. (16 MHz) | 600 | µA |
| | | | | LSI RC osc. (128 kHz) | 200 | |
| | | | Power-down mode | HSE crystal osc. (16 MHz) | 540 | |
| | | | | LSI RC osc. (128 kHz) | 140 | |
| | | Off | Operating mode | LSI RC osc. (128 kHz) | 66 | |
| | | | Power-down mode | | 9 | |

1. Data based on characterization results, not tested in production.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

**Figure 27. Typ. $V_{OL}$ @ $V_{DD}$ = 5 V (high sink ports)**

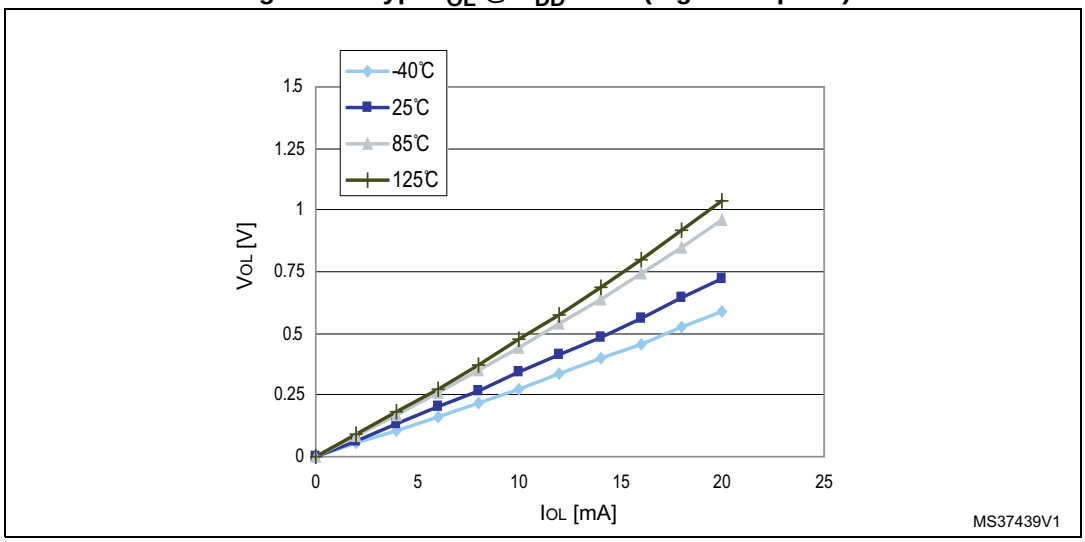



**Figure 28. Typ. $V_{OL}$ @ $V_{DD}$ = 3.3 V (high sink ports)**

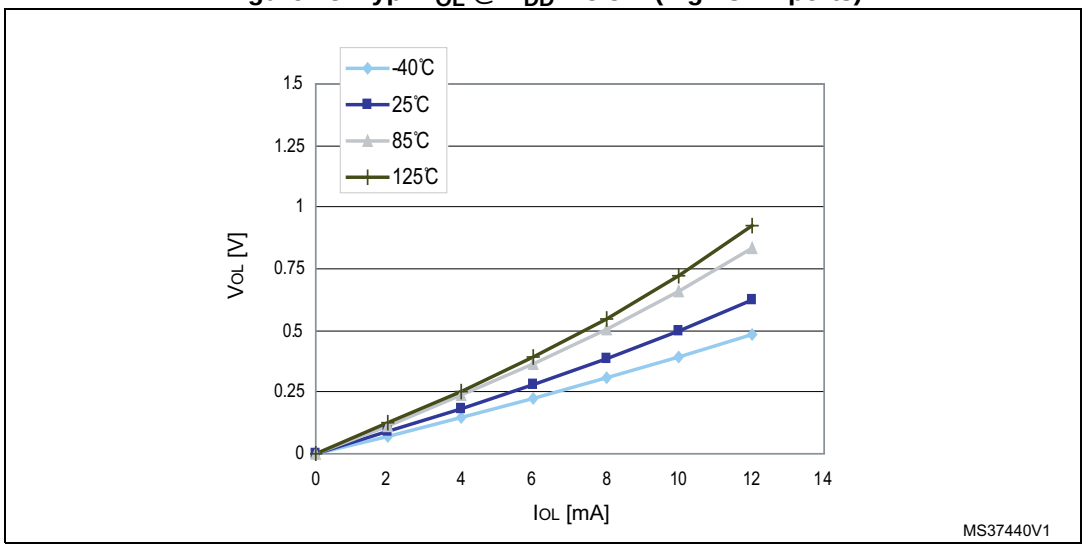


**Figure 31. Typ. $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 5 V (high sink ports)**

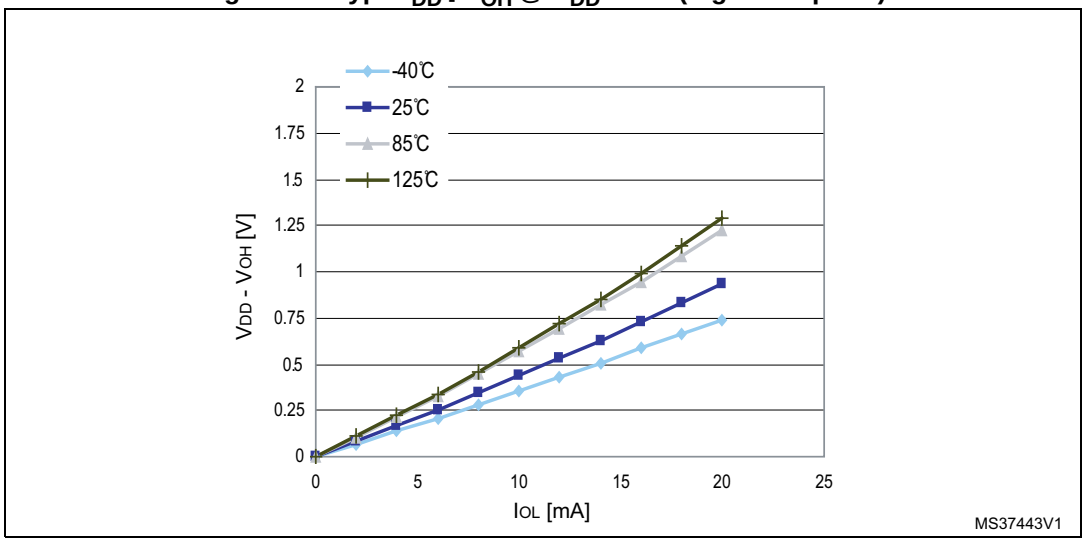



**Figure 32. Typ. $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 3.3 V (high sink ports)**

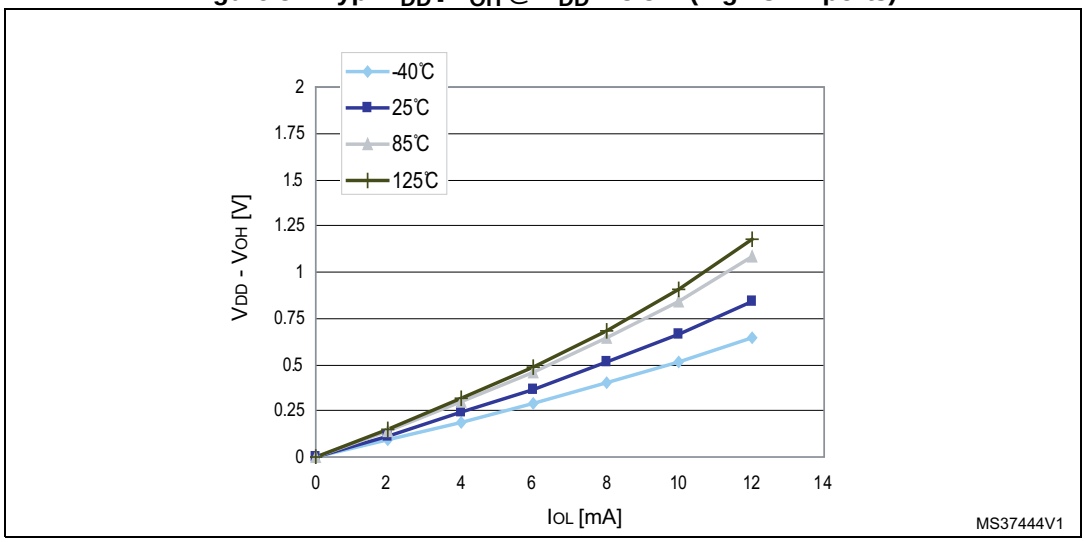
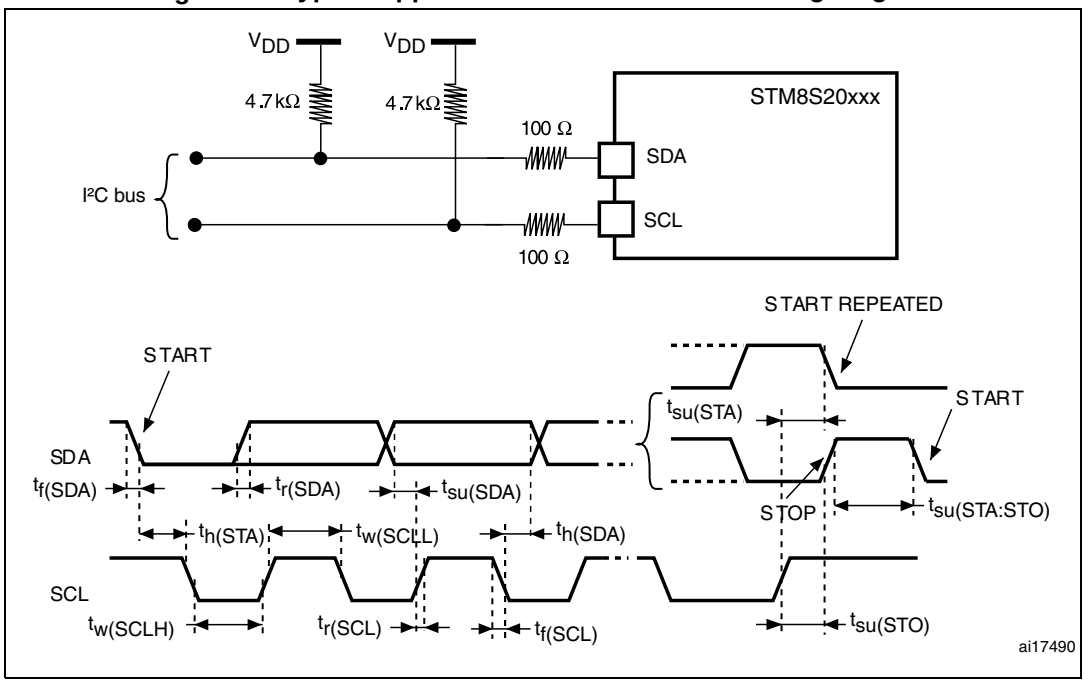


**Figure 40. Typical application with I²C bus and timing diagram**




1. Measurement points are made at CMOS levels: 0.3 x $V_{DD}$ and 0.7 x $V_{DD}$

### Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance:

- A supply overvoltage (applied to each power supply pin)
- A current injection (applied to each input, output and configurable I/O pin) is performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

**Table 50. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class(1) |
|---|---|---|---|
| LU | Static latch-up class | $T_A = 25$ °C | A |
| | | $T_A = 85$ °C | A |
| | | $T_A = 125$ °C | A |

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

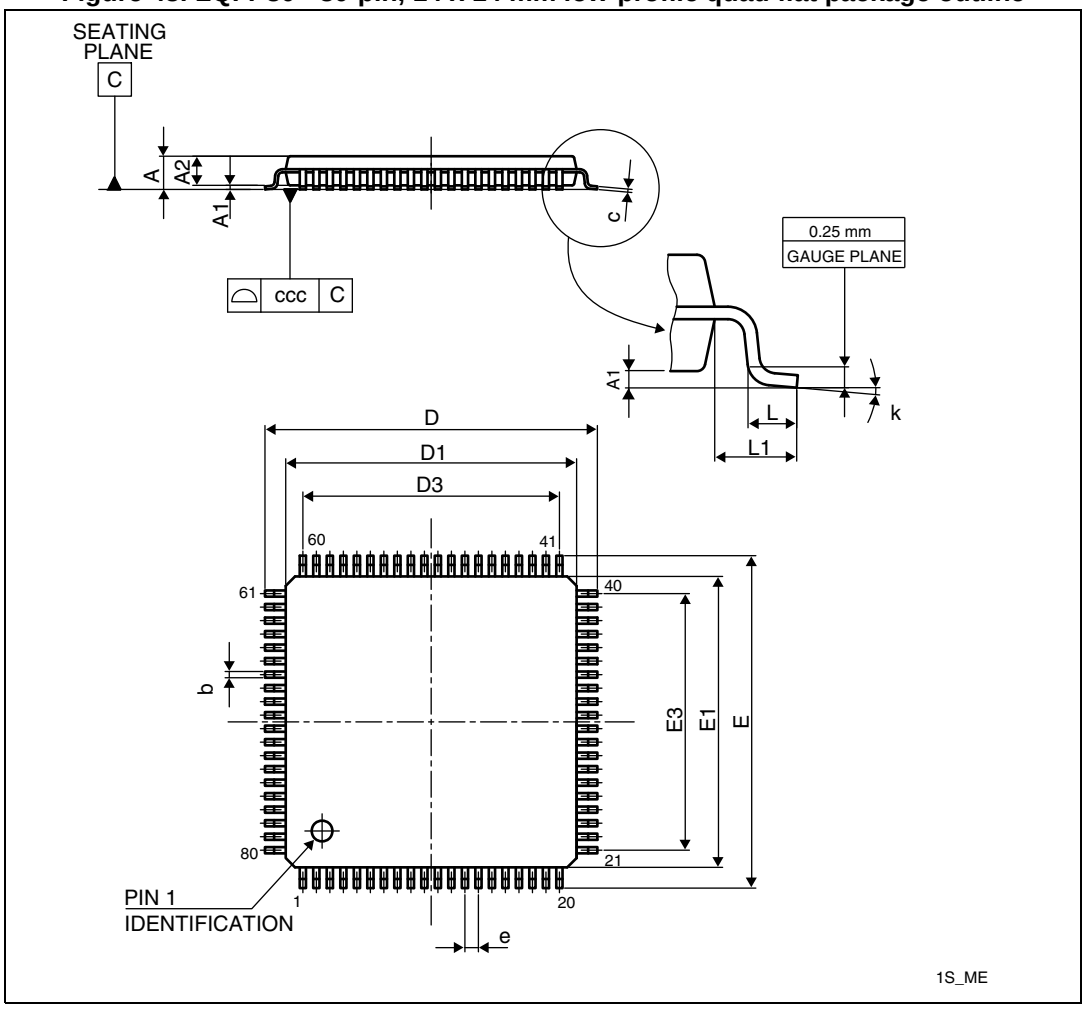
# 11 Package characteristics

To meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at *www.st.com*. ECOPACK® is an ST trademark.

# 11.1 Package information

## 11.1.1 LQFP80 package information

**Figure 43. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package outline**




1. Drawing is not to scale.

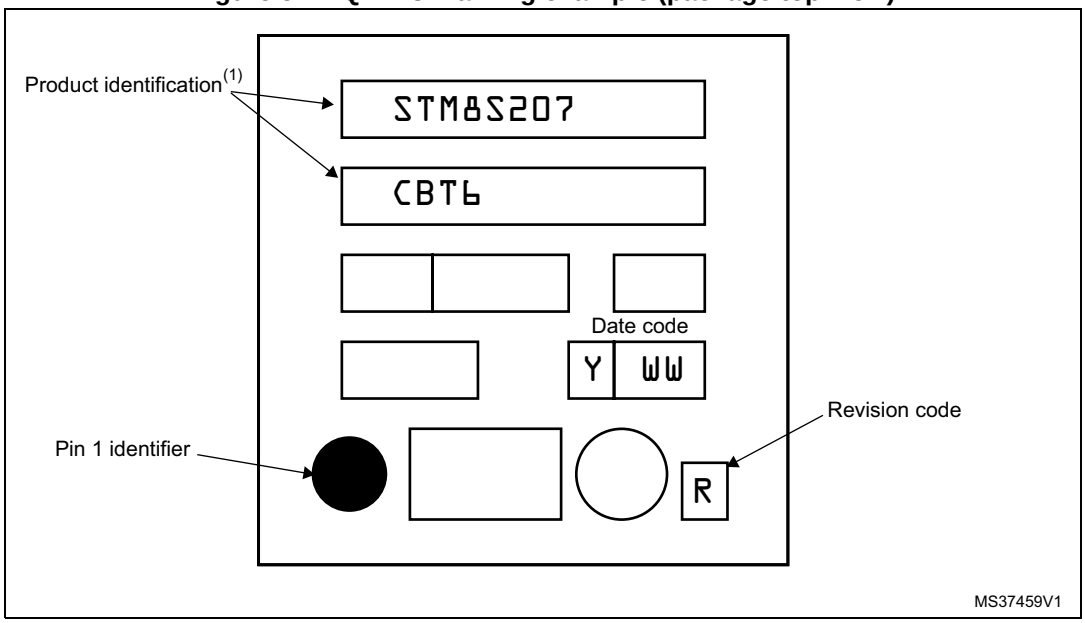
**Table 51. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package mechanical data(1)**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.220 | 0.320 | 0.380 | 0.0087 | 0.0126 | 0.0150 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |

### Device marking

The following figure shows the marking for the LQFP48 package.

**Figure 52. LQFP48 marking example (package top view)**




1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

### 11.1.4 LQFP44 package information

**Figure 53. LQFP44 - 44-pin, 10 x 10 mm low-profile quad flat package outline**