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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	1.5K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s207c8t3tr

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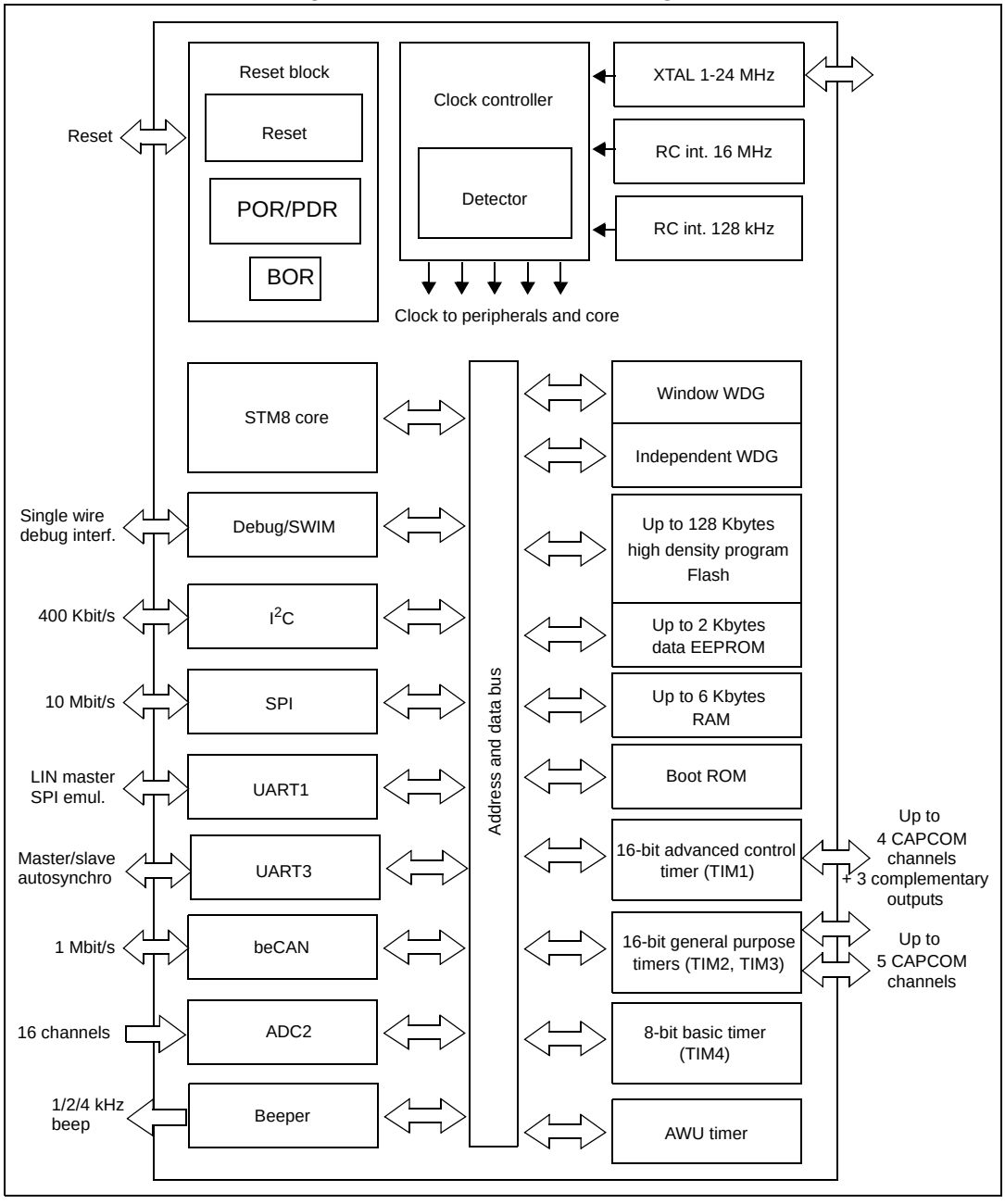
1 Introduction

This datasheet contains the description of the STM8S20xxx features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8S microcontroller memory, registers and peripherals, please refer to the STM8S microcontroller family reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8S Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

3 Block diagram

Figure 1. STM8S20xxx block diagram



1. Legend:
ADC: Analog-to-digital converter
beCAN: Controller area network
BOR: Brownout reset
I²C: Inter-integrated circuit multimaster interface
Independent WDG: Independent watchdog
POR/PDR: Power on reset / power down reset
SPI: Serial peripheral interface
SWIM: Single wire interface module
UART: Universal asynchronous receiver transmitter
Window WDG: Window watchdog

4.14.1 UART1

Main features

- One Mbit/s full duplex SCI
- SPI emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- LIN master mode
- Single wire half duplex mode

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Maximum speed: 1 Mbit/s at 16 MHz (f_{CPU}/16)

LIN master mode

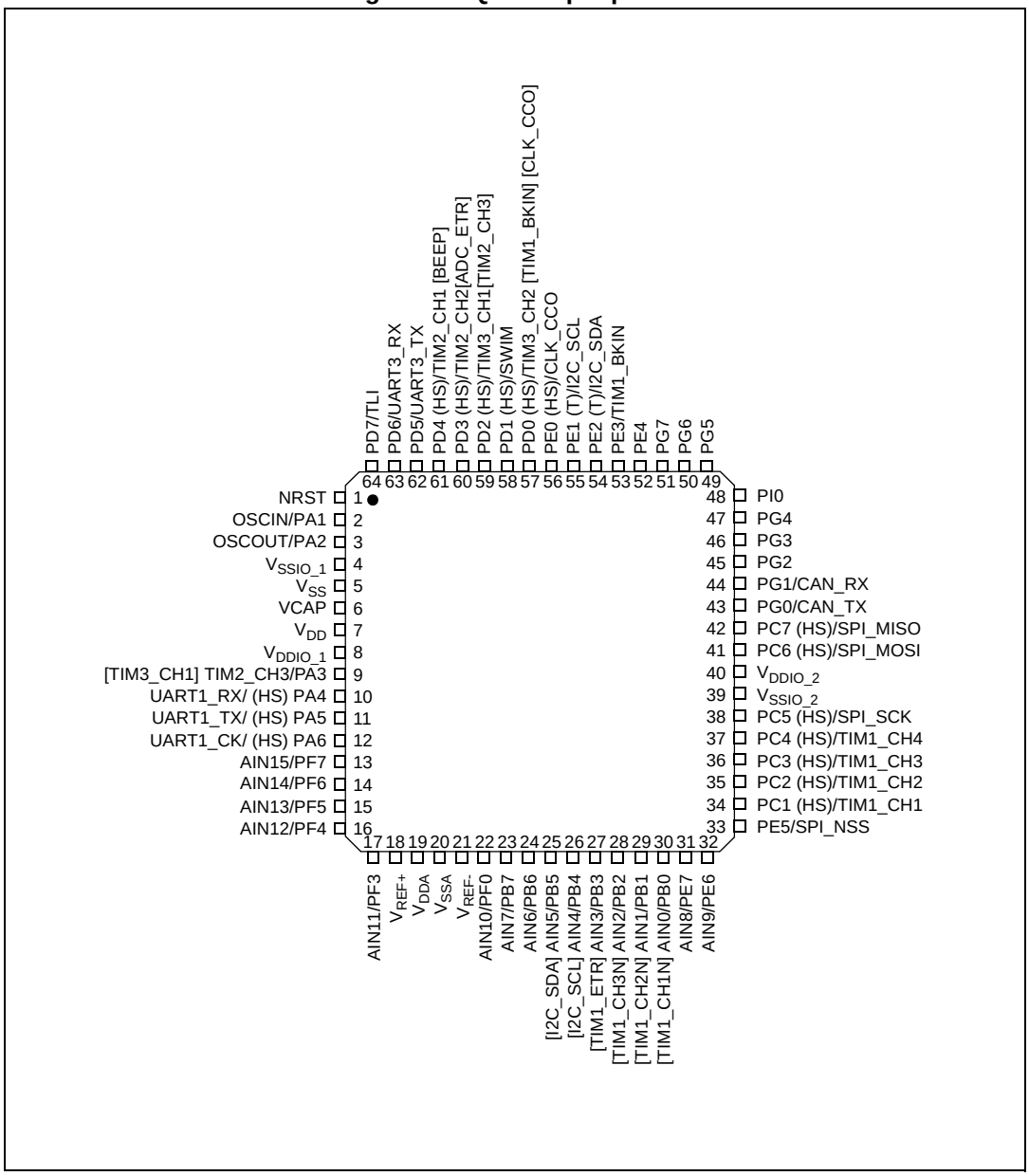
- Emission: Generates 13-bit sync break frame
- Reception: Detects 11-bit break frame

4.14.2 UART3

Main features

- 1 Mbit/s full duplex SCI
- LIN master capable
- High precision baud rate generator

Figure 4. LQFP 64-pin pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
4. CAN_RX and CAN_TX is available on STM8S208xx devices only.

Table 6. Pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	LQFP44	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
12	12	12	11	-	PA6/UART1_CK	I/O	**X**	X	X	HS	O3	X	X	**Port A6**	UART1 synchronous clock	
13	-	-	-	-	PH0	I/O	**X**	X		HS	O3	X	X	**Port H0**		
14	-	-	-	-	PH1	I/O	**X**	X		HS	O3	X	X	**Port H1**		
15	-	-	-	-	PH2	I/O	**X**	X			O1	X	X	**Port H2**		
16	-	-	-	-	PH3	I/O	**X**	X			O1	X	X	**Port H3**		
17	13	-	-	-	PF7/AIN15	I/O	**X**	X			O1	X	X	**Port F7**	Analog input 15	
18	14	-	-	-	PF6/AIN14	I/O	**X**	X			O1	X	X	**Port F6**	Analog input 14	
19	15	-	-	-	PF5/AIN13	I/O	**X**	X			O1	X	X	**Port F5**	Analog input 13	
20	16	-	-	8	PF4/AIN12	I/O	**X**	X			O1	X	X	**Port F4**	Analog input 12	
21	17	-	-	-	PF3/AIN11	I/O	**X**	X			O1	X	X	**Port F3**	Analog input 11	
22	18	-	-	-	V_{REF+}	S								ADC positive reference voltage		
23	19	13	12	9	V_{DDA}	S								Analog power supply		
24	20	14	13	10	V_{SSA}	S								Analog ground		
25	21	-	-	-	V_{REF-}	S								ADC negative reference voltage		
26	22	-	-	-	PF0/AIN10	I/O	**X**	X			O1	X	X	**Port F0**	Analog input 10	
27	23	15	14	-	PB7/AIN7	I/O	**X**	X	X		O1	X	X	**Port B7**	Analog input 7	
28	24	16	15	-	PB6/AIN6	I/O	**X**	X	X		O1	X	X	**Port B6**	Analog input 6	
29	25	17	16	11	PB5/AIN5	I/O	**X**	X	X		O1	X	X	**Port B5**	Analog input 5	I^2C_SDA [AFR6]
30	26	18	17	12	PB4/AIN4	I/O	**X**	X	X		O1	X	X	**Port B4**	Analog input 4	I^2C_SCL [AFR6]

6 Memory and register map

6.1 Memory map

Figure 8. Memory map

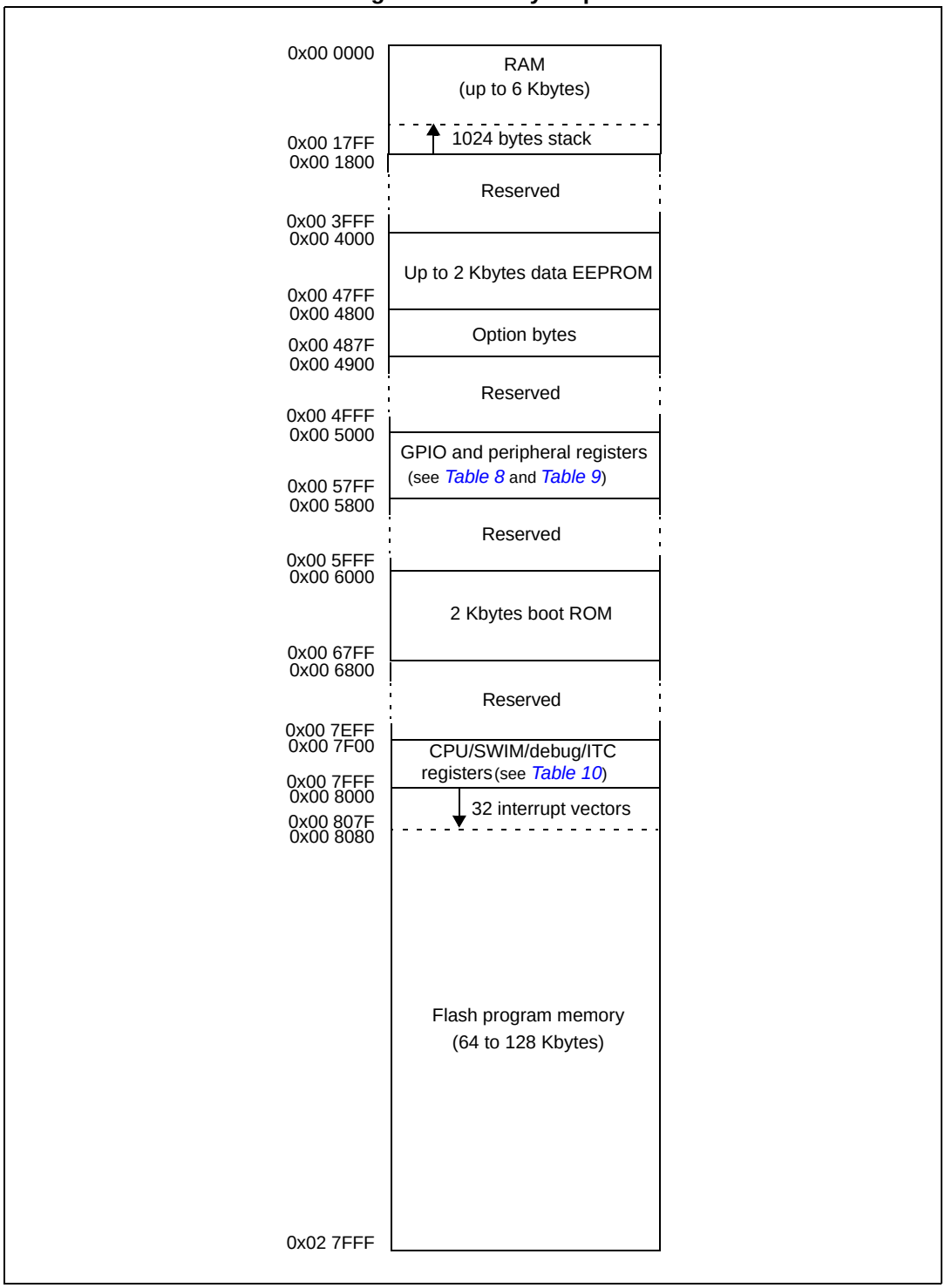


Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 532B	TIM3	TIM3_ARRH	TIM3 auto-reload register high	0xFF
0x00 532C		TIM3_ARRL	TIM3 auto-reload register low	0xFF
0x00 532D		TIM3_CCR1H	TIM3 capture/compare register 1 high	0x00
0x00 532E		TIM3_CCR1L	TIM3 capture/compare register 1 low	0x00
0x00 532F		TIM3_CCR2H	TIM3 capture/compare register 2 high	0x00
0x00 5330		TIM3_CCR2L	TIM3 capture/compare register 2 low	0x00
0x00 5331 to 0x00 533F	Reserved area (15 bytes)			
0x00 5340	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 5341		TIM4_IER	TIM4 interrupt enable register	0x00
0x00 5342		TIM4_SR	TIM4 status register	0x00
0x00 5343		TIM4_EGR	TIM4 event generation register	0x00
0x00 5344		TIM4_CNTR	TIM4 counter	0x00
0x00 5345		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 5346		TIM4_ARR	TIM4 auto-reload register	0xFF
0x00 5347 to 0x00 53FF	Reserved area (185 bytes)			
0x00 5400	ADC2	ADC _CSR	ADC control/status register	0x00
0x00 5401		ADC_CR1	ADC configuration register 1	0x00
0x00 5402		ADC_CR2	ADC configuration register 2	0x00
0x00 5403		ADC_CR3	ADC configuration register 3	0x00
0x00 5404		ADC_DRH	ADC data register high	0xXX
0x00 5405		ADC_DRL	ADC data register low	0xXX
0x00 5406		ADC_TDRH	ADC Schmitt trigger disable register high	0x00
0x00 5407		ADC_TDRL	ADC Schmitt trigger disable register low	0x00
0x00 5408 to 0x00 541F	Reserved area (24 bytes)			
0x00 5420	beCAN	CAN_MCR	CAN master control register	0x02
0x00 5421		CAN_MSR	CAN master status register	0x02
0x00 5422		CAN_TSR	CAN transmit status register	0x00
0x00 5423		CAN_TPR	CAN transmit priority register	0x0C
0x00 5424		CAN_RFR	CAN receive FIFO register	0x00
0x00 5425		CAN_IER	CAN interrupt enable register	0x00
0x00 5426		CAN_DGR	CAN diagnosis register	0x0C
0x00 5427		CAN_FPSR	CAN page selection register	0x00

Total current consumption in active halt mode

Table 24. Total current consumption in active halt mode at V_{DD} = 5 V, T_A -40 to 85° C

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source			
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal oscillator (16 MHz)	1000		µA
				LSI RC oscillator (128 kHz)	200	260	
			Power-down mode	HSE crystal oscillator (16 MHz)	940		
				LSI RC oscillator (128 kHz)	140		
		Off	Operating mode	LSI RC oscillator 128 kHz)	68		
			Power-down mode		11	45	

1. Data based on characterization results, not tested in production.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Table 25. Total current consumption in active halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions			Typ(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source		
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	600	µA
				LSI RC osc. (128 kHz)	200	
			Power-down mode	HSE crystal osc. (16 MHz)	540	
				LSI RC osc. (128 kHz)	140	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	
			Power-down mode		9	

1. Data based on characterization results, not tested in production.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Total current consumption in halt mode

Table 26. Total current consumption in halt mode at V_{DD} = 5 V

Symbol	Parameter	Conditions	Typ	Max at 85 °C	Max at 125 °C	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	63.5			µA
		Flash in power-down mode, HSI clock after wakeup	6.5	35	100	

Table 27. Total current consumption in halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions	Typ	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	61.5	µA
		Flash in power-down mode, HSI clock after wakeup	4.5	

Low power mode wakeup times

Table 28. Wakeup times

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
$t_{WU(WFI)}$	Wakeup time from wait mode to run mode(3)					See note(2)	µs
		$f_{CPU} = f_{MASTER}$ = 16 MHz.			0.56		
$t_{WU(AH)}$	Wakeup time active halt mode to run mode.(3)	MVR voltage regulator on(4)	Flash in operating mode(5)	HSI (after wakeup)	1(6)	2(6)	
			Flash in power-down mode(5)		3(6)		
		MVR voltage regulator off(4)	Flash in operating mode(5)		48(6)		
			Flash in power-down mode(5)		50(6)		
$t_{WU(H)}$	Wakeup time from halt mode to run mode(3)	Flash in operating mode(5)			52		
		Flash in power-down mode(5)			54		

1. Data guaranteed by design, not tested in production.
2. $t_{WU(WFI)} = 2 \times 1/f_{master} + 7 \times 1/f_{CPU}$
3. Measured from interrupt event to interrupt vector fetch.
4. Configured by the REGAH bit in the CLK_ICKR register.
5. Configured by the AHALT bit in the FLASH_CR1 register.
6. Plus 1 LSI clock depending on synchronization.

Current consumption curves

Figure 14 and *Figure 15* show typical current consumption measured with code executing in RAM.

Figure 14. Typ. $I_{DD(RUN)}$ vs V_{DD}, HSI RC osc, f_{CPU} = 16 MHz

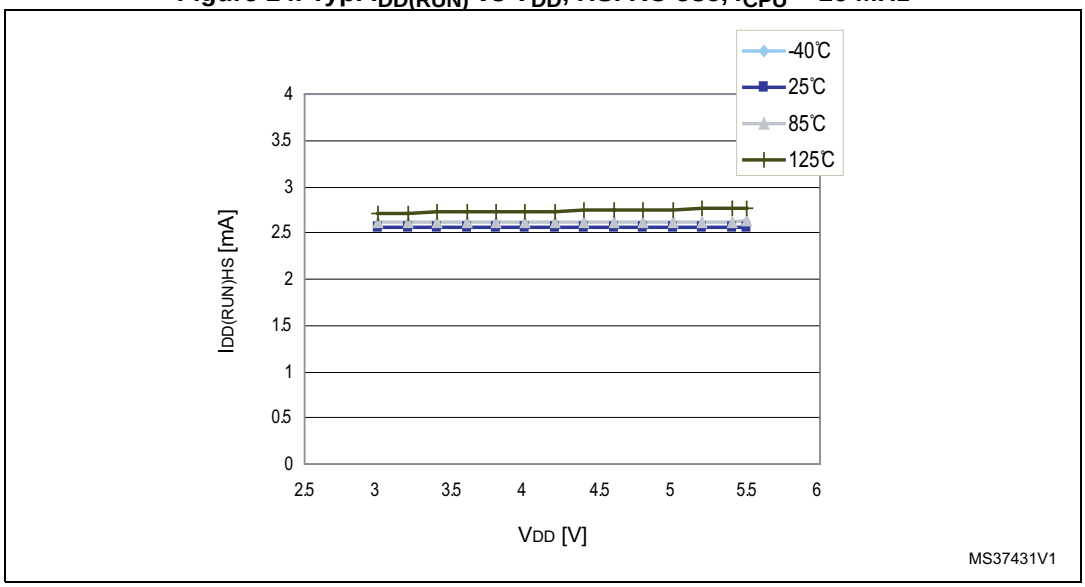


Figure 15. Typ. $I_{DD(WFI)}$ vs V_{DD}, HSI RC osc, f_{CPU} = 16 MHz

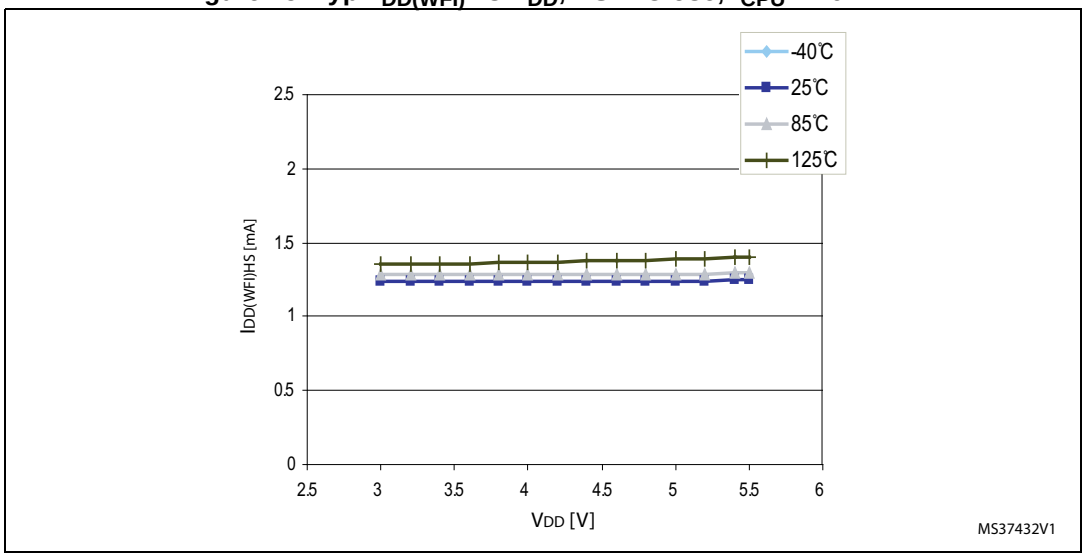
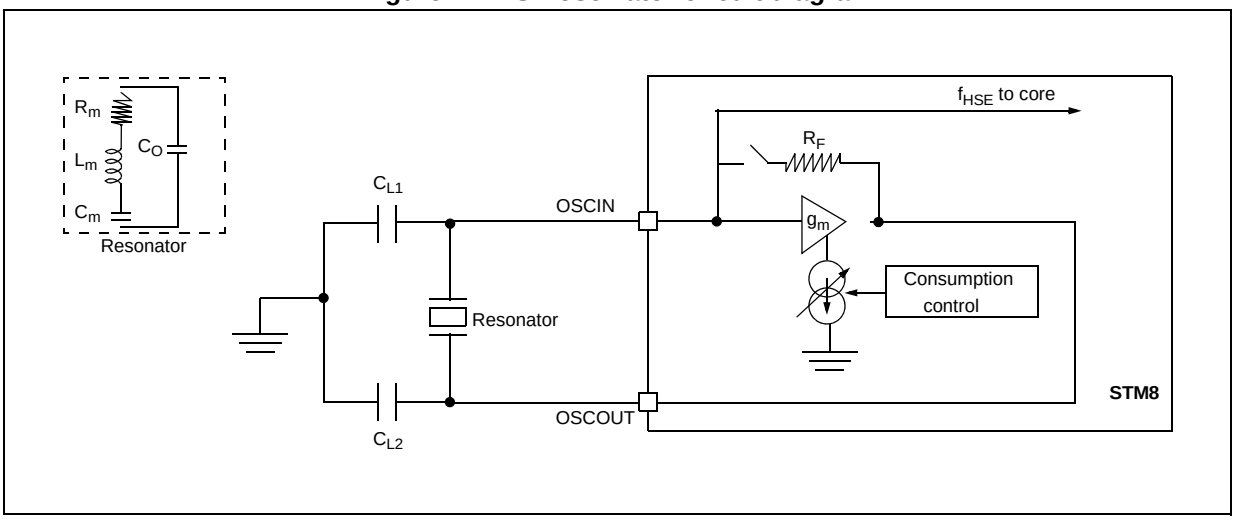


Table 32. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	External high speed oscillator frequency		1		24	MHz
R_F	Feedback resistor			220		kΩ
$C^{(1)}$	Recommended load capacitance (2)				20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 24 MHz			6 (startup) 2 (stabilized)(3)	mA
		C = 10 pF, f_{OSC} = 24 MHz			6 (startup) 1.5 (stabilized)(3)	
g_m	Oscillator transconductance		5			mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized		1		ms

1. C is approximately equivalent to 2 x crystal Cload.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Data based on characterization results, not tested in production.
4. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 24 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 17. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Notional resistance (see crystal specification)
L_m: Notional inductance (see crystal specification)
C_m: Notional capacitance (see crystal specification)
Co: Shunt capacitance (see crystal specification)
C_{L1}=C_{L2}=C: Grounded external capacitance
$g_m >> g_{mcrit}$

Figure 34. Typical NRST pull-up resistance vs V_{DD} @ 4 temperatures

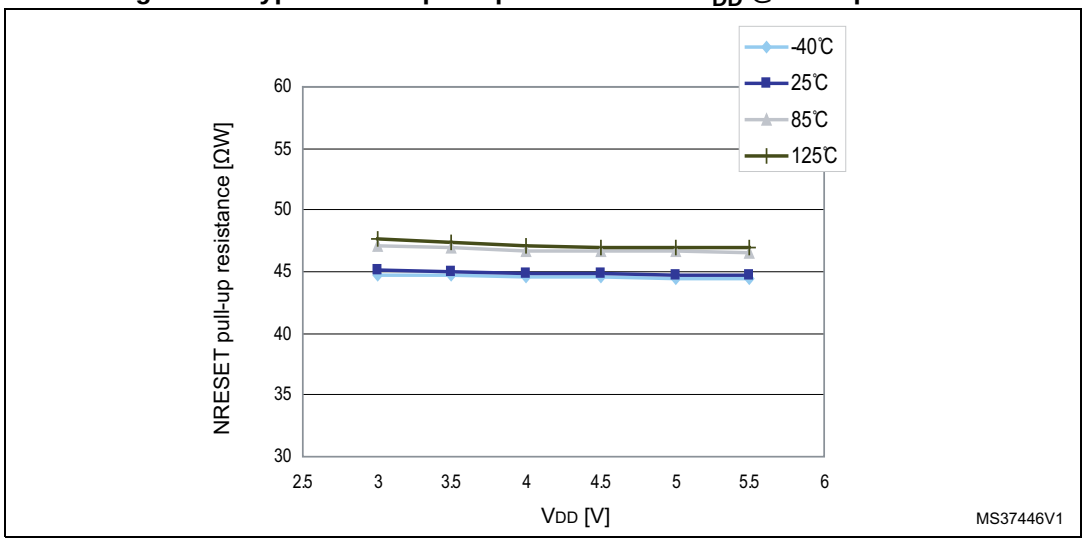
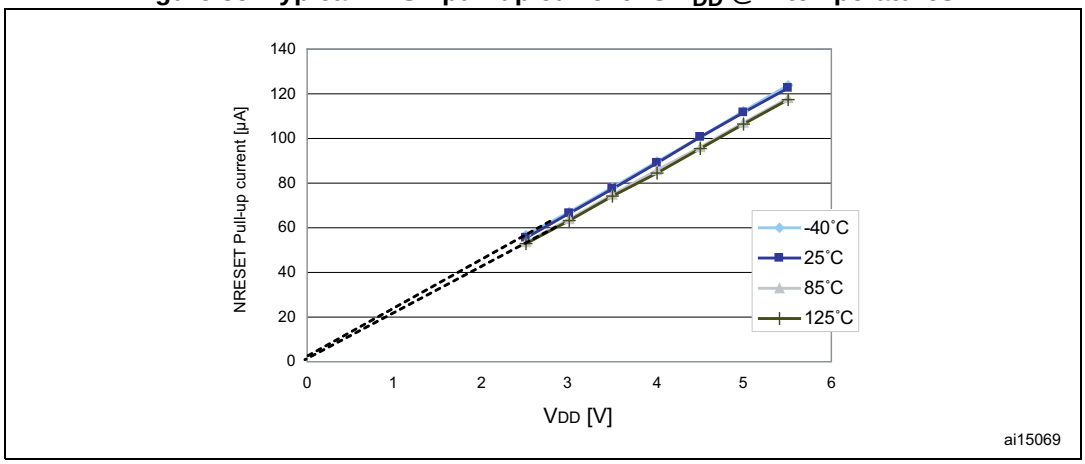
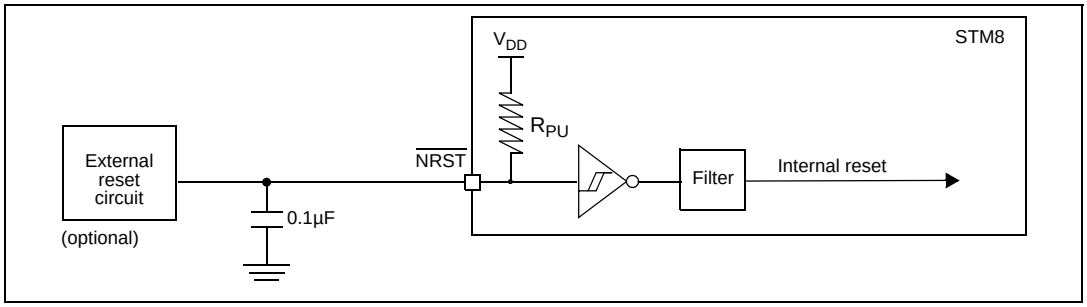


Figure 35. Typical NRST pull-up current vs V_{DD} @ 4 temperatures



The reset network shown in *Figure 36* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in *Table 41*. Otherwise the reset is not taken into account internally. For power consumption sensitive applications, the capacity of the external reset capacitor can be reduced to limit charge/discharge current. If the NRSTsignal is used to reset the external circuitry, care must be taken of the charge/discharge time of the external capacitor to fulfill the external device's reset timing conditions. The minimum recommended capacity is 10 nF.

Figure 36. Recommended reset pin protection



10.3.8 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 42* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 42. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	10	MHz
		Slave mode	0	6	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		25	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	4 x t_{MASTER}		
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	70		
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode	$t_{SCK}/2$ - 15	$t_{SCK}/2$ + 15	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5		
		Slave mode	5		
$t_{h(MI)}$ (1) $t_{h(SI)}$ (1)	Data input hold time	Master mode	7		
		Slave mode	10		
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode		3 x t_{MASTER}	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	25		
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)		75	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)		30	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	31		
$t_{h(MO)}$ (1)		Master mode (after enable edge)	12		

1. Values based on design simulation and/or characterization results, and not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Table 45. ADC accuracy with R_{AIN} < 10 kΩ , V_{DDA} = 5 V

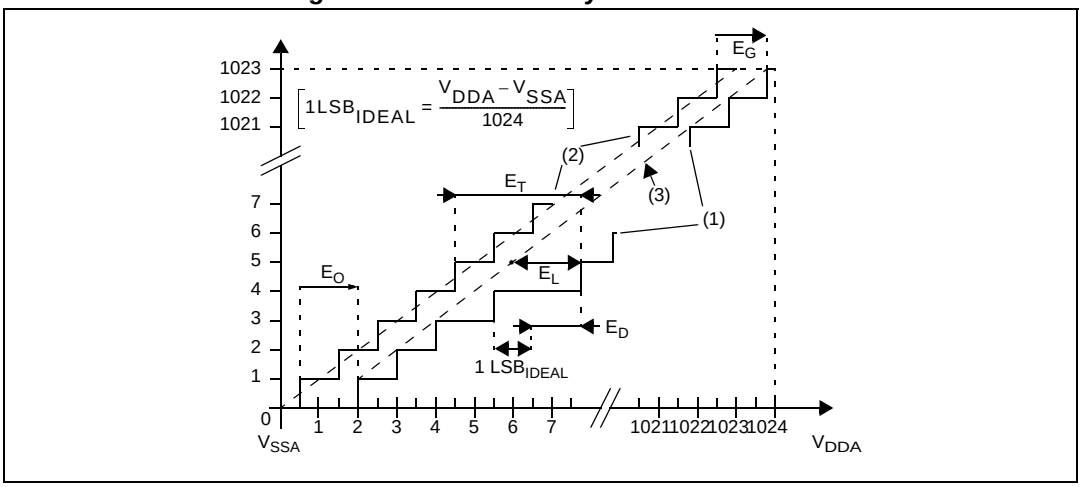
Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error (2)	f_{ADC} = 2 MHz	1	2.5	LSB
		f_{ADC} = 4 MHz	1.4	3	
		f_{ADC} = 6 MHz	1.6	3.5	
$\|E_O\|$	Offset error (2)	f_{ADC} = 2 MHz	0.6	2	
		f_{ADC} = 4 MHz	1.1	2.5	
		f_{ADC} = 6 MHz	1.2	2.5	
$\|E_G\|$	Gain error (2)	f_{ADC} = 2 MHz	0.2	2	
		f_{ADC} = 4 MHz	0.6	2.5	
		f_{ADC} = 6 MHz	0.8	2.5	
$\|E_D\|$	Differential linearity error (2)	f_{ADC} = 2 MHz	0.7	1.5	
		f_{ADC} = 4 MHz	0.7	1.5	
		f_{ADC} = 6 MHz	0.8	1.5	
$\|E_L\|$	Integral linearity error (2)	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.6	1.5	
		f_{ADC} = 6 MHz	0.6	1.5	

1. Data based on characterization results for LQFP80 device with V_{REF+}/V_{REF-}, not tested in production.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 10.3.6* does not affect the ADC accuracy.

Table 46. ADC accuracy with R_{AIN} < 10 kΩ R_{AIN}, V_{DDA} = 3.3 V

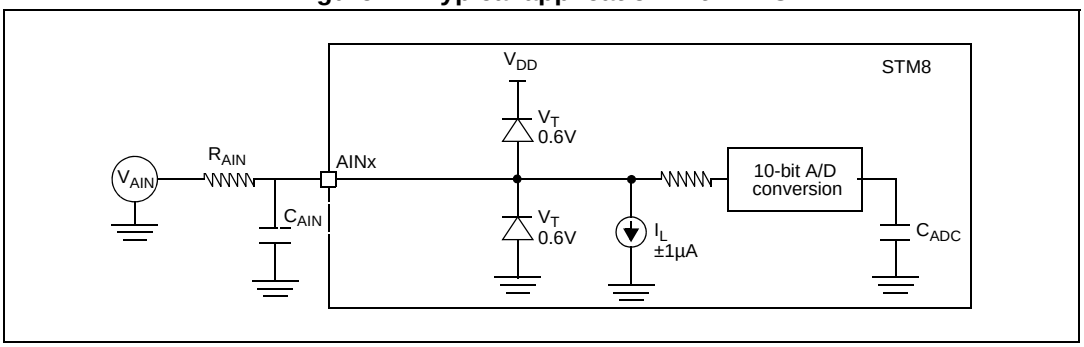
Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 2 MHz	1.1	2	LSB
		f_{ADC} = 4 MHz	1.6	2.5	
$\|E_O\|$	Offset error(2)	f_{ADC} = 2 MHz	0.7	1.5	
		f_{ADC} = 4 MHz	1.3	2	
$\|E_G\|$	Gain error(2)	f_{ADC} = 2 MHz	0.2	1.5	
		f_{ADC} = 4 MHz	0.5	2	
$\|E_D\|$	Differential linearity error(2)	f_{ADC} = 2 MHz	0.7	1	
		f_{ADC} = 4 MHz	0.7	1	
$\|E_L\|$	Integral linearity error(2)	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.6	1.5	

Figure 41. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. The ideal transfer curve
3. End point correlation line
   E_T = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset error: deviation between the first actual transition and the first ideal one.
   E_G = Gain error: deviation between the last ideal transition and the last actual one.
   E_D = Differential linearity error: maximum deviation between actual steps and the ideal one.
   E_L = Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

Figure 42. Typical application with ADC



10.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

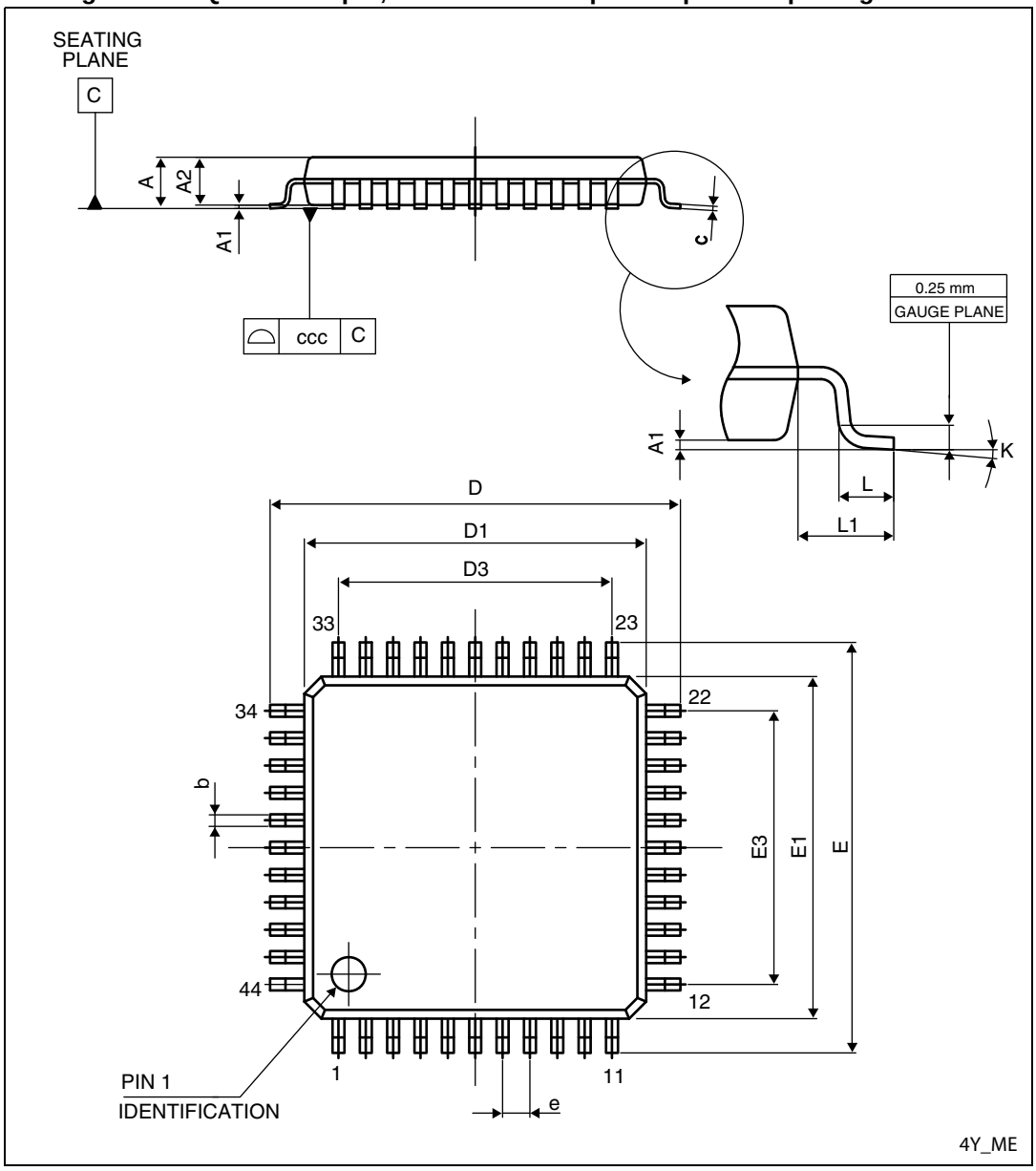
To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 47. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 5 V, T_A = 25 °C, f_{MASTER} = 16 MHz, conforming to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 5 V, T_A = 25 °C, f_{MASTER} = 16 MHz, conforming to IEC 61000-4-4	4A

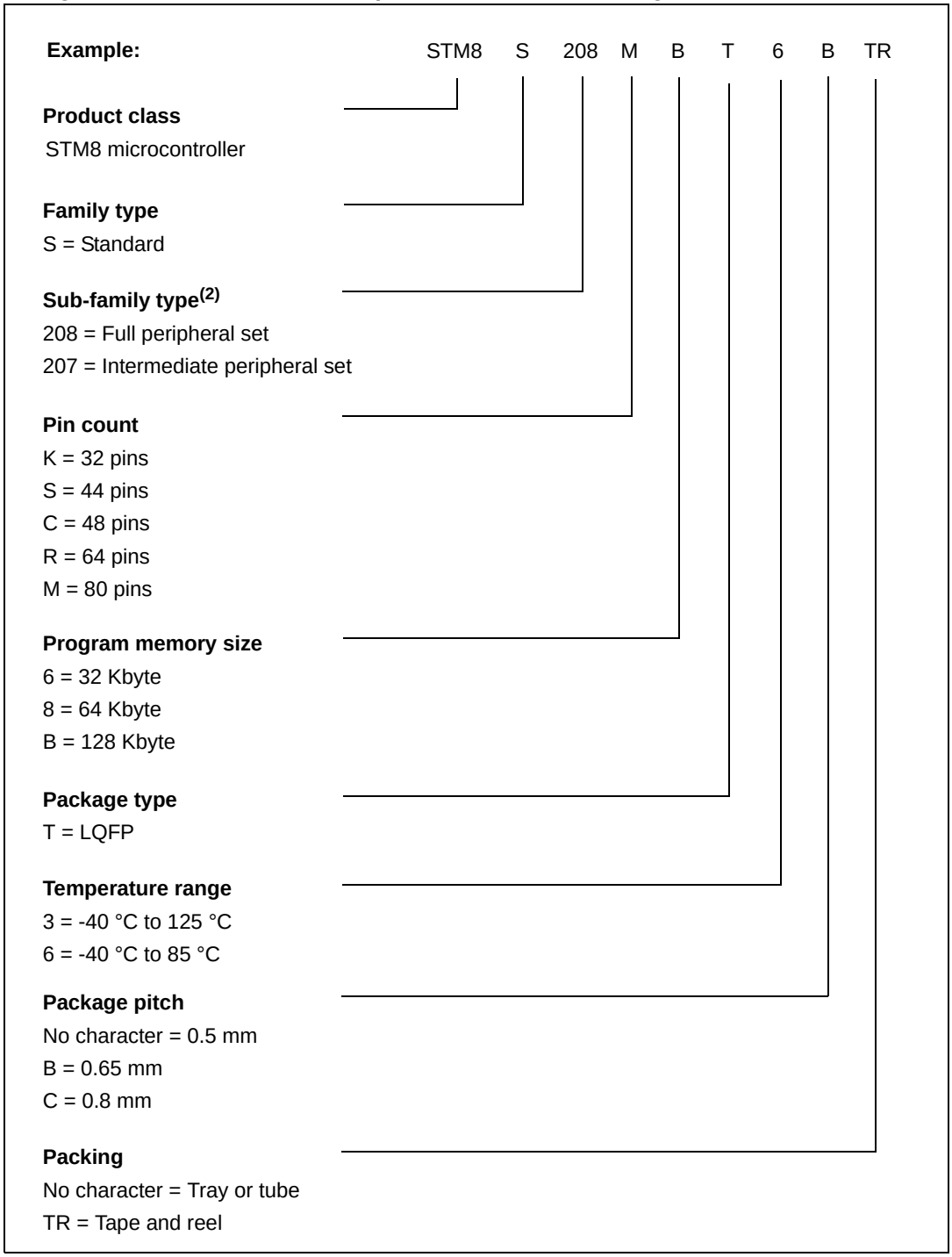
11.1.4 LQFP44 package information

Figure 53. LQFP44 - 44-pin, 10 x 10 mm low-profile quad flat package outline



13 Ordering information

Figure 59. STM8S207xx/208xx performance line ordering information scheme(1)



1. For a list of available options (e.g. memory size, package) and order-able part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the ST Sales Office nearest to you.
2. Refer to *Table 2: STM8S20xxx performance line features* for detailed description.

Table 58. Document revision history (continued)

Date	Revision	Changes
14-Sep-2010	10	Added part number STM8S208M8 to *Table 1: Device summary*. Updated “reset state” of *Table 5: Legend/abbreviations for pinout table*. Added footnote *4* to *Table 6: Pin description*. *Table 9: General hardware register map*: standardized all reset state values; updated the reset state values of RST_SR, CLK_SWCR, CLK_HSITRIMR, CLK_SWIMCCR, IWDG_KR, and ADC_DRx registers; added the reset values of the CAN paged registers. *Figure 36: Recommended reset pin protection*: replaced 0.01 µF with 0.1 µF. *Figure 40: Typical application with I2C bus and timing diagram*: $t_{w(SCKH)}$, $t_{w(SCKL)}$, $t_{r(SCK)}$, and $t_{f(SCK)}$ replaced by $t_{w(SCLH)}$, $t_{w(SCLL)}$, $t_{r(SCL)}$, and $t_{f(SCL)}$ respectively.
22-Mar-2011	11	*Table 1: Device summary*: added STM8S207K8. *Table 2: STM8S20xxx performance line features*: added STM8S207K8 device and changed the RAM value of all other devices to 6 Kbytes. *Figure 5*, *Figure 4*, *Figure 5*, and *Figure 7*: removed TIM1_CH4 from pins 80, 64, 48, and 32 respectively. *Table 6: Pin description*: updated note *3* and added note *5*. *Table 9: General hardware register map*: removed I2C_PECR register. *Section 10.3.7: Reset pin characteristics*: added text regarding the rest network.
10-Feb-2012	12	*Figure 1: STM8S20xxx block diagram*: updated POR/PDR and BOR; updated LINUART input; added legend. *Table 18: General operating conditions*: updated V_{CAP}. *Table 26: Total current consumption in halt mode at VDD = 5 V*: updated title, modified existing max column, and added new max column (at 125 °C) with data. *Table 37: I/O static characteristics*: added new condition and new max values for rise and fall time; added footnote *3*; updated Typ and max pull-up resistor values. *Section 10.3.7: Reset pin characteristics*: updated cross reference in text below *Figure 35* *Table 41: NRST pin characteristics*: updated Typ and max values of the NRST pull-up resistor.