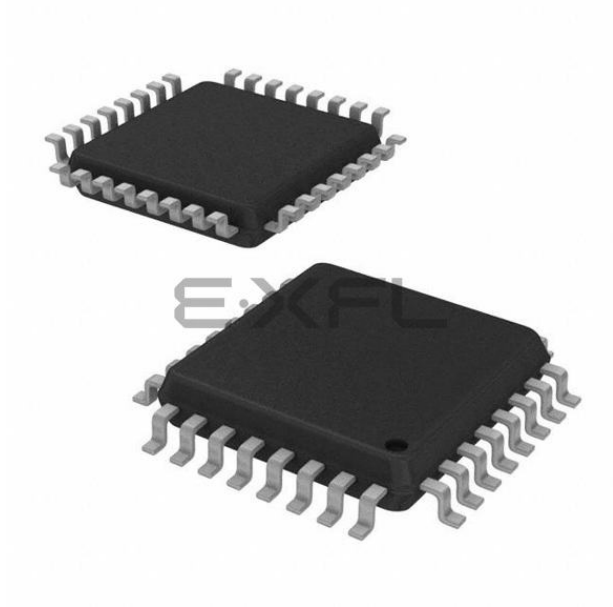


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s207k6t3c

List of figures

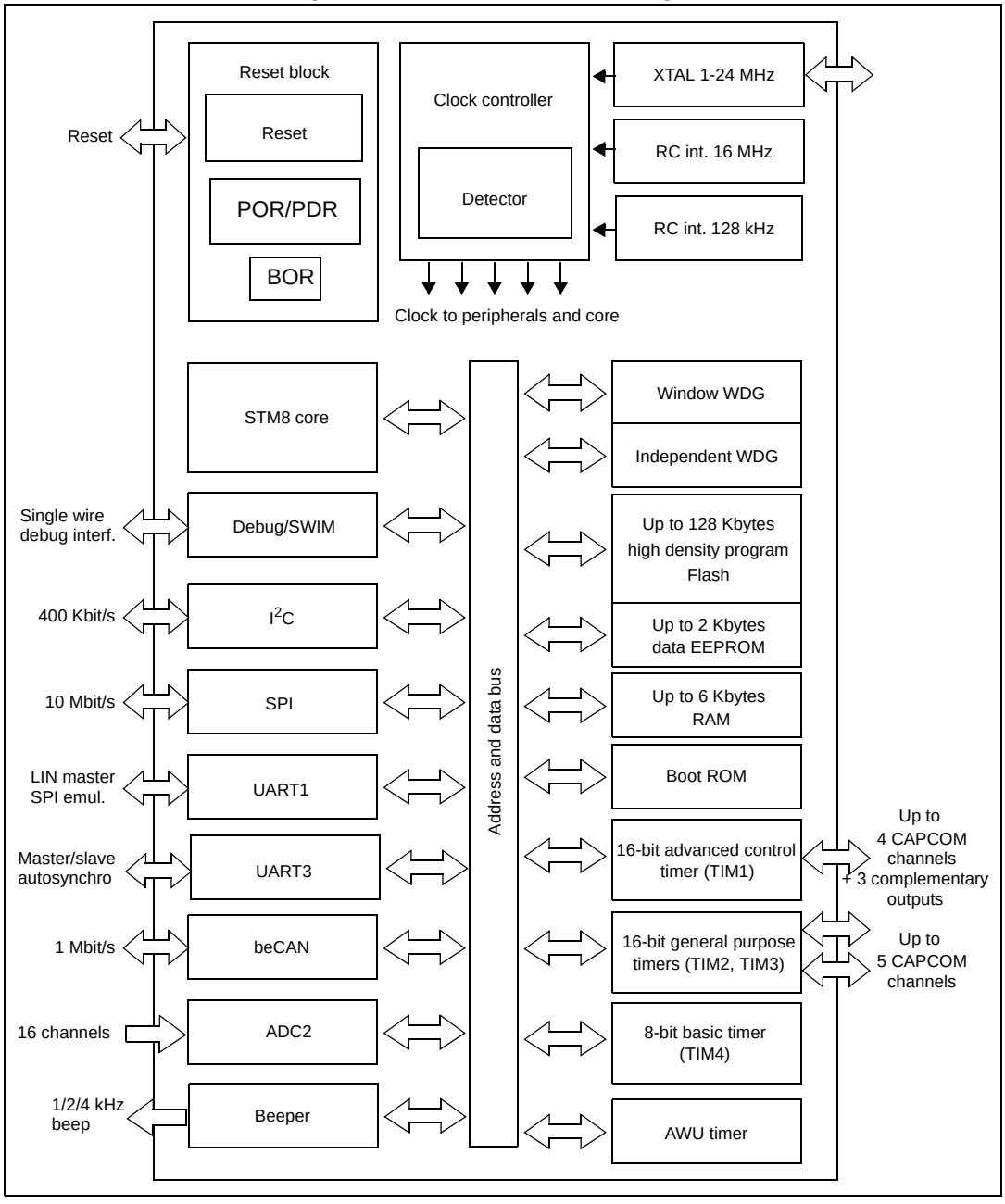
1 Introduction

This datasheet contains the description of the STM8S20xxx features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8S microcontroller memory, registers and peripherals, please refer to the STM8S microcontroller family reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8S Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

3 Block diagram

Figure 1. STM8S20xxx block diagram



1. Legend:
ADC: Analog-to-digital converter
beCAN: Controller area network
BOR: Brownout reset
I²C: Inter-integrated circuit multimaster interface
Independent WDG: Independent watchdog
POR/PDR: Power on reset / power down reset
SPI: Serial peripheral interface
SWIM: Single wire interface module
UART: Universal asynchronous receiver transmitter
Window WDG: Window watchdog

4.5 Clock controller

The clock controller distributes the system clock (f_{MASTER}) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- ***Clock prescaler*:** To get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- ***Safe clock switching*:** Clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- ***Clock management*:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- ***Master clock sources*:** Four different clock sources can be used to drive the master clock:
  - 1-24 MHz high-speed external crystal (HSE)
  - Up to 24 MHz high-speed user-external clock (HSE user-ext)
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
- ***Startup clock*:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- ***Clock security system (CSS)*:** This feature can be enabled by software. If an HSE clock failure occurs, the internal RC (16 MHz/8) is automatically selected by the CSS and an interrupt can optionally be generated.
- ***Configurable main clock output (CCO)*:** This outputs an external clock for use by the application.

Table 3. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers

Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock
PCKEN17	TIM1	PCKEN13	UART3	PCKEN27	beCAN	PCKEN23	ADC
PCKEN16	TIM3	PCKEN12	UART1	PCKEN26	Reserved	PCKEN22	AWU
PCKEN15	TIM2	PCKEN11	SPI	PCKEN25	Reserved	PCKEN21	Reserved
PCKEN14	TIM4	PCKEN10	I^2C	PCKEN24	Reserved	PCKEN20	Reserved

4.12 TIM4 - 8-bit basic timer

- 8-bit autoreload, adjustable prescaler ratio to any power of 2 from 1 to 128
- Clock source: CPU clock
- Interrupt source: 1 x overflow/update

Table 4. TIM timer features

Timer	Counter size (bits)	Prescaler	Counting mode	CAPCOM channels	Complem. outputs	Ext. trigger	Timer synchr-onization/ chaining
TIM1	16	Any integer from 1 to 65536	Up/down	4	3	Yes	No
TIM2	16	Any power of 2 from 1 to 32768	Up	3	0	No	
TIM3	16	Any power of 2 from 1 to 32768	Up	2	0	No	
TIM4	8	Any power of 2 from 1 to 128	Up	0	0	No	

4.13 Analog-to-digital converter (ADC2)

STM8S20xxx performance line products contain a 10-bit successive approximation A/D converter (ADC2) with up to 16 multiplexed input channels and the following main features:

- Input voltage range: 0 to V_{DDA}
- Dedicated voltage reference (VREF) pins available on 80 and 64-pin devices
- Conversion time: 14 clock cycles
- Single and continuous modes
- External trigger input
- Trigger from TIM1 TRGO
- End of conversion (EOC) interrupt

4.14 Communication interfaces

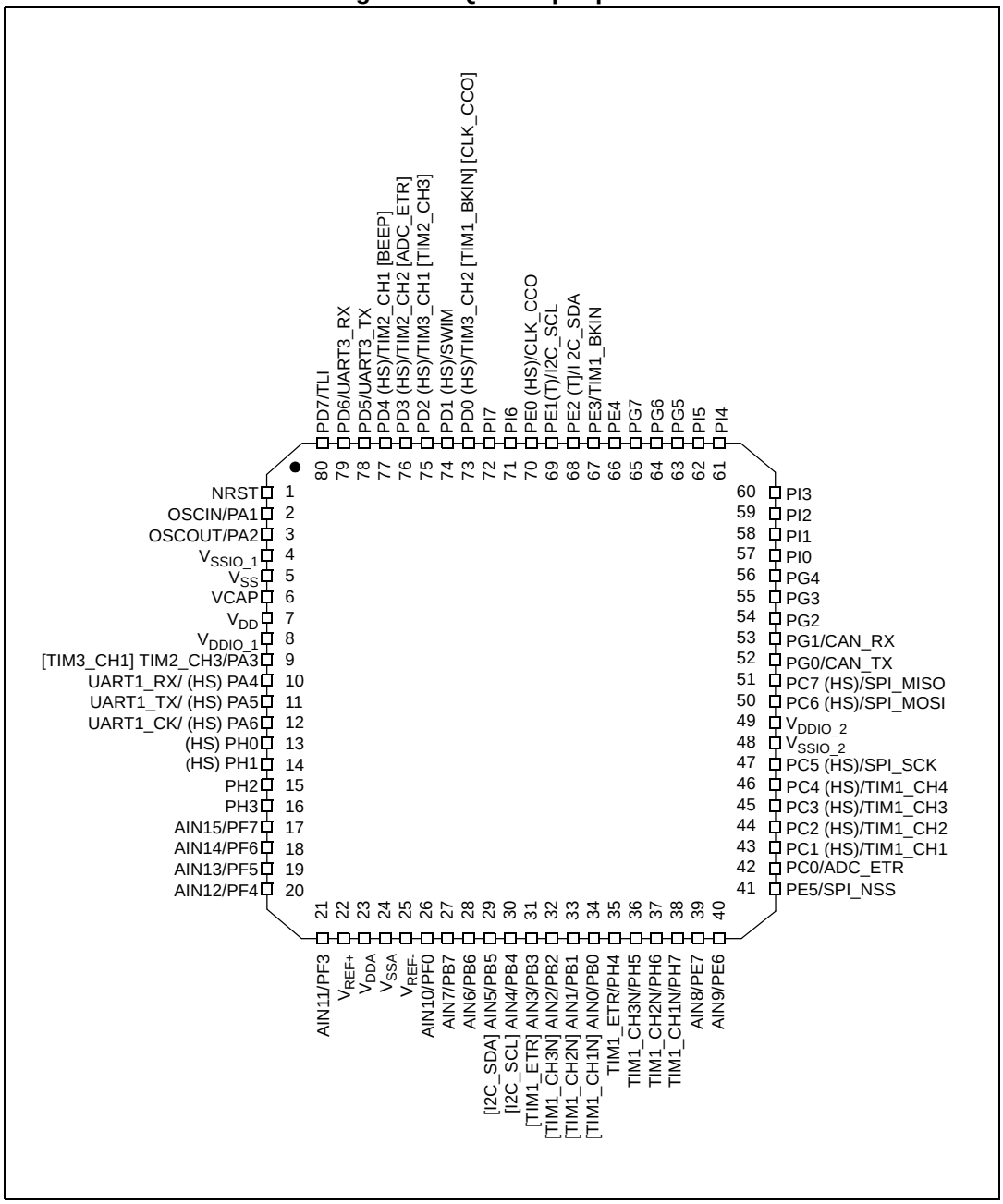
The following communication interfaces are implemented:

- UART1: Full feature UART, SPI emulation, LIN2.1 master capability, Smartcard mode, IrDA mode, single wire mode.
- UART3: Full feature UART, LIN2.1 master/slave capability
- SPI: Full and half-duplex, 10 Mbit/s
- I^2C: Up to 400 Kbit/s
- beCAN (rev. 2.0A,B) - 3 Tx mailboxes - up to 1 Mbit/s

5 Pinouts and pin description

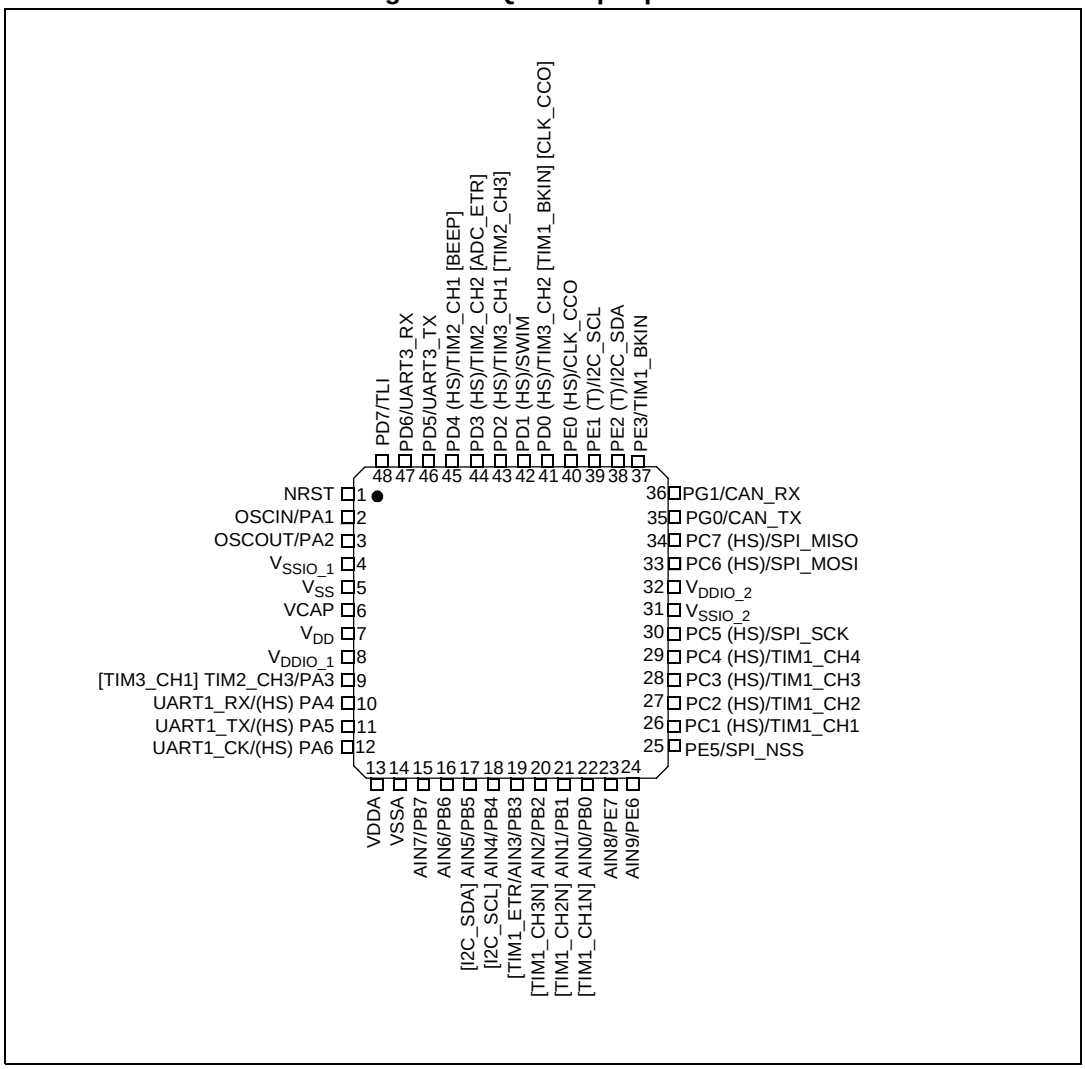
5.1 Package pinouts

Figure 3. LQFP 80-pin pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
4. CAN_RX and CAN_TX is available on STM8S208xx devices only.

Figure 5. LQFP 48-pin pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
4. CAN_RX and CAN_TX is available on STM8S208xx devices only.

6 Memory and register map

6.1 Memory map

Figure 8. Memory map

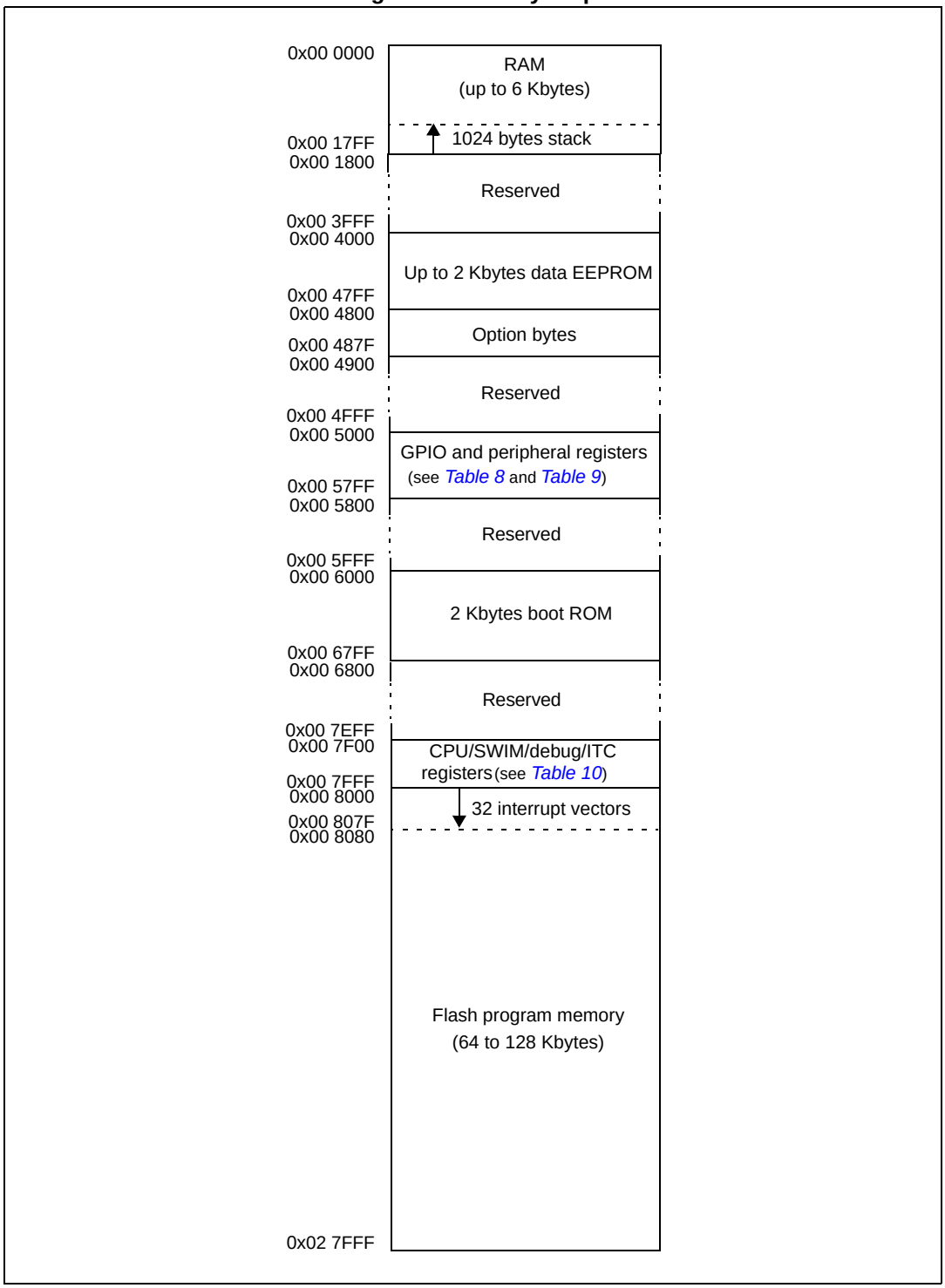


Table 16. Current characteristics

Symbol	Ratings	Max.(1)	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(2)	60	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(2)	60	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	20	
ΣI_{IO}	Total output current sourced (sum of all I/O and control pins) for devices with two V_{DDIO} pins(3)	200	
	Total output current sourced (sum of all I/O and control pins) for devices with one V_{DDIO} pin(3)	100	
	Total output current sunk (sum of all I/O and control pins) for devices with two V_{SSIO} pins(3)	160	
	Total output current sunk (sum of all I/O and control pins) for devices with one V_{SSIO} pin(3)	80	
$I_{INJ(PIN)}$(4)(5)	Injected current on NRST pin	±4	
	Injected current on OSCIN pin	±4	
	Injected current on any other pin(6)	±4	
$\Sigma I_{INJ(PIN)}$(4)	Total injected current (sum of all I/O and control pins)(6)	±20	

1. Data based on characterization results, not tested in production.
2. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external supply.
3. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package between the V_{DDIO}/V_{SSIO} pins.
4. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected
5. Negative injection disturbs the analog performance of the device. See note in *Section 10.3.10: 10-bit ADC characteristics on page 85*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 17. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	150	

Total current consumption in wait mode

Table 22. Total current consumption in wait mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 24 MHz, $T_A \leq$ 105 °C	HSE crystal osc. (24 MHz)	2.4		mA
			HSE user ext. clock (24 MHz)	1.8	4.7	
		$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	2.0		
			HSE user ext. clock (16 MHz)	1.4	4.4	
			HSI RC osc. (16 MHz)	1.2	1.6	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	1.0		
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.55		
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.5		

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Table 23. Total current consumption in wait mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 24 MHz, $T_A \leq$ 105 °C	HSE crystal osc. (24 MHz)	2.0		mA
			HSE user ext. clock (24 MHz)	1.8	4.7	
		$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.6		
			HSE user ext. clock (16 MHz)	1.4	4.4	
			HSI RC osc. (16 MHz)	1.2	1.6	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	1.0		
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.55		
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	LSI RC osc. (128 kHz)	0.5		

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Total current consumption in active halt mode

Table 24. Total current consumption in active halt mode at V_{DD} = 5 V, T_A -40 to 85° C

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source			
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal oscillator (16 MHz)	1000		µA
				LSI RC oscillator (128 kHz)	200	260	
			Power-down mode	HSE crystal oscillator (16 MHz)	940		
				LSI RC oscillator (128 kHz)	140		
		Off	Operating mode	LSI RC oscillator 128 kHz)	68		
			Power-down mode		11	45	

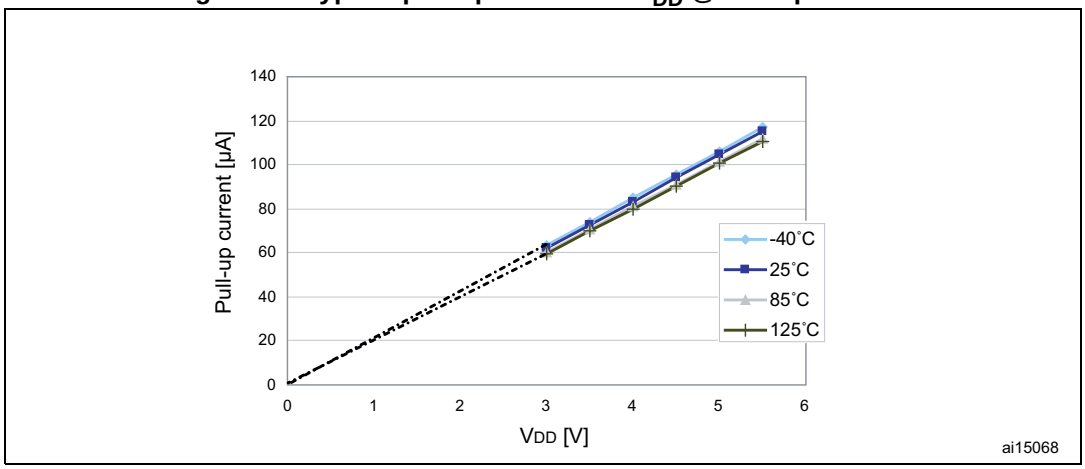
1. Data based on characterization results, not tested in production.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Table 25. Total current consumption in active halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions			Typ(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source		
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	600	µA
				LSI RC osc. (128 kHz)	200	
			Power-down mode	HSE crystal osc. (16 MHz)	540	
				LSI RC osc. (128 kHz)	140	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	
			Power-down mode		9	

1. Data based on characterization results, not tested in production.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Figure 22. Typical pull-up current vs V_{DD} @ 4 temperatures



1. The pull-up is a pure resistor (slope goes through 0).

Table 38. Output driving current (standard ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO} = 10 mA, V_{DD} = 5 V		2	V
	Output low level with 4 pins sunk	I_{IO} = 4 mA, V_{DD} = 3.3 V		1(1)	
V_{OH}	Output high level with 8 pins sourced	I_{IO} = 10 mA, V_{DD} = 5 V	2.8		V
	Output high level with 4 pins sourced	I_{IO} = 4 mA, V_{DD} = 3.3 V	2.1(1)		

1. Data based on characterization results, not tested in production

Table 39. Output driving current (true open drain ports)

Symbol	Parameter	Conditions	Max	Unit
V_{OL}	Output low level with 2 pins sunk	I_{IO} = 10 mA, V_{DD} = 5 V	1	V
		I_{IO} = 10 mA, V_{DD} = 3.3 V	1.5(1)	
		I_{IO} = 20 mA, V_{DD} = 5 V	2(1)	

1. Data based on characterization results, not tested in production

Table 40. Output driving current (high sink ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO} = 10 mA, V_{DD} = 5 V		0.8	V
	Output low level with 4 pins sunk	I_{IO} = 10 mA, V_{DD} = 3.3 V		1(1)	
	Output low level with 4 pins sunk	I_{IO} = 20 mA, V_{DD} = 5 V		1.5(1)	
V_{OH}	Output high level with 8 pins sourced	I_{IO} = 10 mA, V_{DD} = 5 V	4.0		
	Output high level with 4 pins sourced	I_{IO} = 10 mA, V_{DD} = 3.3 V	2.1(1)		
	Output high level with 4 pins sourced	I_{IO} = 20 mA, V_{DD} = 5 V	3.3(1)		

1. Data based on characterization results, not tested in production

10.3.7 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 41. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage (1)		-0.3 V		0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST Input high level voltage (1)		0.7 x V_{DD}		V_{DD} + 0.3	
$V_{OL(NRST)}$	NRST Output low level voltage (1)	I_{OL}= 2 mA			0.5	
$R_{PU(NRST)}$	NRST Pull-up resistor (2)		30	55	80	kΩ
$t_{IFP(NRST)}$	NRST Input filtered pulse (3)				75	ns
$t_{INFP(NRST)}$	NRST Input not filtered pulse (3)		500			ns
$t_{OP(NRST)}$	NRST output pulse (1)		15			µs

1. Data based on characterization results, not tested in production.
2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor
3. Data guaranteed by design, not tested in production.

Figure 33. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

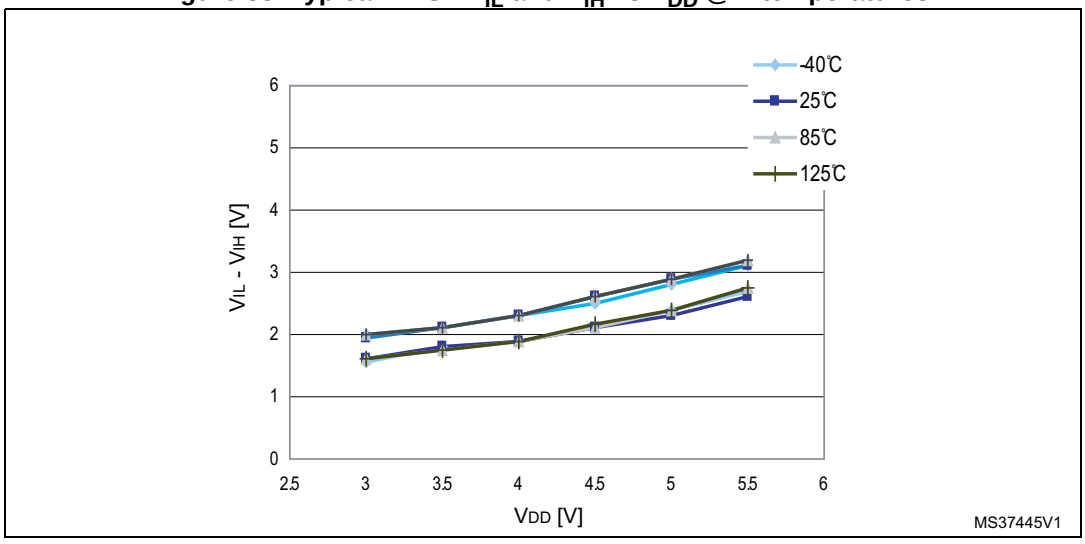
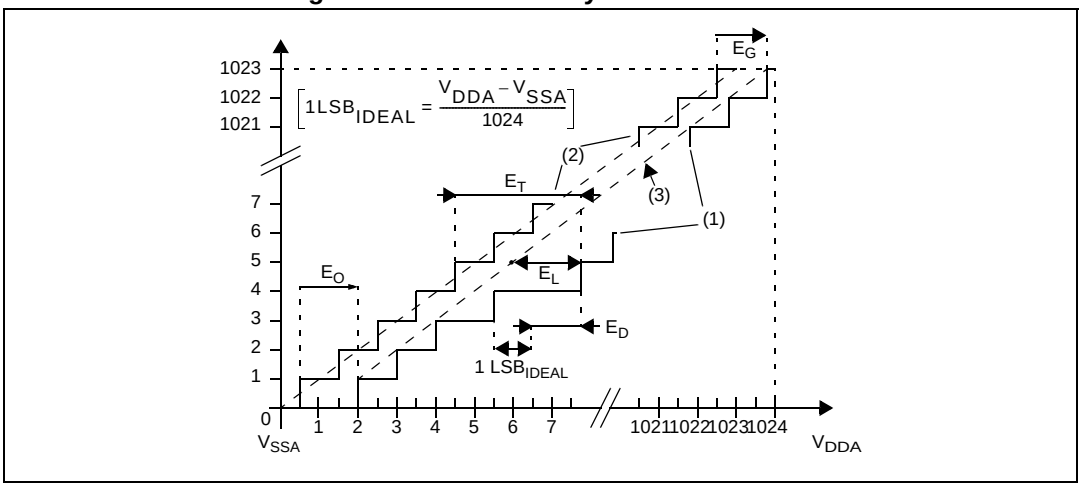


Figure 41. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. The ideal transfer curve
3. End point correlation line
   E_T = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset error: deviation between the first actual transition and the first ideal one.
   E_G = Gain error: deviation between the last ideal transition and the last actual one.
   E_D = Differential linearity error: maximum deviation between actual steps and the ideal one.
   E_L = Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

Figure 42. Typical application with ADC

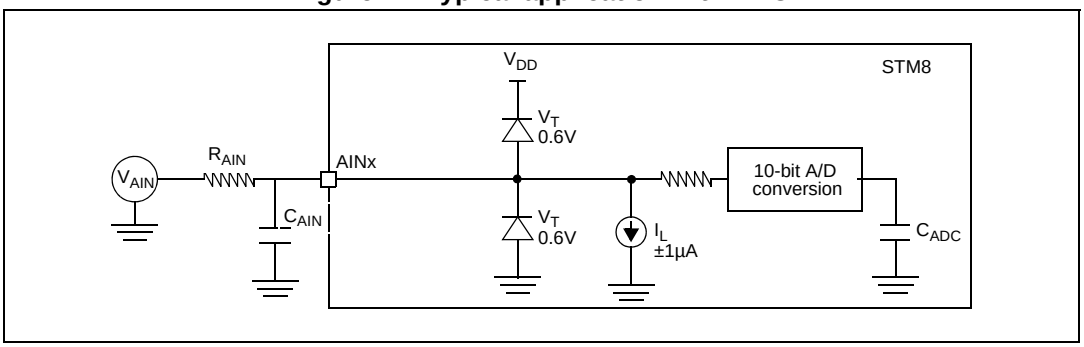
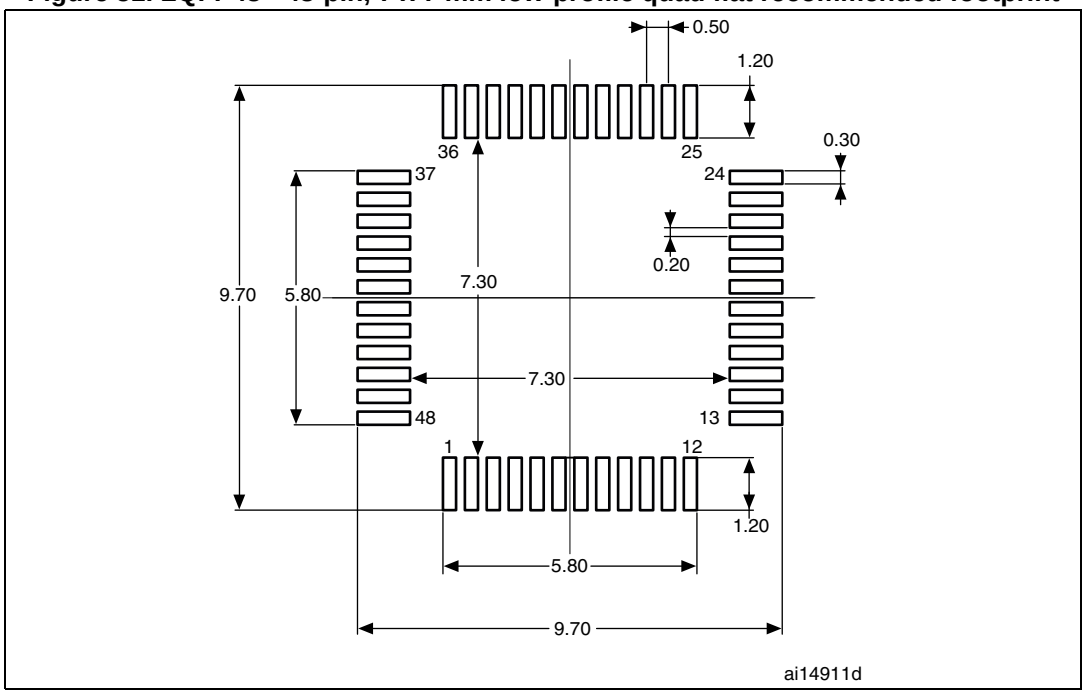


Table 54. LQFP48 - 48-pin, 7x 7 mm low-profile quad flat package mechanical (continued)

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal places.

Figure 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint

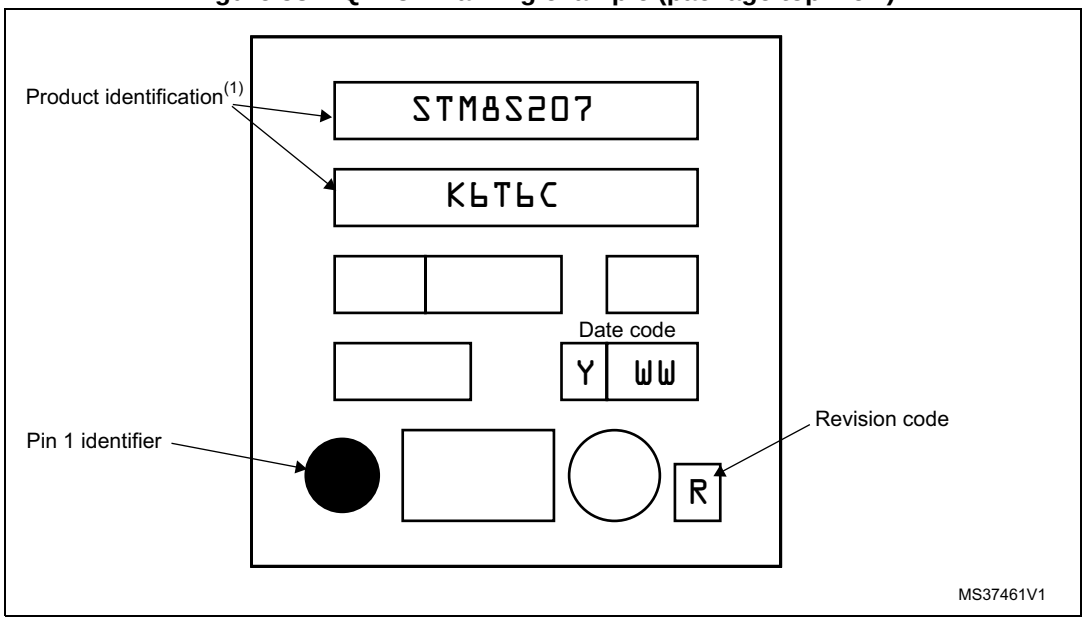


1. Dimensions are expressed in millimeters.

Device marking

The following figure shows the marking for the LQFP32 package.

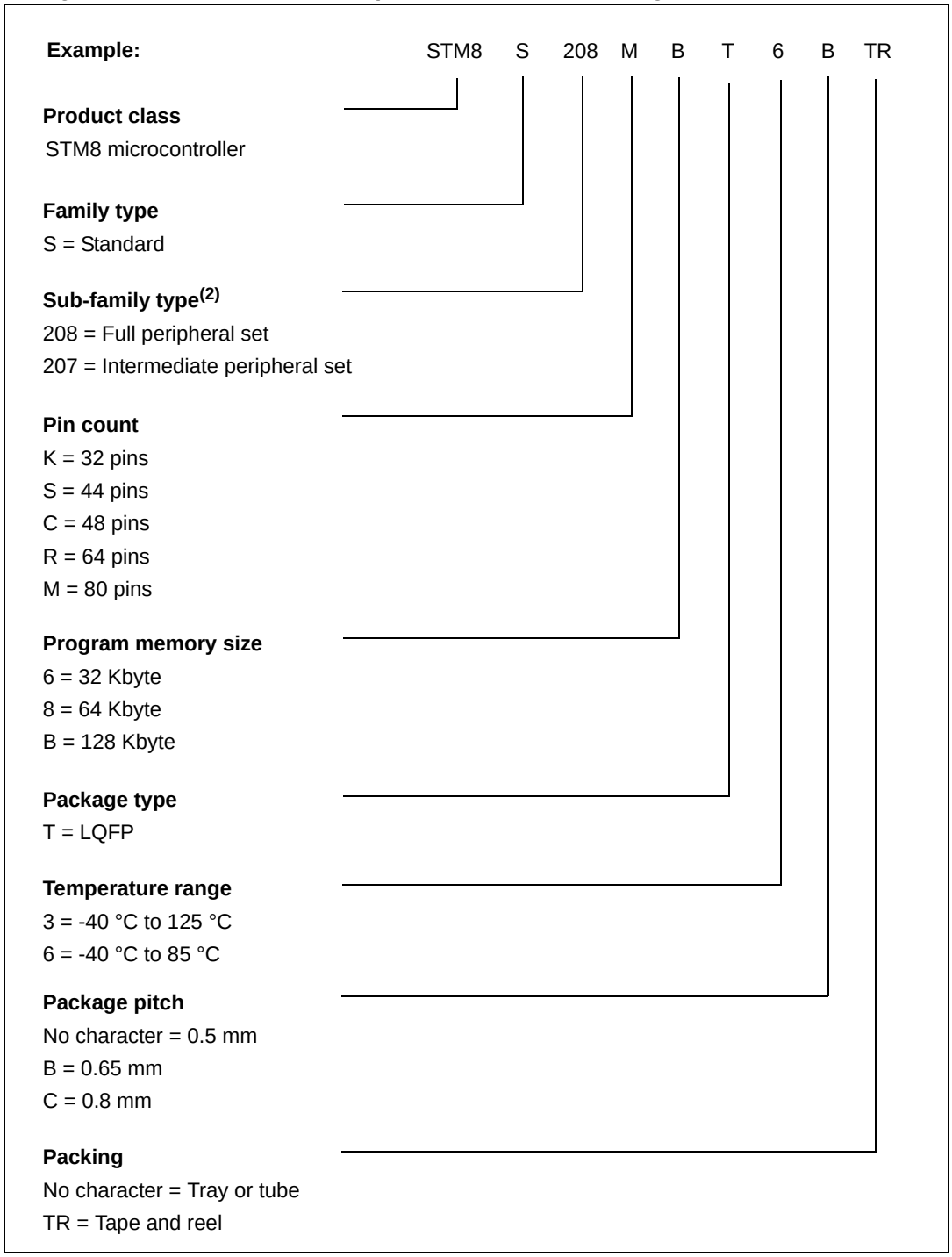
Figure 58. LQFP32 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

13 Ordering information

Figure 59. STM8S207xx/208xx performance line ordering information scheme(1)



1. For a list of available options (e.g. memory size, package) and order-able part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the ST Sales Office nearest to you.
2. Refer to *Table 2: STM8S20xxx performance line features* for detailed description.

Table 58. Document revision history (continued)

Date	Revision	Changes
14-Sep-2010	10	Added part number STM8S208M8 to *Table 1: Device summary*. Updated “reset state” of *Table 5: Legend/abbreviations for pinout table*. Added footnote *4* to *Table 6: Pin description*. *Table 9: General hardware register map*: standardized all reset state values; updated the reset state values of RST_SR, CLK_SWCR, CLK_HSITRIMR, CLK_SWIMCCR, IWDG_KR, and ADC_DRx registers; added the reset values of the CAN paged registers. *Figure 36: Recommended reset pin protection*: replaced 0.01 µF with 0.1 µF. *Figure 40: Typical application with I2C bus and timing diagram*: $t_{w(SCKH)}$, $t_{w(SCKL)}$, $t_{r(SCK)}$, and $t_{f(SCK)}$ replaced by $t_{w(SCLH)}$, $t_{w(SCLL)}$, $t_{r(SCL)}$, and $t_{f(SCL)}$ respectively.
22-Mar-2011	11	*Table 1: Device summary*: added STM8S207K8. *Table 2: STM8S20xxx performance line features*: added STM8S207K8 device and changed the RAM value of all other devices to 6 Kbytes. *Figure 5*, *Figure 4*, *Figure 5*, and *Figure 7*: removed TIM1_CH4 from pins 80, 64, 48, and 32 respectively. *Table 6: Pin description*: updated note *3* and added note *5*. *Table 9: General hardware register map*: removed I2C_PECR register. *Section 10.3.7: Reset pin characteristics*: added text regarding the rest network.
10-Feb-2012	12	*Figure 1: STM8S20xxx block diagram*: updated POR/PDR and BOR; updated LINUART input; added legend. *Table 18: General operating conditions*: updated V_{CAP}. *Table 26: Total current consumption in halt mode at VDD = 5 V*: updated title, modified existing max column, and added new max column (at 125 °C) with data. *Table 37: I/O static characteristics*: added new condition and new max values for rise and fall time; added footnote *3*; updated Typ and max pull-up resistor values. *Section 10.3.7: Reset pin characteristics*: updated cross reference in text below *Figure 35* *Table 41: NRST pin characteristics*: updated Typ and max values of the NRST pull-up resistor.