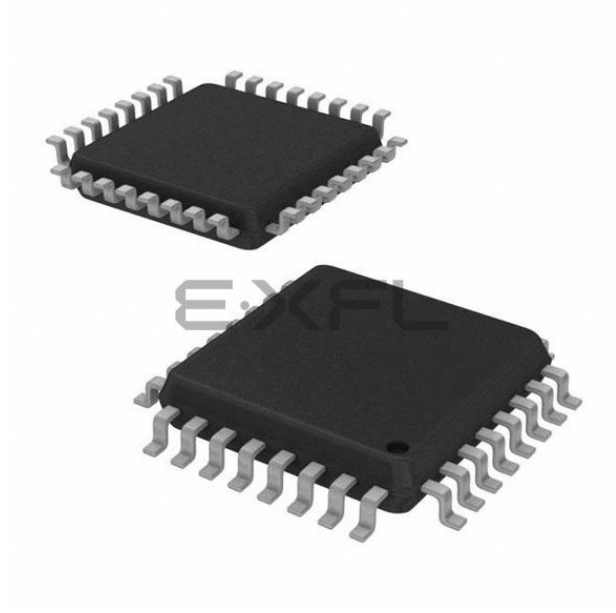

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s207k6t3ctr

List of figures

2 Description

The STM8S20xxx performance line 8-bit microcontrollers offer from 32 to 128 Kbytes Flash program memory. They are referred to as high-density devices in the STM8S microcontroller family reference manual.

All STM8S20xxx devices provide the following benefits: reduced system cost, performance robustness, short development cycles, and product longevity.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 k write/erase cycles and a high system integration level with internal clock oscillators, watchdog, and brown-out reset.

Device performance is ensured by 20 MIPS at 24 MHz CPU clock frequency and enhanced characteristics which include robust I/O, independent watchdogs (with a separate clock source), and a clock security system.

Short development cycles are guaranteed due to application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals. Full documentation is offered with a wide choice of development tools.

Product longevity is ensured in the STM8S family thanks to their advanced core which is made in a state-of-the art technology for applications with 2.95 V to 5.5 V operating supply.

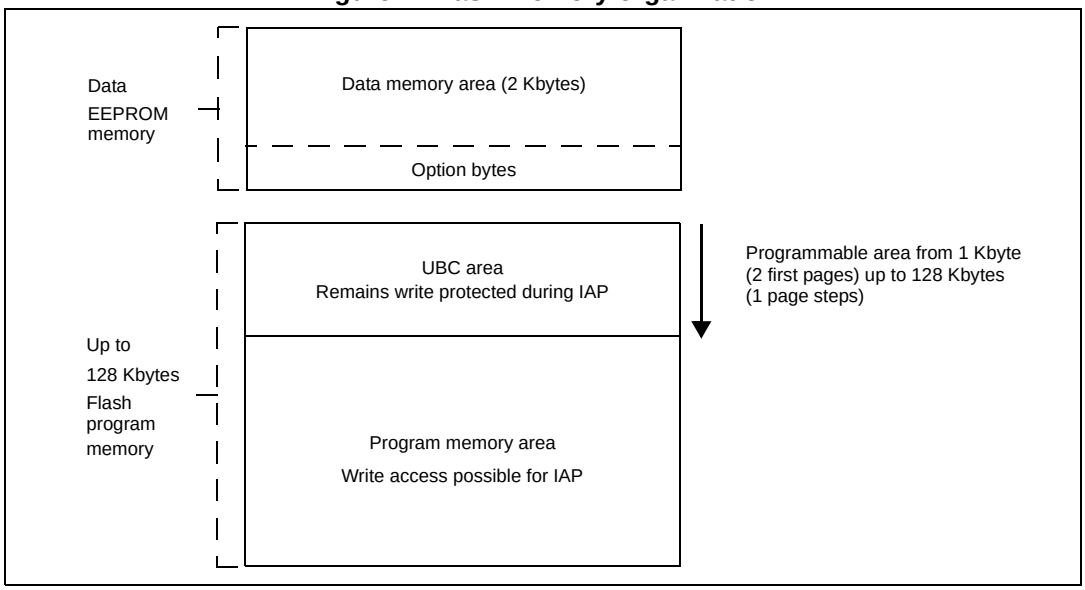
The size of the UBC is programmable through the UBC option byte (*Table 13.*), in increments of 1 page (512 bytes) by programming the UBC option byte in ICP mode.

This divides the program memory into two areas:

- Main program memory: Up to 128 Kbytes minus UBC
- User-specific boot code (UBC): Configurable up to 128 Kbytes

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

Figure 2. Flash memory organization



Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure

The IWDG time base spans from 60 µs to 1 s.

4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock
- LSI clock can be internally connected to TIM3 input capture channel 1 for calibration

4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

4.10 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signals
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

4.11 TIM2, TIM3 - 16-bit general purpose timers

- 16-bit autoreload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1…32768
- Timers with 3 or 2 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 2 or 3 x input capture/output compare, 1 x overflow/update

4.14.1 UART1

Main features

- One Mbit/s full duplex SCI
- SPI emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- LIN master mode
- Single wire half duplex mode

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Maximum speed: 1 Mbit/s at 16 MHz (f_{CPU}/16)

LIN master mode

- Emission: Generates 13-bit sync break frame
- Reception: Detects 11-bit break frame

4.14.2 UART3

Main features

- 1 Mbit/s full duplex SCI
- LIN master capable
- High precision baud rate generator

Table 6. Pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	LQFP44	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
31	27	19	18	13	PB3/AIN3	I/O	**X**	X	X		O1	X	X	**Port B3**	Analog input 3	TIM1_ETR [AFR5]
32	28	20	19	14	PB2/AIN2	I/O	**X**	X	X		O1	X	X	**Port B2**	Analog input 2	TIM1_ CH3N [AFR5]
33	29	21	20	15	PB1/AIN1	I/O	**X**	X	X		O1	X	X	**Port B1**	Analog input 1	TIM1_ CH2N [AFR5]
34	30	22	21	16	PB0/AIN0	I/O	**X**	X	X		O1	X	X	**Port B0**	Analog input 0	TIM1_ CH1N [AFR5]
35	-	-	-	-	PH4/TIM1_ETR	I/O	**X**	X			O1	X	X	**Port H4**	Timer 1 - trigger input	
36	-	-	-	-	PH5/ TIM1_CH3N	I/O	**X**	X			O1	X	X	**Port H5**	Timer 1 - inverted channel 3	
37	-	-	-	-	PH6/ TIM1_CH2N	I/O	**X**	X			O1	X	X	**Port H6**	Timer 1 - inverted channel 2	
38	-	-	-	-	PH7/ TIM1_CH1N	I/O	**X**	X			O1	X	X	**Port H7**	Timer 1 - inverted channel 2	
39	31	23	-	-	PE7/AIN8	I/O	**X**	X	X		O1	X	X	**Port E7**	Analog input 8	
40	32	24	22	-	PE6/AIN9	I/O	**X**	X	X		O1	X	X	**Port E6**	Analog input 9	
41	33	25	23	17	PE5/SPI_NSS	I/O	**X**	X	X		O1	X	X	**Port E5**	SPI master/slave select	
42	-	-	-	-	PC0/ADC_ETR	I/O	**X**	X	X		O1	X	X	**Port C0**	ADC trigger input	
43	34	26	24	18	PC1/TIM1_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port C1**	Timer 1 - channel 1	
44	35	27	25	19	PC2/TIM1_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port C2**	Timer 1- channel 2	
45	36	28	26	20	PC3/TIM1_CH3	I/O	**X**	X	X	HS	O3	X	X	**Port C3**	Timer 1 - channel 3	

Table 6. Pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	LQFP44	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
46	37	29	-	21	PC4/TIM1_CH4	I/O	**X**	X	X	HS	O3	X	X	**Port C4**	Timer 1 - channel 4	
47	38	30	27	22	PC5/SPI_SCK	I/O	**X**	X	X	HS	O3	X	X	**Port C5**	SPI clock	
48	39	31	28	-	V_{SSIO_2}	S								I/O ground		
49	40	32	29	-	V_{DDIO_2}	S								I/O power supply		
50	41	33	30	23	PC6/SPI_MOSI	I/O	**X**	X	X	HS	O3	X	X	**Port C6**	SPI master out/ slave in	
51	42	34	31	24	PC7/SPI_MISO	I/O	**X**	X	X	HS	O3	X	X	**Port C7**	SPI master in/ slave out	
52	43	35	32	-	PG0/CAN_TX(2)	I/O	**X**	X			O1	X	X	**Port G0**	beCAN transmit	
53	44	36	33	-	PG1/CAN_RX(2)	I/O	**X**	X			O1	X	X	**Port G1**	beCAN receive	
54	45	-	-	-	PG2	I/O	**X**	X			O1	X	X	**Port G2**		
55	46	-	-	-	PG3	I/O	**X**	X			O1	X	X	**Port G3**		
56	47	-	-	-	PG4	I/O	**X**	X			O1	X	X	**Port G4**		
57	48	-	-	-	PI0	I/O	**X**	X			O1	X	X	**Port I0**		
58	-	-	-	-	PI1	I/O	**X**	X			O1	X	X	**Port I1**		
59	-	-	-	-	PI2	I/O	**X**	X			O1	X	X	**Port I2**		
60	-	-	-	-	PI3	I/O	**X**	X			O1	X	X	**Port I3**		
61	-	-	-	-	PI4	I/O	**X**	X			O1	X	X	**Port I4**		
62	-	-	-	-	PI5	I/O	**X**	X			O1	X	X	**Port I5**		
63	49	-	-	-	PG5	I/O	**X**	X			O1	X	X	**Port G5**		
64	50	-	-	-	PG6	I/O	**X**	X			O1	X	X	**Port G6**		
65	51	-	-	-	PG7	I/O	**X**	X			O1	X	X	**Port G7**		
66	52	-	-	-	PE4	I/O	**X**	X	X		O1	X	X	**Port E4**		
67	53	37	-	-	PE3/TIM1_BKIN	I/O	**X**	X	X		O1	X	X	**Port E3**	Timer 1 - break input	
68	54	38	34	-	PE2/I^2C_SDA	I/O	**X**		X		O1	T(3)		**Port E2**	I^2C data	

Table 9. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5050 to 0x00 5059	Reserved area (10 bytes)			
0x00 505A	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 505B		FLASH_CR2	Flash control register 2	0x00
0x00 505C		FLASH_NCR2	Flash complementary control register 2	0xFF
0x00 505D		FLASH _FPR	Flash protection register	0x00
0x00 505E		FLASH _NFPR	Flash complementary protection register	0xFF
0x00 505F		FLASH _IAPSR	Flash in-application programming status register	0x00
0x00 5060 to 0x00 5061	Reserved area (2 bytes)			
0x00 5062	Flash	FLASH _PUKR	Flash Program memory unprotection register	0x00
0x00 5063	Reserved area (1 byte)			
0x00 5064	Flash	FLASH _DUKR	Data EEPROM unprotection register	0x00
0x00 5065 to 0x00 509F	Reserved area (59 bytes)			
0x00 50A0	ITC	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2 to 0x00 50B2	Reserved area (17 bytes)			
0x00 50B3	RST	RST_SR	Reset status register	0xXX(1)
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_ICKR	Internal clock control register	0x01
0x00 50C1		CLK_ECKR	External clock control register	0x00
0x00 50C2	Reserved area (1 byte)			
0x00 50C3	CLK	CLK_CMSR	Clock master status register	0xE1
0x00 50C4		CLK_SWR	Clock master switch register	0xE1
0x00 50C5		CLK_SWCR	Clock switch control register	0xXX
0x00 50C6		CLK_CKDIVR	Clock divider register	0x18
0x00 50C7		CLK_PCKENR1	Peripheral clock gating register 1	0xFF
0x00 50C8		CLK_CSSR	Clock security system register	0x00
0x00 50C9		CLK_CCOR	Configurable clock control register	0x00
0x00 50CA		CLK_PCKENR2	Peripheral clock gating register 2	0xFF
0x00 50CB		CLK_CANCCR	CAN clock control register	0x00

Table 16. Current characteristics

Symbol	Ratings	Max.(1)	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(2)	60	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(2)	60	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	20	
ΣI_{IO}	Total output current sourced (sum of all I/O and control pins) for devices with two V_{DDIO} pins(3)	200	
	Total output current sourced (sum of all I/O and control pins) for devices with one V_{DDIO} pin(3)	100	
	Total output current sunk (sum of all I/O and control pins) for devices with two V_{SSIO} pins(3)	160	
	Total output current sunk (sum of all I/O and control pins) for devices with one V_{SSIO} pin(3)	80	
$I_{INJ(PIN)}$(4)(5)	Injected current on NRST pin	±4	
	Injected current on OSCIN pin	±4	
	Injected current on any other pin(6)	±4	
$\Sigma I_{INJ(PIN)}$(4)	Total injected current (sum of all I/O and control pins)(6)	±20	

1. Data based on characterization results, not tested in production.
2. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external supply.
3. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package between the V_{DDIO}/V_{SSIO} pins.
4. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected
5. Negative injection disturbs the analog performance of the device. See note in *Section 10.3.10: 10-bit ADC characteristics on page 85*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 17. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	150	

10.3.3 External clock sources and timing characteristics

HSE user external clock

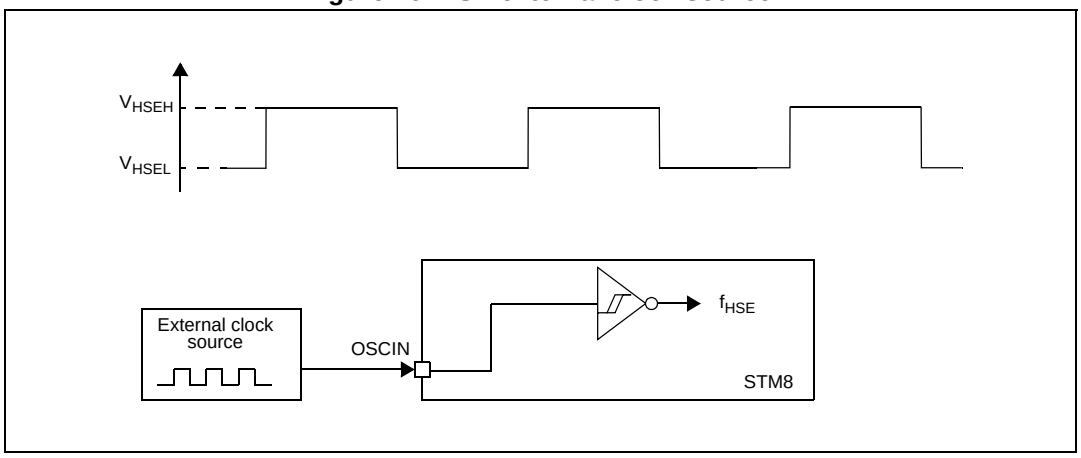
Subject to general operating conditions for V_{DD} and T_A.

Table 31. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency		0		24	MHz
V_{HSEH}(1)	OSCIN input pin high level voltage		0.7 x V_{DD}		V_{DD} + 0.3 V	V
V_{HSEL}(1)	OSCIN input pin low level voltage		V_{SS}		0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1		1	µA

1. Data based on characterization results, not tested in production.

Figure 16. HSE external clock source



HSE crystal/ceramic resonator oscillator

The HSE clock can be supplied with a 1 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Figure 29. Typ. V_{DD} - V_{OH} @ V_{DD} = 5 V (standard ports)

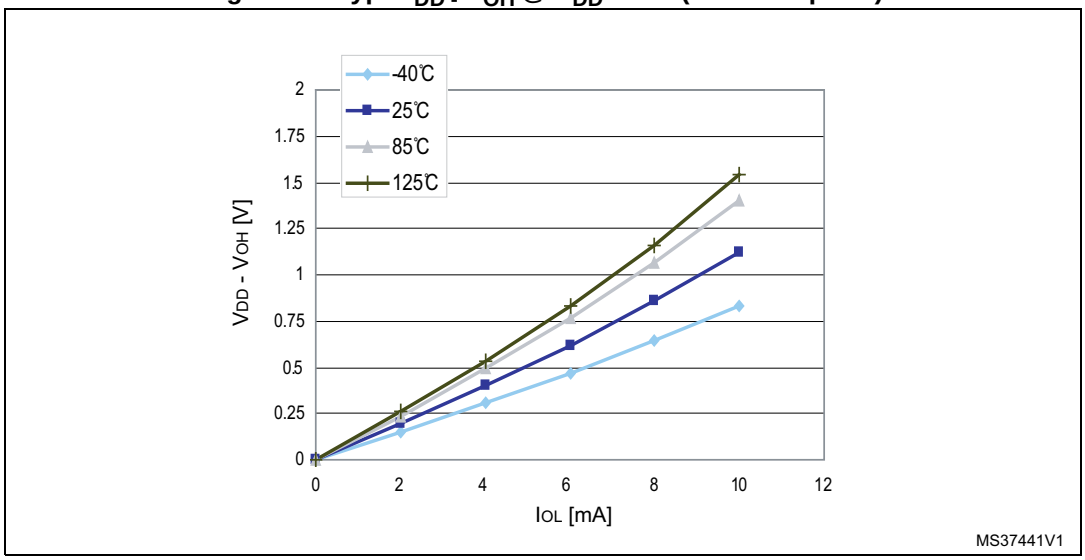
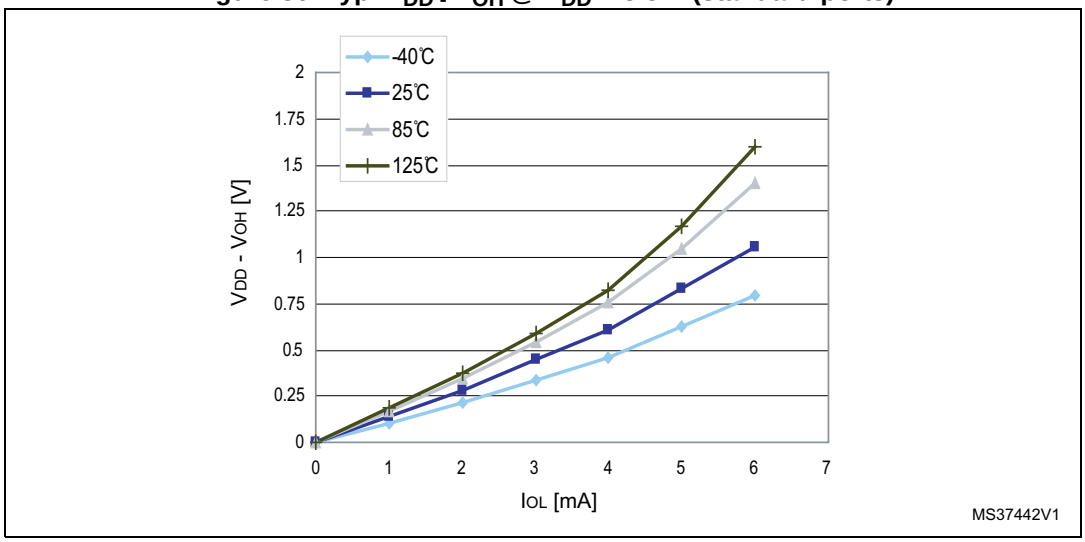


Figure 30. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (standard ports)



10.3.7 Reset pin characteristics

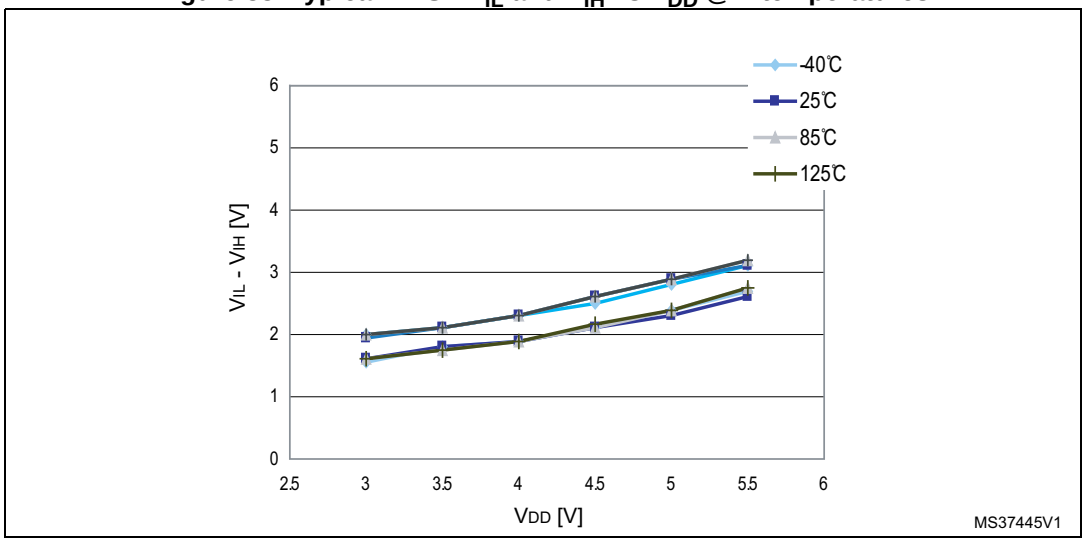
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 41. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage (1)		-0.3 V		0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST Input high level voltage (1)		0.7 x V_{DD}		V_{DD} + 0.3	
$V_{OL(NRST)}$	NRST Output low level voltage (1)	I_{OL}= 2 mA			0.5	
$R_{PU(NRST)}$	NRST Pull-up resistor (2)		30	55	80	kΩ
$t_{IFP(NRST)}$	NRST Input filtered pulse (3)				75	ns
$t_{INFP(NRST)}$	NRST Input not filtered pulse (3)		500			ns
$t_{OP(NRST)}$	NRST output pulse (1)		15			µs

1. Data based on characterization results, not tested in production.
2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor
3. Data guaranteed by design, not tested in production.

Figure 33. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures



10.3.8 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 42* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 42. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	10	MHz
		Slave mode	0	6	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		25	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	4 x t_{MASTER}		
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	70		
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode	$t_{SCK}/2$ - 15	$t_{SCK}/2$ + 15	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5		
		Slave mode	5		
$t_{h(MI)}$ (1) $t_{h(SI)}$ (1)	Data input hold time	Master mode	7		
		Slave mode	10		
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode		3 x t_{MASTER}	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	25		
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)		75	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)		30	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	31		
$t_{h(MO)}$ (1)		Master mode (after enable edge)	12		

1. Values based on design simulation and/or characterization results, and not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 37. SPI timing diagram - slave mode and CPHA = 0

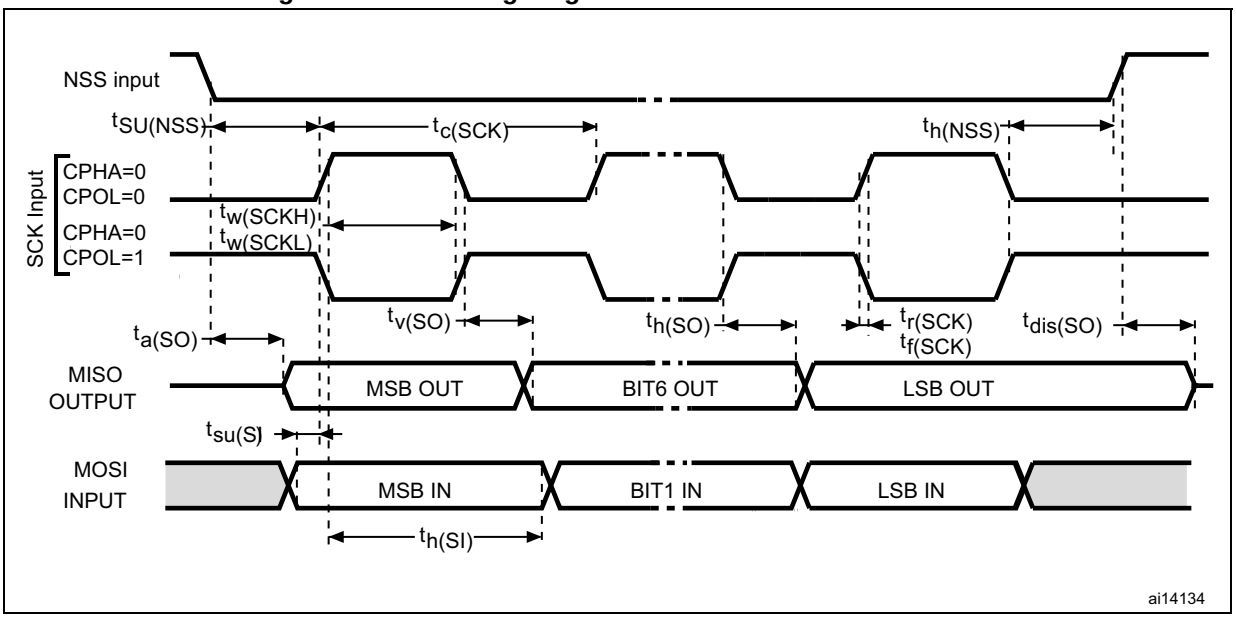
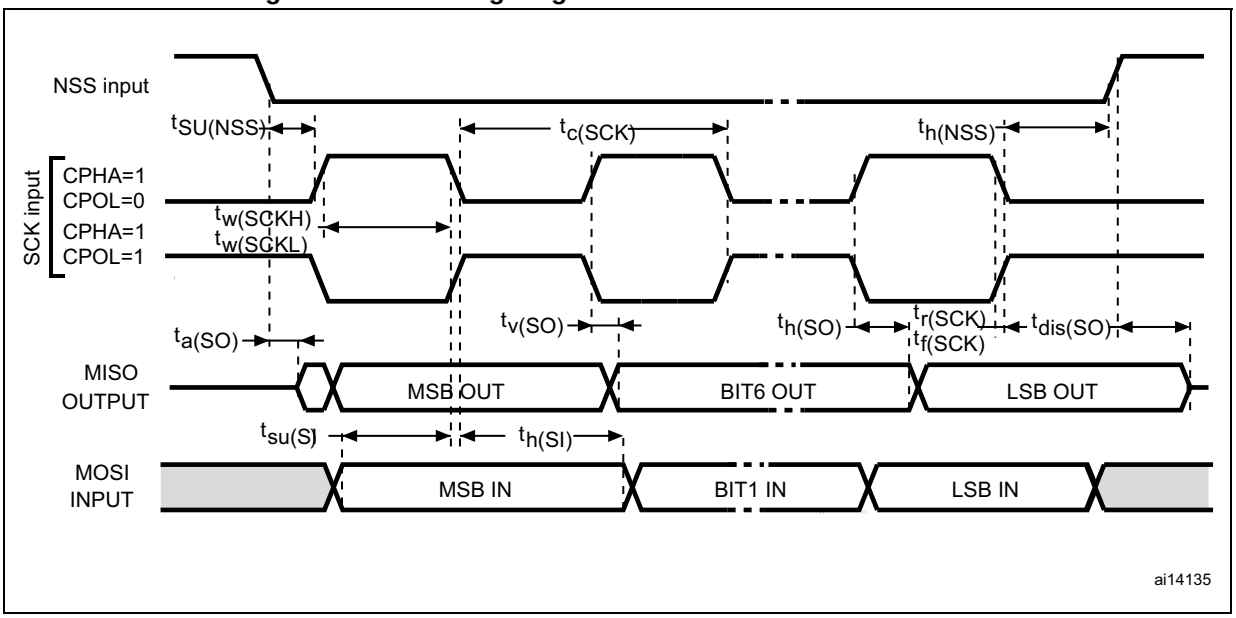


Figure 38. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Electromagnetic interference (EMI)

Emission tests conform to the SAE IEC 61967-2 standard for test software, board layout and pin loading.

Table 48. EMI data

Symbol	Parameter	Conditions					Unit
		General conditions	Monitored frequency band	Max f_{HSE}/f_{CPU} (1)			
				8 MHz/ 8 MHz	8 MHz/ 16 MHz	8 MHz/ 24 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V T_A = 25 °C LQFP80 package conforming to SAE IEC 61967-2	0.1MHz to 30 MHz	15	20	24	dBµV
			30 MHz to 130 MHz	18	21	16	
			130 MHz to 1 GHz	-1	1	4	
	SAE EMI level		SAE EMI level	2	2.5	2.5	

1. Data based on characterization results, not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 49. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value (1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to JESD22-A114	A	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	T_A= 25°C, conforming to JESD22-C101	IV	1000	V

1. Data based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance:

- A supply overvoltage (applied to each power supply pin)
- A current injection (applied to each input, output and configurable I/O pin) is performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 50. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	$T_A = 25$ °C	A
		$T_A = 85$ °C	A
		$T_A = 125$ °C	A

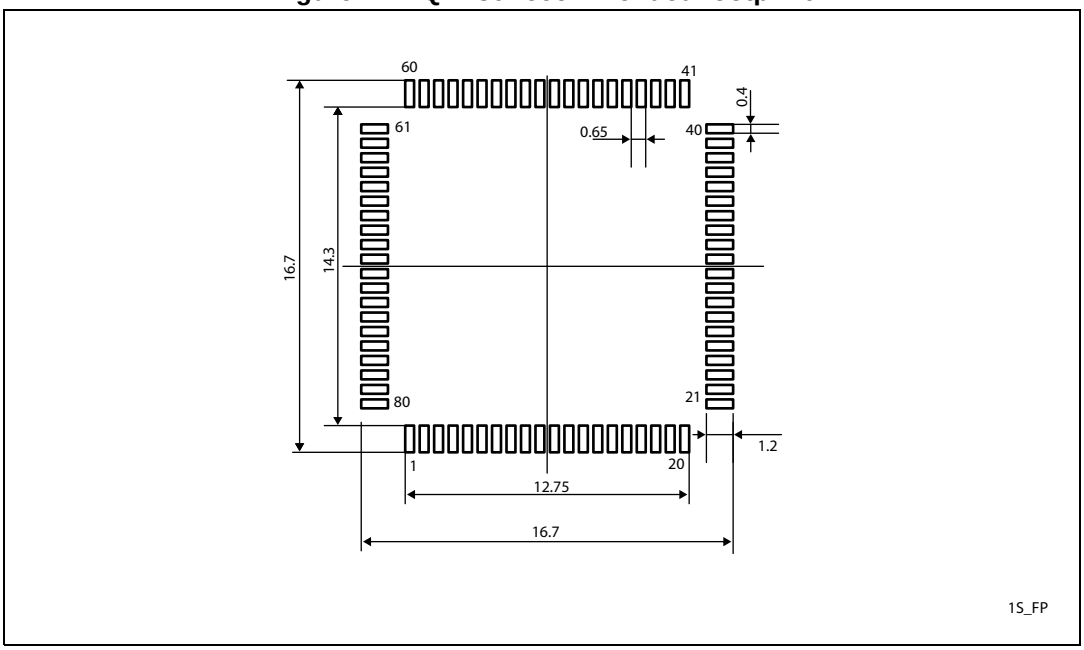
1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

Table 51. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package mechanical data(1) (continued)

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.350	-	-	0.4862	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.350	-	-	0.4862	-
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. LQFP80 recommended footprint



11.2 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 18: General operating conditions on page 56*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins, where: $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$, and taking account of the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 57. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 80 - 14 x 14 mm	38	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 64 - 14 x 14 mm	45	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 64 - 10 x 10 mm	46	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm	57	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 44 - 10 x 10 mm	54	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	60	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

11.2.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

14 Revision history

Table 58. Document revision history

Date	Revision	Changes
23-May-2008	1	Initial release.
05-Jun-2008	2	Added part numbers on page 1 and in *Table 2 on page 11*. Updated *Section 4: Product overview*. Updated *Section 10: Electrical characteristics*.
22-Jun-2008	3	Added part numbers on page 1 and in *Table 2 on page 11*.
12-Aug-2008	4	Added 32 pin device pinout and ordering information. Updated UBC option description in *Table 13 on page 48*. USART renamed UART1, LINUART renamed UART3. Max. ADC frequency increased to 6 MHz.
20-Oct-2008	5	Removed STM8S207K4 part number. Removed LQFP64 14 x 14 mm package. Added medium and high density Flash memory categories. Added *Section 6: Memory and register map on page 34*. Replaced beCAN3 by beCAN in *Section 4.14.5: beCAN*. Updated *Section 10: Electrical characteristics on page 52*. Updated LQFP44 (*Figure 53* and *Table 55*), and LQFP32 outline and mechanical data (*Figure 56*, and *Table 56*).
08-Dec-2008	6	Changed V_{DD} minimum value from 3.0 to 2.95 V. Updated number of High Sink I/Os in pinout. Removed FLASH _NFPR and FLASH _FPR registers in *Table 9: General hardware register map*.
30-Jan-2009	7	Removed preliminary status. Removed VQFN32 package. Added STM8S207C6, STM8S207S6. Updated external interrupts in *Table 2 on page 11*. Updated *Section 10: Electrical characteristics*.
10-Jul-2009	8	Document status changed from “preliminary data” to “datasheet”. Added LQFP64 14 x 14 mm package. Added STM8S207M8, STM8S207SB, STM8S208R8, STM8S208R6, STM8S208C8, and STM8S208C6, STM8S208SB, STM8S208S8, and STM8S208S6. Replaced “CAN” with “beCAN”. Added *Table 3* to *Section 4.5: Clock controller*. Updated *Section 4.8: Auto wakeup counter*. Added beCAN peripheral (impacting *Table 1* and *Figure 6*). Added footnote about CAN_RX/TX to pinout figures *5*, *4*, and *6*. *Table 6*: Removed ‘X’ from wpu column of I^2C pins (no wpu available). Added *Table 11: Interrupt mapping*.