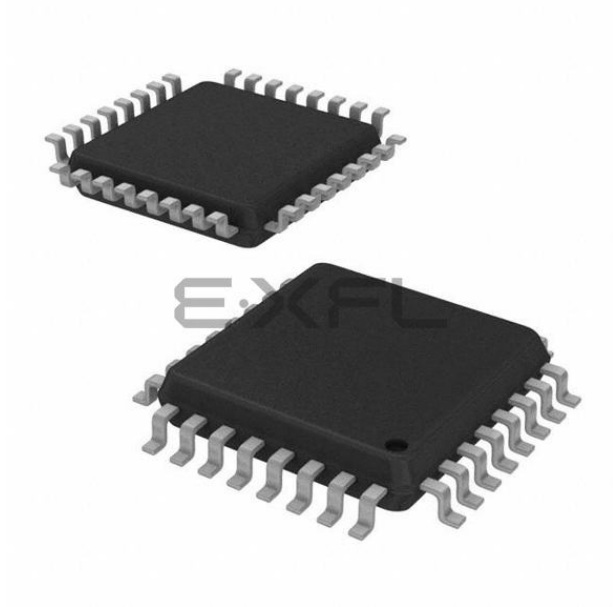


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | STM8 |
| Core Size | 8-Bit |
| Speed | 24MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 25 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 6K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.95V ~ 5.5V |
| Data Converters | A/D 7x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-LQFP |
| Supplier Device Package | 32-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s207k8t3c |

## 4.6 Power management

For efficient power management, the application can be put in one of four different low-power modes. You can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- ***Wait mode***: In this mode, the CPU is stopped, but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.
- ***Active halt mode with regulator on***: In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in active halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- ***Active halt mode with regulator off:*** This mode is the same as active halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.
- ***Halt mode***: In this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

## 4.7 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

Activation of the watchdog timers is controlled by option bytes or by software. Once activated, the watchdogs cannot be disabled by the user program without performing a reset.

### Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application perfectly.

The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout: At 16 MHz CPU clock the time-out period can be adjusted between 75 µs up to 64 ms.
2. Refresh out of window: The downcounter is refreshed before its value is lower than the one stored in the window register.

## 4.12 TIM4 - 8-bit basic timer

- 8-bit autoreload, adjustable prescaler ratio to any power of 2 from 1 to 128
- Clock source: CPU clock
- Interrupt source: 1 x overflow/update

**Table 4. TIM timer features**

| Timer | Counter size (bits) | Prescaler | Counting mode | CAPCOM channels | Complem. outputs | Ext. trigger | Timer synchr-onization/ chaining |
|---|---|---|---|---|---|---|---|
| TIM1 | 16 | Any integer from 1 to 65536 | Up/down | 4 | 3 | Yes | No |
| TIM2 | 16 | Any power of 2 from 1 to 32768 | Up | 3 | 0 | No | |
| TIM3 | 16 | Any power of 2 from 1 to 32768 | Up | 2 | 0 | No | |
| TIM4 | 8 | Any power of 2 from 1 to 128 | Up | 0 | 0 | No | |

## 4.13 Analog-to-digital converter (ADC2)

STM8S20xxx performance line products contain a 10-bit successive approximation A/D converter (ADC2) with up to 16 multiplexed input channels and the following main features:

- Input voltage range: 0 to $V_{DDA}$
- Dedicated voltage reference (VREF) pins available on 80 and 64-pin devices
- Conversion time: 14 clock cycles
- Single and continuous modes
- External trigger input
- Trigger from TIM1 TRGO
- End of conversion (EOC) interrupt

## 4.14 Communication interfaces

The following communication interfaces are implemented:

- UART1: Full feature UART, SPI emulation, LIN2.1 master capability, Smartcard mode, IrDA mode, single wire mode.
- UART3: Full feature UART, LIN2.1 master/slave capability
- SPI: Full and half-duplex, 10 Mbit/s
- $I^2C$: Up to 400 Kbit/s
- beCAN (rev. 2.0A,B) - 3 Tx mailboxes - up to 1 Mbit/s

### 4.14.1 UART1

#### Main features

- One  Mbit/s full duplex SCI
- SPI emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- LIN master mode
- Single wire half duplex mode

#### Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s ($f_{CPU}$/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

#### Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Maximum speed: 1 Mbit/s at 16 MHz ($f_{CPU}$/16)

#### LIN master mode

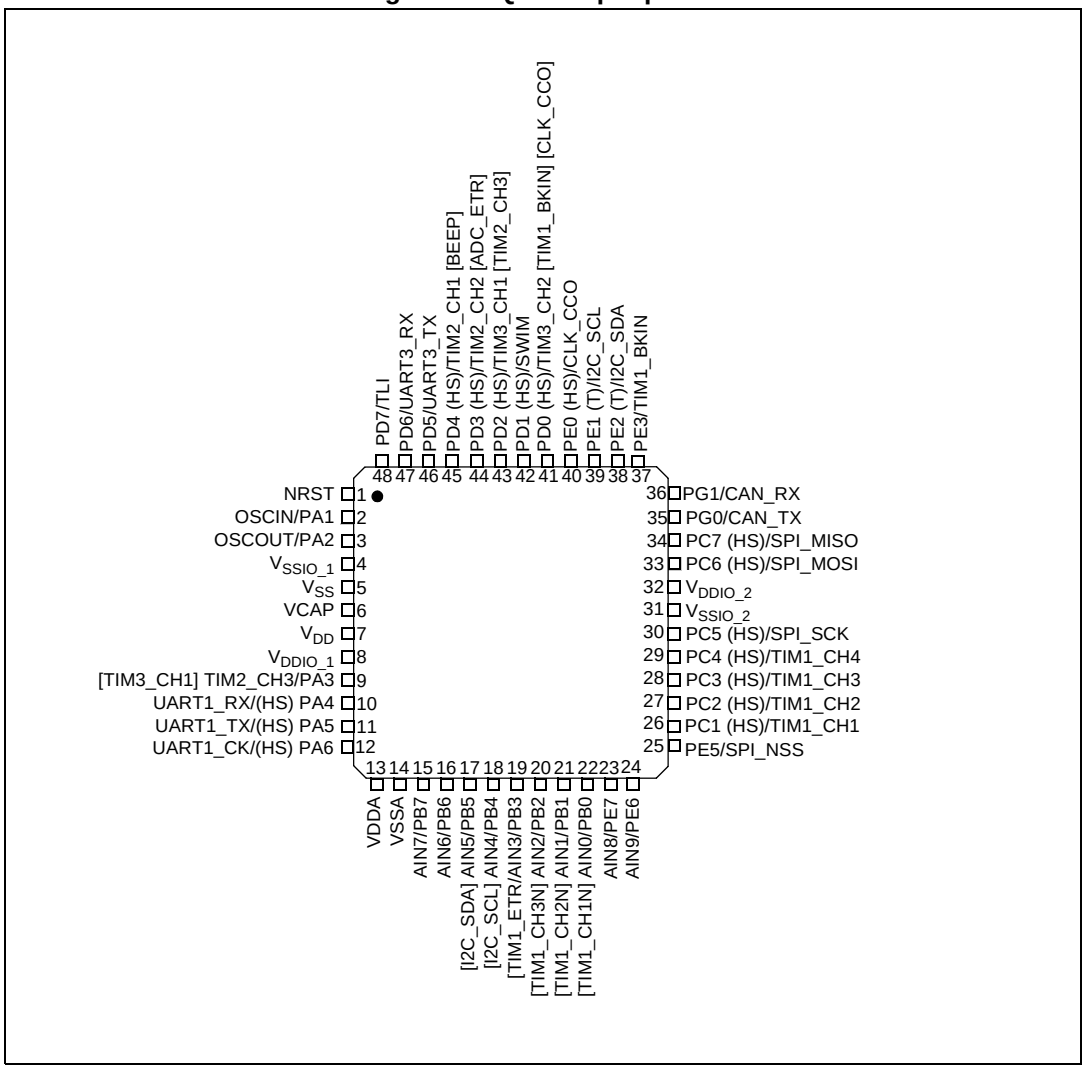
- Emission: Generates 13-bit sync break frame
- Reception: Detects 11-bit break frame

### 4.14.2 UART3

#### Main features

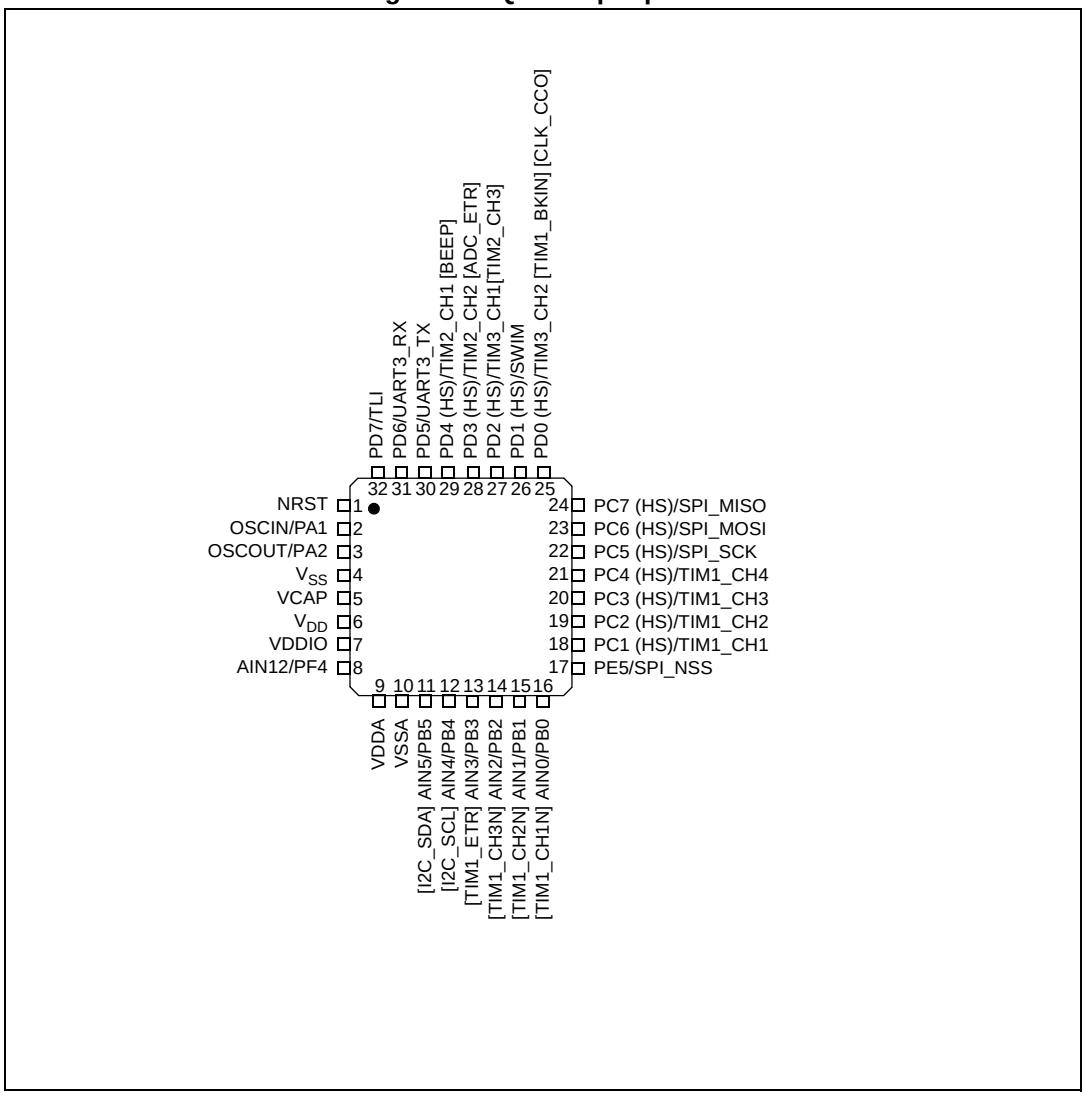
- 1 Mbit/s full duplex SCI
- LIN master capable
- High precision baud rate generator

**Figure 5. LQFP 48-pin pinout**




1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to $V_{DD}$ not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
4. CAN_RX and CAN_TX is available on STM8S208xx devices only.

**Figure 7. LQFP 32-pin pinout**




1. (HS) high sink capability.
2. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

**Table 5. Legend/abbreviations for pinout table**

| | | |
|---|---|---|
| **Type** | I= Input, O = Output, S = Power supply | |
| **Level** | Input | CM = CMOS |
| | Output | HS = High sink |
| **Output speed** | O1 = Slow (up to 2 MHz)<br>O2 = Fast (up to 10 MHz)<br>O3 = Fast/slow programmability with slow as default state after reset<br>O4 = Fast/slow programmability with fast as default state after reset | |
| **Port and control configuration** | Input | float = floating, wpu = weak pull-up |
| | Output | T = True open drain, OD = Open drain, PP = Push pull |
| **Reset state** | Bold **X** (pin state after internal reset release)<br>Unless otherwise specified, the pin state is the same during the reset phase and after the internal reset release. | |

**Table 6. Pin description**

| Pin number | | | | | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP80 | LQFP64 | LQFP48 | LQFP44 | LQFP32 | | | floating | wpu | Ext. interrupt | High sink | Speed | OD | PP | | | |
| 1 | 1 | 1 | 1 | 1 | NRST | I/O | | **X** | | | | | | Reset | | |
| 2 | 2 | 2 | 2 | 2 | PA1/OSCIN | I/O | **X** | X | | | O1 | X | X | **Port A1** | Resonator/ crystal in | |
| 3 | 3 | 3 | 3 | 3 | PA2/OSCOUT | I/O | **X** | X | X | | O1 | X | X | **Port A2** | Resonator/ crystal out | |
| 4 | 4 | 4 | 4 | - | $V_{SSIO\_1}$ | S | | | | | | | | I/O ground | | |
| 5 | 5 | 5 | 5 | 4 | $V_{SS}$ | S | | | | | | | | Digital ground | | |
| 6 | 6 | 6 | 6 | 5 | VCAP | S | | | | | | | | 1.8 V regulator capacitor | | |
| 7 | 7 | 7 | 7 | 6 | $V_{DD}$ | S | | | | | | | | Digital power supply | | |
| 8 | 8 | 8 | 8 | 7 | $V_{DDIO\_1}$ | S | | | | | | | | I/O power supply | | |
| 9 | 9 | 9 | - | - | PA3/TIM2_CH3 | I/O | **X** | X | X | | O1 | X | X | **Port A3** | Timer 2 - channel3 | TIM3_CH1 [AFR1] |
| 10 | 10 | 10 | 9 | - | PA4/UART1_RX (1) | I/O | **X** | X | X | HS | O3 | X | X | **Port A4** | UART1 receive | |
| 11 | 11 | 11 | 10 | - | PA5/UART1_TX | I/O | **X** | X | X | HS | O3 | X | X | **Port A5** | UART1 transmit | |

# 10 Electrical characteristics

## 10.1 Parameter conditions

Unless otherwise specified, all voltages are referred to $V_{SS}$.

### 10.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$ = 25 °C and $T_A = T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3 Σ).

### 10.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD}$ = 5 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2 Σ).

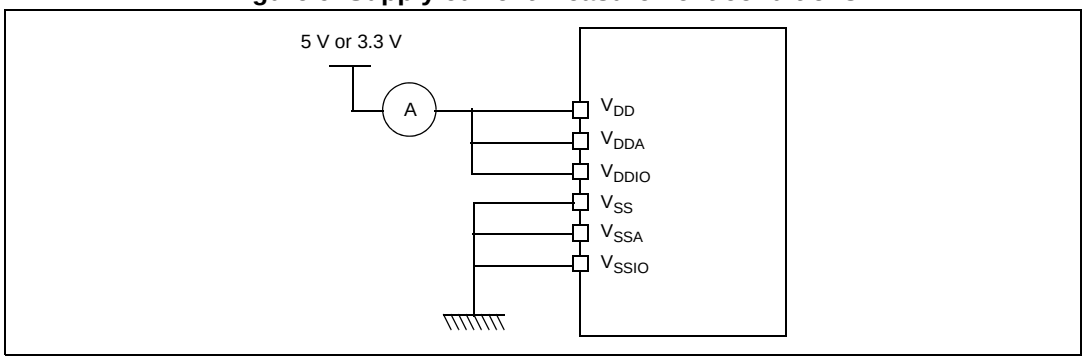
### 10.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 10.1.4 Typical current consumption

For typical current consumption measurements, $V_{DD}$, $V_{DDIO}$ and $V_{DDA}$ are connected together in the configuration shown in *Figure 9*.

**Figure 9. Supply current measurement conditions**



### Total current consumption in active halt mode

**Table 24. Total current consumption in active halt mode at $V_{DD}$ = 5 V, $T_A$ -40 to 85° C**

| Symbol | Parameter | Conditions | | | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|---|
| | | Main voltage regulator (MVR)(2) | Flash mode(3) | Clock source | | | |
| $I_{DD(AH)}$ | Supply current in active halt mode | On | Operating mode | HSE crystal oscillator (16 MHz) | 1000 | | µA |
| | | | | LSI RC oscillator (128 kHz) | 200 | 260 | |
| | | | Power-down mode | HSE crystal oscillator (16 MHz) | 940 | | |
| | | | | LSI RC oscillator (128 kHz) | 140 | | |
| | | Off | Operating mode | LSI RC oscillator 128 kHz) | 68 | | |
| | | | Power-down mode | | 11 | 45 | |

1. Data based on characterization results, not tested in production.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

**Table 25. Total current consumption in active halt mode at $V_{DD}$ = 3.3 V**

| Symbol | Parameter | Conditions | | | Typ(1) | Unit |
|---|---|---|---|---|---|---|
| | | Main voltage regulator (MVR)(2) | Flash mode(3) | Clock source | | |
| $I_{DD(AH)}$ | Supply current in active halt mode | On | Operating mode | HSE crystal osc. (16 MHz) | 600 | µA |
| | | | | LSI RC osc. (128 kHz) | 200 | |
| | | | Power-down mode | HSE crystal osc. (16 MHz) | 540 | |
| | | | | LSI RC osc. (128 kHz) | 140 | |
| | | Off | Operating mode | LSI RC osc. (128 kHz) | 66 | |
| | | | Power-down mode | | 9 | |

1. Data based on characterization results, not tested in production.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

### Current consumption curves

*Figure 14* and *Figure 15* show typical current consumption measured with code executing in RAM.

**Figure 14. Typ. $I_{DD(RUN)}$ vs $V_{DD}$, HSI RC osc, $f_{CPU}$ = 16 MHz**

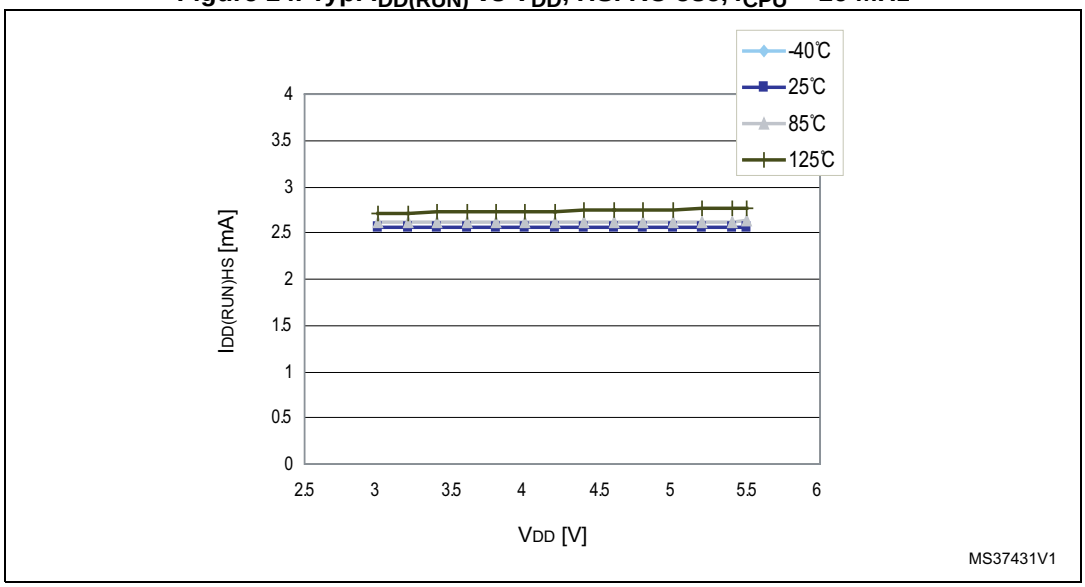



**Figure 15. Typ. $I_{DD(WFI)}$ vs $V_{DD}$, HSI RC osc, $f_{CPU}$ = 16 MHz**

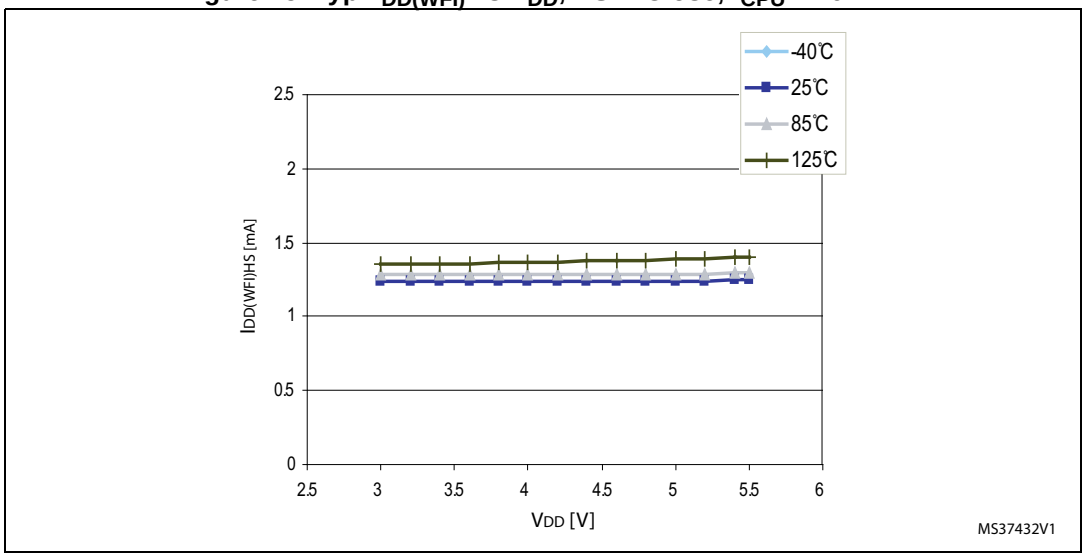
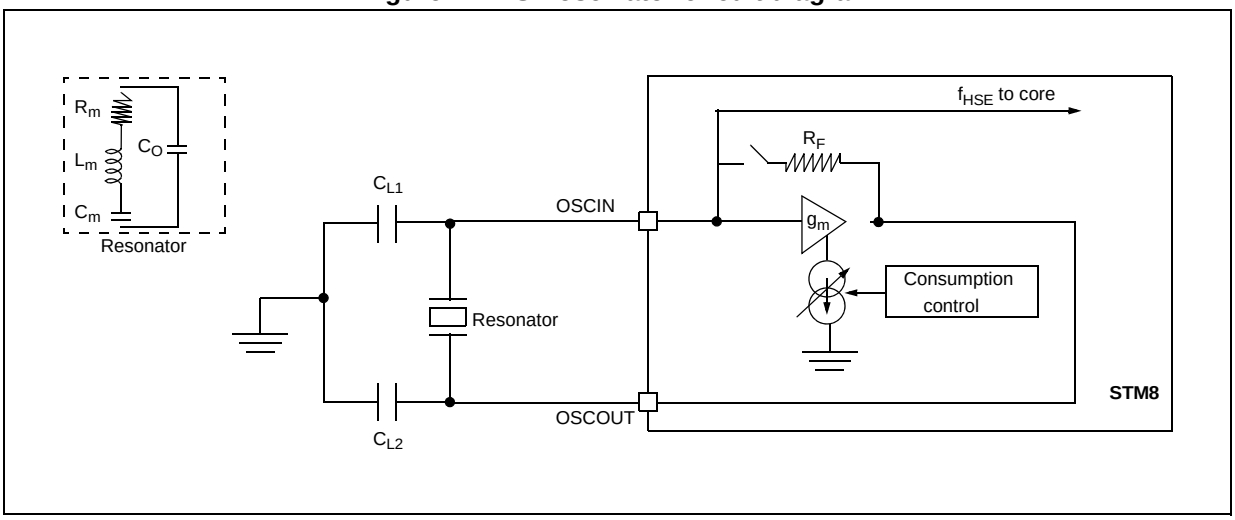


**Table 32. HSE oscillator characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE}$ | External high speed oscillator frequency | | 1 | | 24 | MHz |
| $R_F$ | Feedback resistor | | | 220 | | kΩ |
| $C^{(1)}$ | Recommended load capacitance (2) | | | | 20 | pF |
| $I_{DD(HSE)}$ | HSE oscillator power consumption | C = 20 pF, $f_{OSC}$ = 24 MHz | | | 6 (startup) 2 (stabilized)(3) | mA |
| | | C = 10 pF, $f_{OSC}$ = 24 MHz | | | 6 (startup) 1.5 (stabilized)(3) | |
| $g_m$ | Oscillator transconductance | | 5 | | | mA/V |
| $t_{SU(HSE)}^{(4)}$ | Startup time | $V_{DD}$ is stabilized | | 1 | | ms |

1. C is approximately equivalent to 2 x crystal Cload.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small $R_m$ value. Refer to crystal manufacturer for more details
3. Data based on characterization results, not tested in production.
4. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 24 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

**Figure 17. HSE oscillator circuit diagram**




**HSE oscillator critical $g_m$ formula**

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

$R_m$: Notional resistance (see crystal specification)
$L_m$: Notional inductance (see crystal specification)
$C_m$: Notional capacitance (see crystal specification)
Co: Shunt capacitance (see crystal specification)
$C_{L1}$=$C_{L2}$=C: Grounded external capacitance
$g_m >> g_{mcrit}$

## 10.3.5 Memory characteristics

### RAM and hardware registers

**Table 35. RAM and hardware registers**

| Symbol | Parameter | Conditions | Min | Unit |
|---|---|---|---|---|
| $V_{RM}$ | Data retention mode(1) | Halt mode (or reset) | $V_{IT-max}$(2) | V |

1. Minimum supply voltage without losing data stored in RAM (in halt mode or under reset) or in hardware registers (only in halt mode). Guaranteed by design, not tested in production.
2. Refer to *Table 19 on page 57* for the value of $V_{IT-max}$.

### Flash program memory/data EEPROM memory

General conditions: $T_A$ = -40 to 125 °C.

**Table 36. Flash program memory/data EEPROM memory**

| Symbol | Parameter | Conditions | Min(1) | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage (all modes, execution/write/erase) | $f_{CPU} \leq$ 24 MHz | 2.95 | | 5.5 | V |
| $t_{prog}$ | Standard programming time (including erase) for byte/word/block (1 byte/4 bytes/128 bytes) | | | 6 | 6.6 | ms |
| | Fast programming time for 1 block (128 bytes) | | | 3 | 3.3 | ms |
| $t_{erase}$ | Erase time for 1 block (128 bytes) | | | 3 | 3.3 | ms |
| $N_{RW}$ | Erase/write cycles(2) (program memory) | $T_A$ = 85 °C | 10 k | | | cycles |
| | Erase/write cycles (data memory)(2) | $T_A$ = 125 ° C | 300 k | 1M | | |
| $t_{RET}$ | Data retention (program memory) after 10 k erase/write cycles at $T_A$ = 85 °C | $T_{RET}$ = 55° C | 20 | | | years |
| | Data retention (data memory) after 10 k erase/write cycles at $T_A$ = 85 °C | $T_{RET}$ = 55° C | 20 | | | |
| | Data retention (data memory) after 300k erase/write cycles at $T_A$ = 125 °C | $T_{RET}$ = 85° C | 1 | | | |
| $I_{DD}$ | Supply current (Flash programming or erasing for 1 to 128 bytes) | | | 2 | | mA |

1. Data based on characterization results, not tested in production.
2. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.

**Figure 20. Typical $V_{IL}$ and $V_{IH}$ vs $V_{DD}$ @ 4 temperatures**

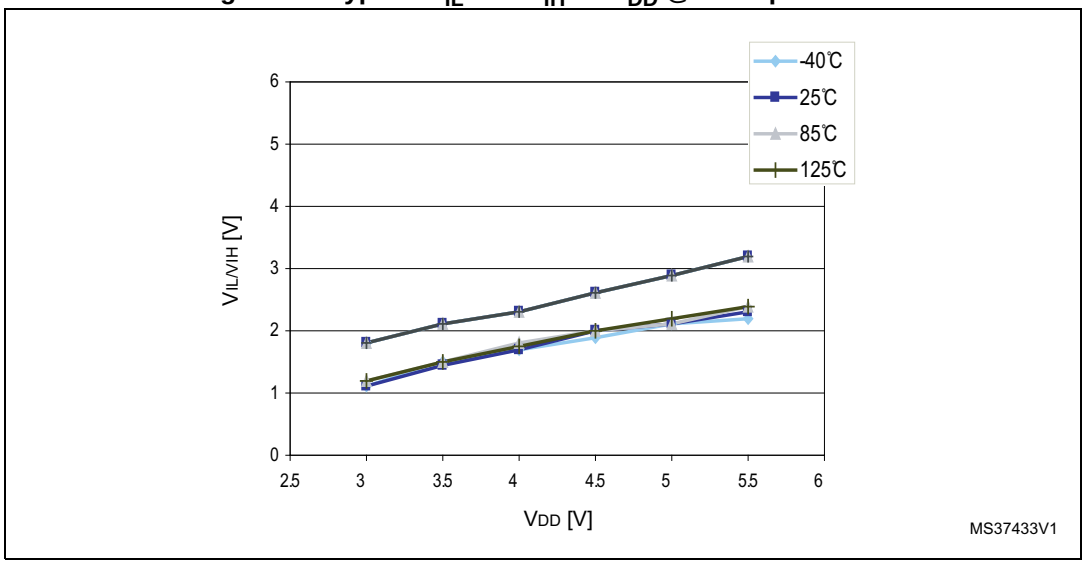
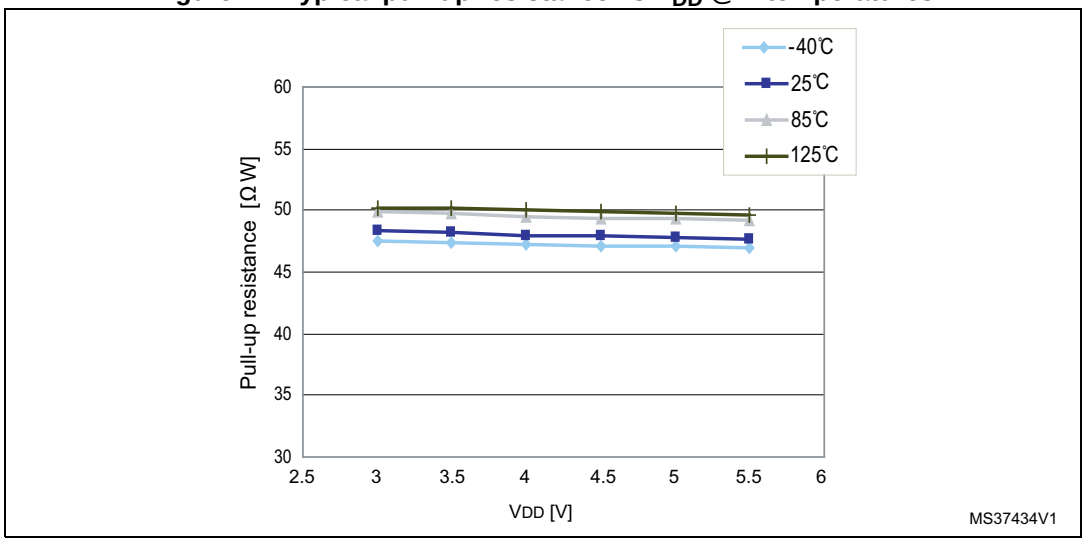



**Figure 21. Typical pull-up resistance vs $V_{DD}$ @ 4 temperatures**



### Typical output level curves

*Figure 24* to *Figure 31* show typical output level curves measured with output on a single pin.

**Figure 23. Typ. $V_{OL}$ @ $V_{DD}$ = 5 V (standard ports)**

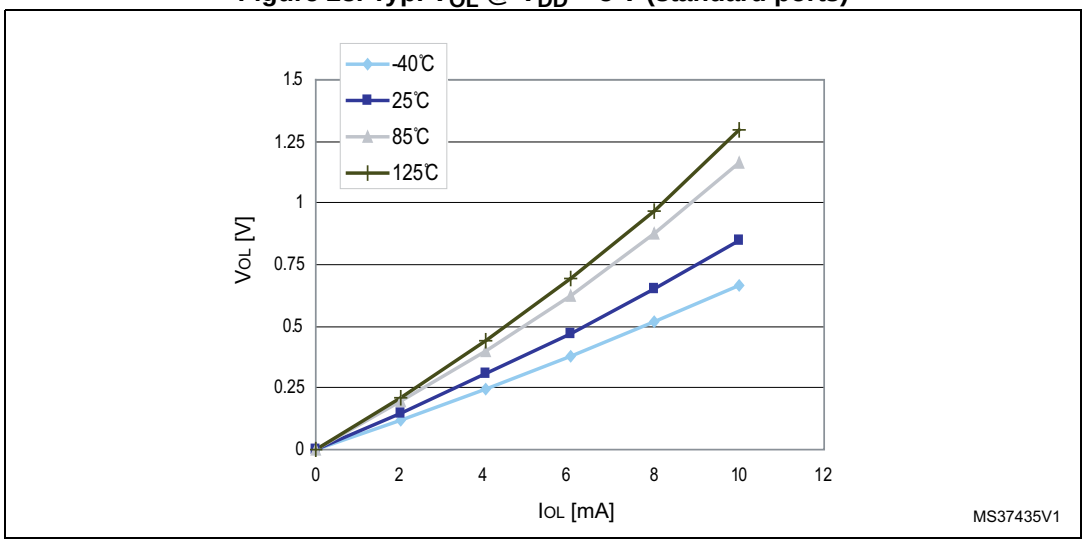



**Figure 24. Typ. $V_{OL}$ @ $V_{DD}$ = 3.3 V (standard ports)**

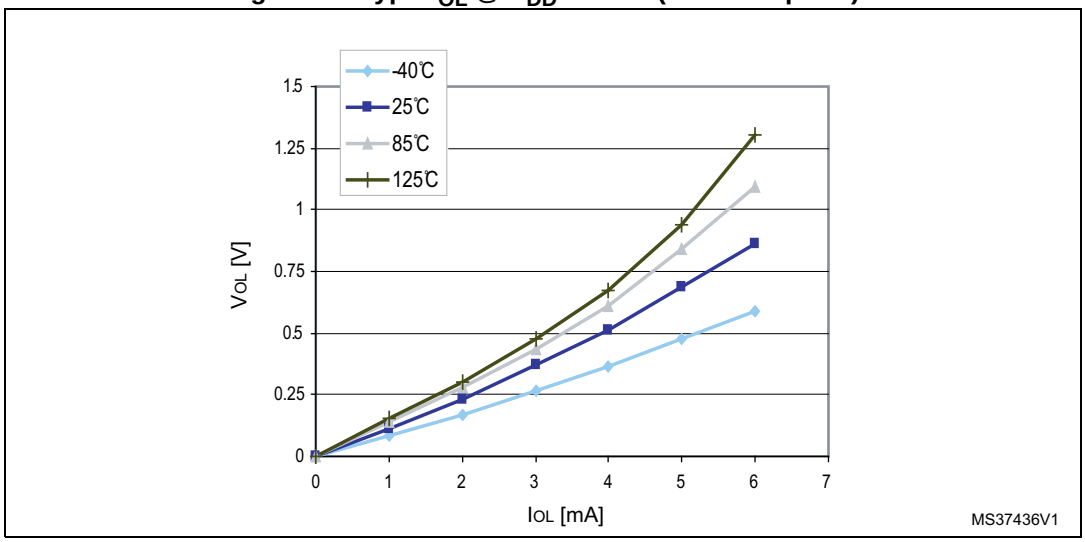


**Figure 27. Typ. $V_{OL}$ @ $V_{DD}$ = 5 V (high sink ports)**

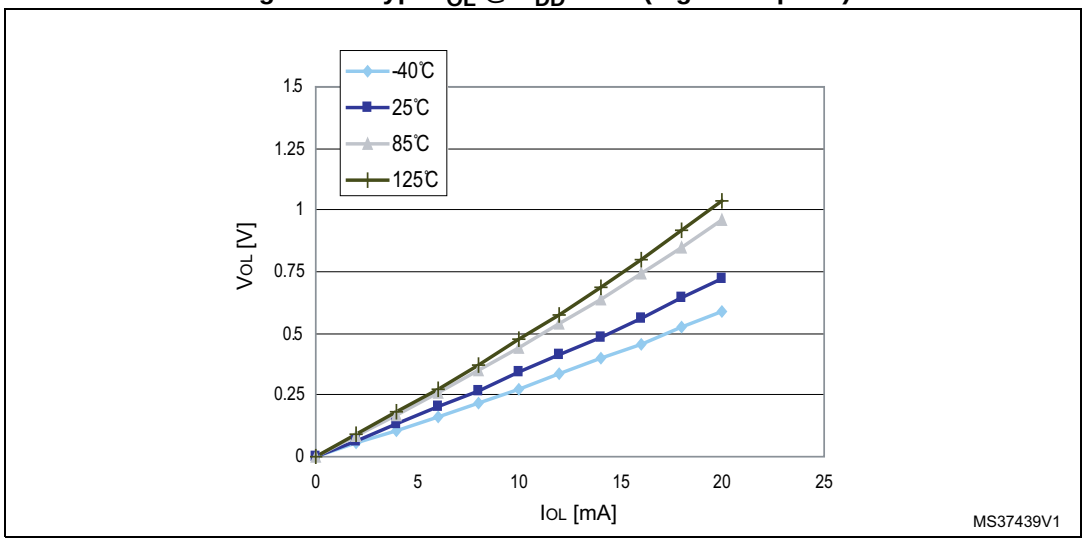



**Figure 28. Typ. $V_{OL}$ @ $V_{DD}$ = 3.3 V (high sink ports)**

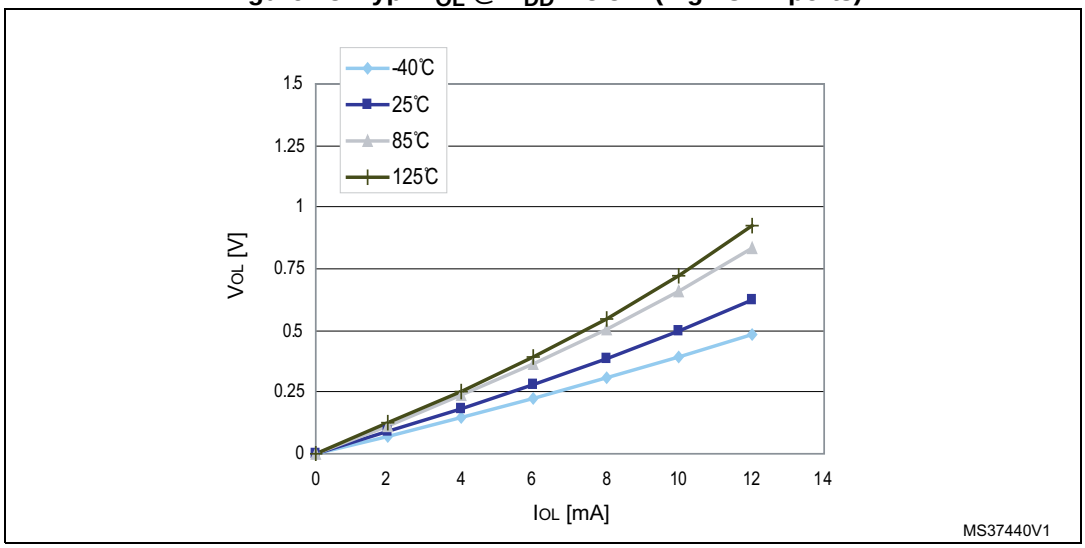


**Figure 31. Typ. $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 5 V (high sink ports)**

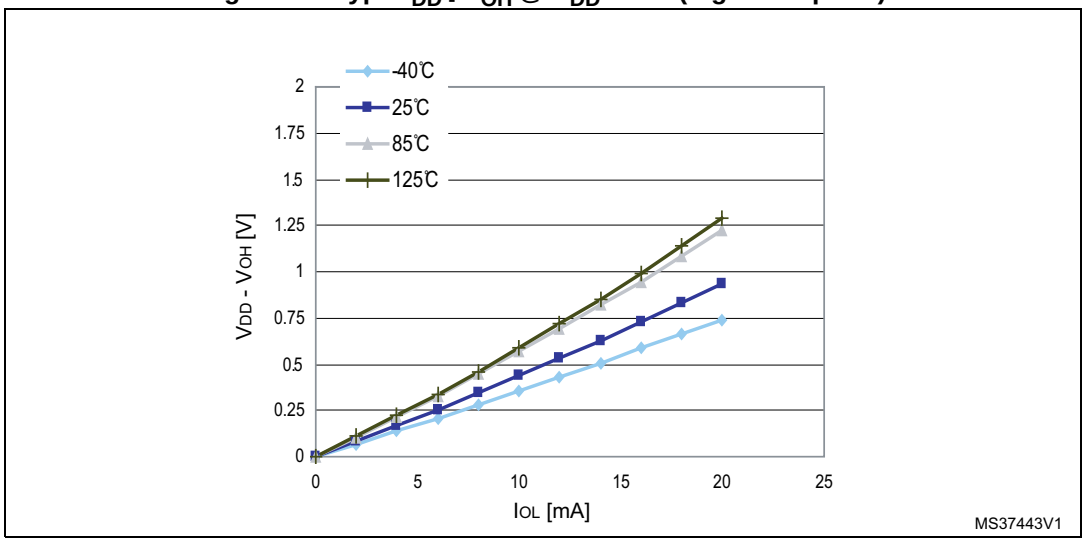



**Figure 32. Typ. $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 3.3 V (high sink ports)**

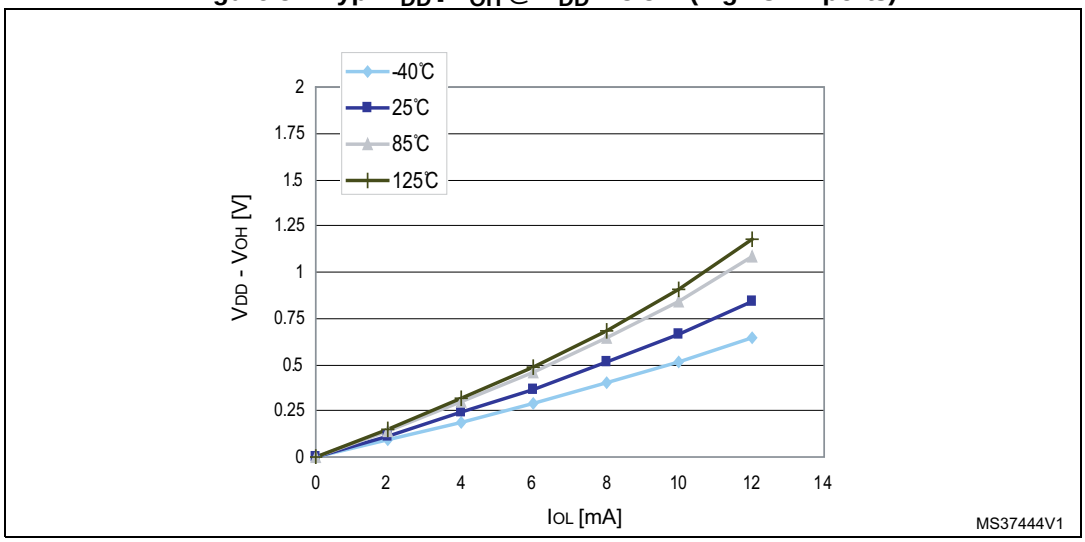
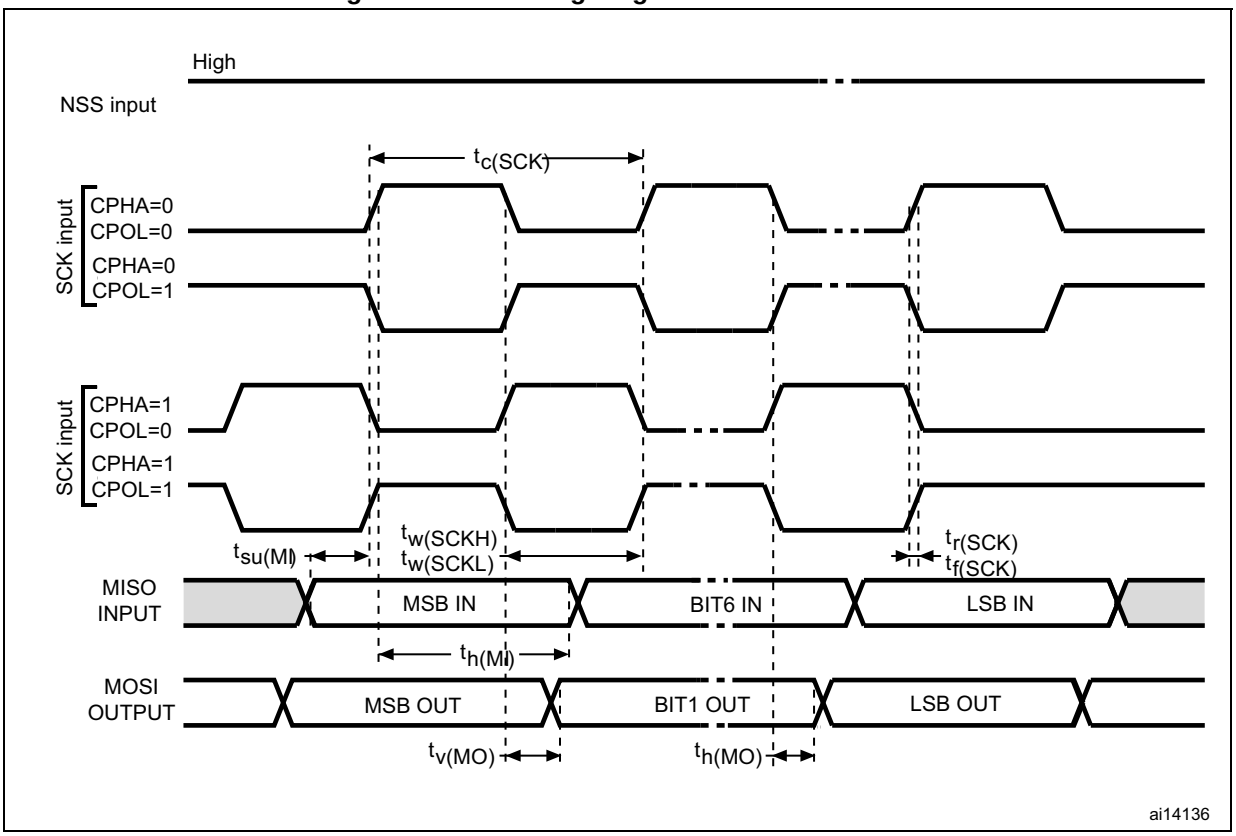


**Figure 39. SPI timing diagram - master mode(1)**




1. Measurement points are done at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

## 11.2 Thermal characteristics

The maximum chip junction temperature ($T_{Jmax}$) must never exceed the values given in *Table 18: General operating conditions on page 56*.

The maximum chip-junction temperature, $T_{Jmax}$, in degrees Celsius, may be calculated using the following equation:

$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$

Where:

- $T_{Amax}$ is the maximum ambient temperature in °C
- $\Theta_{JA}$ is the package junction-to-ambient thermal resistance in ° C/W
- $P_{Dmax}$ is the sum of $P_{INTmax}$ and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- $P_{INTmax}$ is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins, where: $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$, and taking account of the actual $V_{OL}/I_{OL}$ and $V_{OH}/I_{OH}$ of the I/Os at low and high level in the application.

**Table 57. Thermal characteristics(1)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance junction-ambient LQFP 80 - 14 x 14 mm | 38 | °C/W |
| $\Theta_{JA}$ | Thermal resistance junction-ambient LQFP 64 - 14 x 14 mm | 45 | °C/W |
| $\Theta_{JA}$ | Thermal resistance junction-ambient LQFP 64 - 10 x 10 mm | 46 | °C/W |
| $\Theta_{JA}$ | Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm | 57 | °C/W |
| $\Theta_{JA}$ | Thermal resistance junction-ambient LQFP 44 - 10 x 10 mm | 54 | °C/W |
| $\Theta_{JA}$ | Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm | 60 | °C/W |

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

### 11.2.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

### 11.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see *Figure 59: STM8S207xx/208xx performance line ordering information scheme(1) on page 112*).

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

- Maximum ambient temperature $T_{Amax}$= 82 °C (measured according to JESD51-2)
- $I_{DDmax}$ = 15 mA, $V_{DD}$ = 5.5 V
- Maximum eight standard I/Os used at the same time in output at low level with $I_{OL}$ = 10 mA, $V_{OL}$= 2 V
- Maximum four high sink I/Os used at the same time in output at low level with $I_{OL}$ = 20 mA, $V_{OL}$= 1.5 V
- Maximum two true open drain I/Os used at the same time in output at low level with $I_{OL}$ = 20 mA, $V_{OL}$= 2 V

  $P_{INTmax}$ = 15 mA x 5.5 V = 82.5 mW

  $P_{IOmax}$ = (10 mA x 2 V x 8) + (20 mA x 2 V x 2) + (20 mA x 1.5 V x 4) = 360 mW

  This gives: $P_{INTmax}$ = 82.5 mW and $P_{IOmax}$ 360 mW:

  $P_{Dmax}$ = 82.5 mW + 360 mW

  Thus: $P_{Dmax}$ = 443 mW

Using the values obtained in *Table 57: Thermal characteristics on page 108* $T_{Jmax}$ is calculated as follows for LQFP64 10 x 10 mm = 46 °C/W:

$T_{Jmax}$ = 82 °C + (46 °C/W x 443 mW) = 82 °C + 20 °C = 102 °C

This is within the range of the suffix 6 version parts (-40 < $T_J$ < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6.