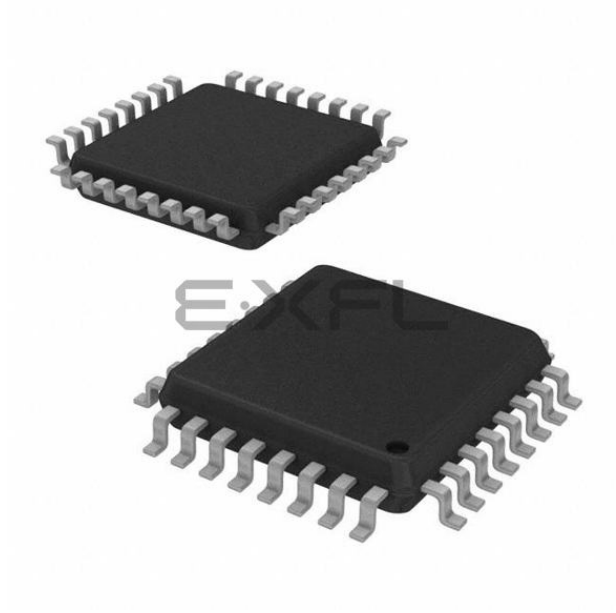

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s207k8t6ctr

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2 Description

The STM8S20xxx performance line 8-bit microcontrollers offer from 32 to 128 Kbytes Flash program memory. They are referred to as high-density devices in the STM8S microcontroller family reference manual.

All STM8S20xxx devices provide the following benefits: reduced system cost, performance robustness, short development cycles, and product longevity.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 k write/erase cycles and a high system integration level with internal clock oscillators, watchdog, and brown-out reset.

Device performance is ensured by 20 MIPS at 24 MHz CPU clock frequency and enhanced characteristics which include robust I/O, independent watchdogs (with a separate clock source), and a clock security system.

Short development cycles are guaranteed due to application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals. Full documentation is offered with a wide choice of development tools.

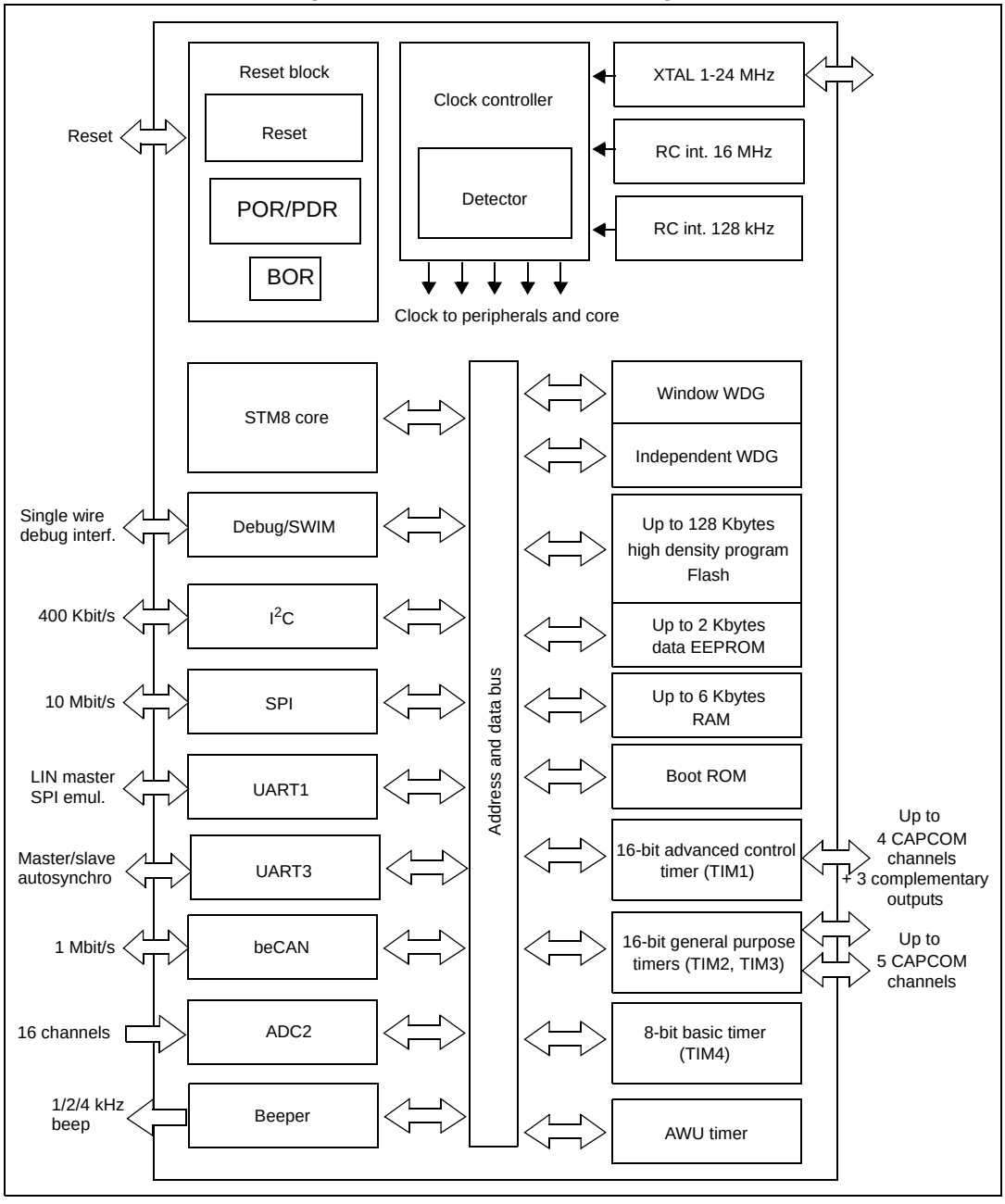
Product longevity is ensured in the STM8S family thanks to their advanced core which is made in a state-of-the art technology for applications with 2.95 V to 5.5 V operating supply.

Table 2. STM8S20xxx performance line features

Device	Pin count	Max. number of GPIOs (I/O)	Ext. interrupt pins	Timer CAPCOM channels	Timer complementary outputs	A/D converter channels	High sink I/Os	High density Flash program memory (bytes)	Data EEPROM (bytes	RAM (bytes)	beCAN interface
STM8S207MB	80	68	37	9	3	16	18	128 K	2048	6 K	
STM8S207M8	80	68	37	9	3	16	18	64 K	2048	6 K	
STM8S207RB	64	52	36	9	3	16	16	128 K	2048	6 K	
STM8S207R8	64	52	36	9	3	16	16	64 K	1536	6 K	
STM8S207R6	64	52	36	9	3	16	16	32 K	1024	6 K	
STM8S207CB	48	38	35	9	3	10	16	128 K	2048	6 K	
STM8S207C8	48	38	35	9	3	10	16	64 K	1536	6 K	No
STM8S207C6	48	38	35	9	3	10	16	32 K	1024	6 K	
STM8S207SB	44	34	31	8	3	9	15	128 K	1536	6 K	
STM8S207S8	44	34	31	8	3	9	15	64 K	1536	6 K	
STM8S207S6	44	34	31	8	3	9	15	32 K	1024	6 K	
STM8S207K8	32	25	23	8	3	7	12	64 K	1024	6 K	
STM8S207K6	32	25	23	8	3	7	12	32 K	1024	6 K	
STM8S208MB	80	68	37	9	3	16	18	128 K	2048	6 K	
STM8S208RB	64	52	37	9	3	16	16	128 K	2048	6 K	
STM8S208R8	64	52	37	9	3	16	16	64 K	2048	6 K	
STM8S208R6	64	52	37	9	3	16	16	32 K	2048	6 K	
STM8S208CB	48	38	35	9	3	10	16	128 K	2048	6 K	Yes
STM8S208C8	48	38	35	9	3	10	16	64 K	2048	6 K	
STM8S208C6	48	38	35	9	3	10	16	32 K	2048	6 K	
STM8S208SB	44	34	31	8	3	9	15	128 K	1536	6 K	
STM8S208S8	44	34	31	8	3	9	15	64 K	1536	6 K	
STM8S208S6	44	34	31	8	3	9	15	32 K	1536	6 K	

3 Block diagram

Figure 1. STM8S20xxx block diagram



1. Legend:
ADC: Analog-to-digital converter
beCAN: Controller area network
BOR: Brownout reset
I²C: Inter-integrated circuit multimaster interface
Independent WDG: Independent watchdog
POR/PDR: Power on reset / power down reset
SPI: Serial peripheral interface
SWIM: Single wire interface module
UART: Universal asynchronous receiver transmitter
Window WDG: Window watchdog

4.5 Clock controller

The clock controller distributes the system clock (f_{MASTER}) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- ***Clock prescaler*:** To get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- ***Safe clock switching*:** Clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- ***Clock management*:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- ***Master clock sources*:** Four different clock sources can be used to drive the master clock:
  - 1-24 MHz high-speed external crystal (HSE)
  - Up to 24 MHz high-speed user-external clock (HSE user-ext)
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
- ***Startup clock*:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- ***Clock security system (CSS)*:** This feature can be enabled by software. If an HSE clock failure occurs, the internal RC (16 MHz/8) is automatically selected by the CSS and an interrupt can optionally be generated.
- ***Configurable main clock output (CCO)*:** This outputs an external clock for use by the application.

Table 3. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers

Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock
PCKEN17	TIM1	PCKEN13	UART3	PCKEN27	beCAN	PCKEN23	ADC
PCKEN16	TIM3	PCKEN12	UART1	PCKEN26	Reserved	PCKEN22	AWU
PCKEN15	TIM2	PCKEN11	SPI	PCKEN25	Reserved	PCKEN21	Reserved
PCKEN14	TIM4	PCKEN10	I^2C	PCKEN24	Reserved	PCKEN20	Reserved

Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure

The IWDG time base spans from 60 µs to 1 s.

4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock
- LSI clock can be internally connected to TIM3 input capture channel 1 for calibration

4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

4.10 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signals
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

4.11 TIM2, TIM3 - 16-bit general purpose timers

- 16-bit autoreload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1…32768
- Timers with 3 or 2 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 2 or 3 x input capture/output compare, 1 x overflow/update

4.12 TIM4 - 8-bit basic timer

- 8-bit autoreload, adjustable prescaler ratio to any power of 2 from 1 to 128
- Clock source: CPU clock
- Interrupt source: 1 x overflow/update

Table 4. TIM timer features

Timer	Counter size (bits)	Prescaler	Counting mode	CAPCOM channels	Complem. outputs	Ext. trigger	Timer synchr-onization/ chaining
TIM1	16	Any integer from 1 to 65536	Up/down	4	3	Yes	No
TIM2	16	Any power of 2 from 1 to 32768	Up	3	0	No	
TIM3	16	Any power of 2 from 1 to 32768	Up	2	0	No	
TIM4	8	Any power of 2 from 1 to 128	Up	0	0	No	

4.13 Analog-to-digital converter (ADC2)

STM8S20xxx performance line products contain a 10-bit successive approximation A/D converter (ADC2) with up to 16 multiplexed input channels and the following main features:

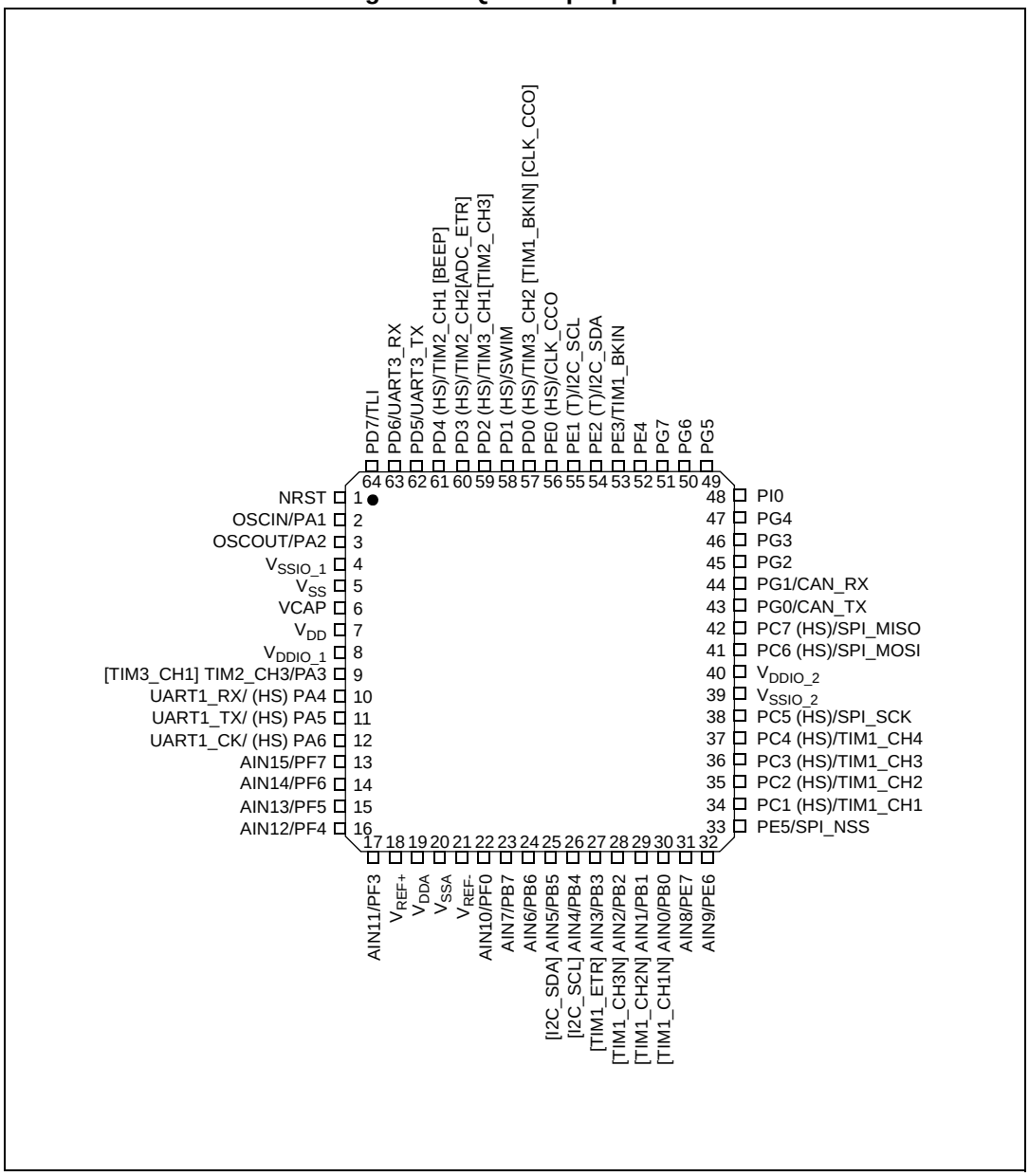
- Input voltage range: 0 to V_{DDA}
- Dedicated voltage reference (VREF) pins available on 80 and 64-pin devices
- Conversion time: 14 clock cycles
- Single and continuous modes
- External trigger input
- Trigger from TIM1 TRGO
- End of conversion (EOC) interrupt

4.14 Communication interfaces

The following communication interfaces are implemented:

- UART1: Full feature UART, SPI emulation, LIN2.1 master capability, Smartcard mode, IrDA mode, single wire mode.
- UART3: Full feature UART, LIN2.1 master/slave capability
- SPI: Full and half-duplex, 10 Mbit/s
- I^2C: Up to 400 Kbit/s
- beCAN (rev. 2.0A,B) - 3 Tx mailboxes - up to 1 Mbit/s

Figure 4. LQFP 64-pin pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
4. CAN_RX and CAN_TX is available on STM8S208xx devices only.

Table 8. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0x00
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0x00
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0x00
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00
0x00 501E	Port G	PG_ODR	Port G data output latch register	0x00
0x00 501F		PG_IDR	Port G input pin value register	0x00
0x00 5020		PG_DDR	Port G data direction register	0x00
0x00 5021		PG_CR1	Port G control register 1	0x00
0x00 5022		PG_CR2	Port G control register 2	0x00
0x00 5023	Port H	PH_ODR	Port H data output latch register	0x00
0x00 5024		PH_IDR	Port H input pin value register	0x00
0x00 5025		PH_DDR	Port H data direction register	0x00
0x00 5026		PH_CR1	Port H control register 1	0x00
0x00 5027		PH_CR2	Port H control register 2	0x00
0x00 5028	Port I	PI_ODR	Port I data output latch register	0x00
0x00 5029		PI_IDR	Port I input pin value register	0x00
0x00 502A		PI_DDR	Port I data direction register	0x00
0x00 502B		PI_CR1	Port I control register 1	0x00
0x00 502C		PI_CR2	Port I control register 2	0x00

8 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Except for the ROP (read-out protection) byte, each option byte has to be stored twice, in a regular form (OPTx) and a complemented one (NOPTx) for redundancy.

Option bytes can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in *Table 12: Option bytes* below. Option bytes can also be modified 'on the fly' by the application in IAP mode, except the ROP option that can only be modified in ICP mode (via SWIM).

Refer to the STM8S Flash programming manual (PM0051) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

Table 12. Option bytes

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
4800h	Read-out protection (ROP)	OPT0	ROP[7:0]								00h
4801h	User boot code (UBC)	OPT1	UBC[7:0]								00h
4802h		NOPT1	NUBC[7:0]								FFh
4803h	Alternate function remapping (AFR)	OPT2	AFR7	AFR6	AFR5	AFR4	AFR3	AFR2	AFR1	AFR0	00h
4804h		NOPT2	NAFR7	NAFR6	NAFR5	NAFR4	NAFR3	NAFR2	NAFR1	NAFR0	FFh
4805h	Watchdog option	OPT3	Reserved				LSI_EN	IWDG_HW	WWDG_HW	WWDG_HALT	00h
4806h		NOPT3	Reserved				NLSI_EN	NIWDG_HW	NWWDG_HW	NWWDG_HALT	FFh
4807h	Clock option	OPT4	Reserved				EXTCLK	CKAWUSEL	PRSC1	PRSC0	00h
4808h		NOPT4	Reserved				NEXTCLK	NCKAWUSEL	NPRSC1	NPRSC0	FFh
4809h	HSE clock startup	OPT5	HSECNT[7:0]								00h
480Ah		NOPT5	NHSECNT[7:0]								FFh
480Bh	Reserved	OPT6	Reserved								00h
480Ch		NOPT6	Reserved								FFh
480Dh	Flash wait states	OPT7	Reserved							Wait state	00h
480Eh		NOPT7	Reserved							Nwait state	FFh
487Eh	Bootloader	OPTBL	BL[7:0]								00h
487Fh		NOPTBL	NBL[7:0]								FFh

Table 13. Option byte description (continued)

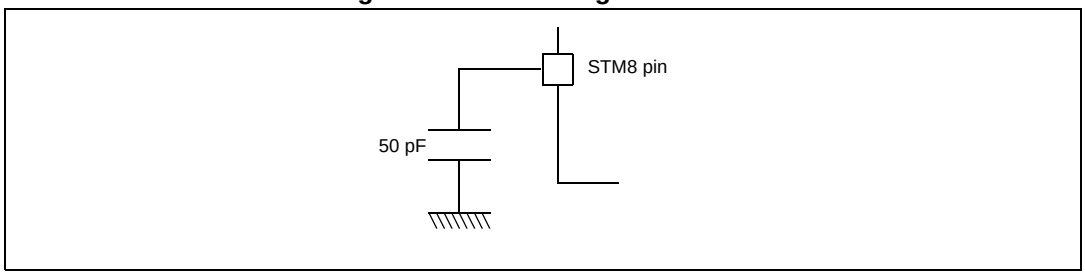
Option byte no.	Description
OPTBL	**BL[7:0]** *Bootloader option byte* For STM8S products, this option is checked by the boot ROM code after reset. Depending on the content of addresses 0x487E, 0x487F, and 0x8000 (reset vector), the CPU jumps to the bootloader or to the reset vector. Refer to the UM0560 (STM8L/S bootloader manual) for more details. For STM8L products, the bootloader option bytes are on addresses 0xXXXX and 0xXXXX+1 (2 bytes). These option bytes control whether the bootloader is active or not. For more details, refer to the UM0560 (STM8L/S bootloader manual) for more details.

10.1.5 Pin loading conditions

10.1.6 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

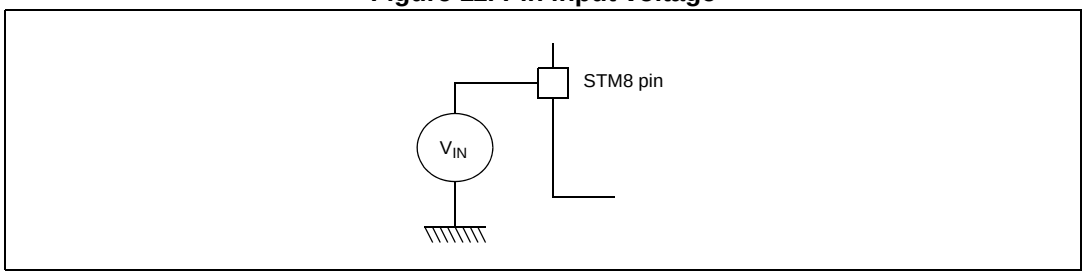
Figure 10. Pin loading conditions



10.1.7 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 11. Pin input voltage



10.3.2 Supply current characteristics

The current consumption is measured as described in *Figure 9 on page 52*.

Total current consumption in run mode

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled (clock stopped by Peripheral Clock Gating registers) except if explicitly mentioned.
- When the MCU is clocked at 24 MHz, $T_A \leq 105$ °C and the WAITSTATE option bit is set.

Subject to general operating conditions for V_{DD} and T_A.

Table 20. Total current consumption with code execution in run mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$	Supply current in run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 24 MHz, $T_A \leq$ 105 °C	HSE crystal osc. (24 MHz)	4.4		mA
			HSE user ext. clock (24 MHz)	3.7	7.3(1)	
		$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	3.3		
			HSE user ext. clock (16 MHz)	2.7	5.8	
			HSI RC osc. (16 MHz)	2.5	3.4	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSE user ext. clock (16 MHz)	1.2	4.1(1)	
			HSI RC osc. (16 MHz)	1.0	1.3(1)	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.55		
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.45		
	Supply current in run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 24 MHz, $T_A \leq$ 105 °C	HSE crystal osc. (24 MHz)	11.4		
			HSE user ext. clock (24 MHz)	10.8	18(1)	
		$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	9.0		
			HSE user ext. clock (16 MHz)	8.2	15.2(1)	
			HSI RC osc.(16 MHz)	8.1	13.2(1)	
		$f_{CPU} = f_{MASTER}$ = 2 MHz.	HSI RC osc. (16 MHz/8)(2)	1.5		
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	1.1		
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.6		
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.55		

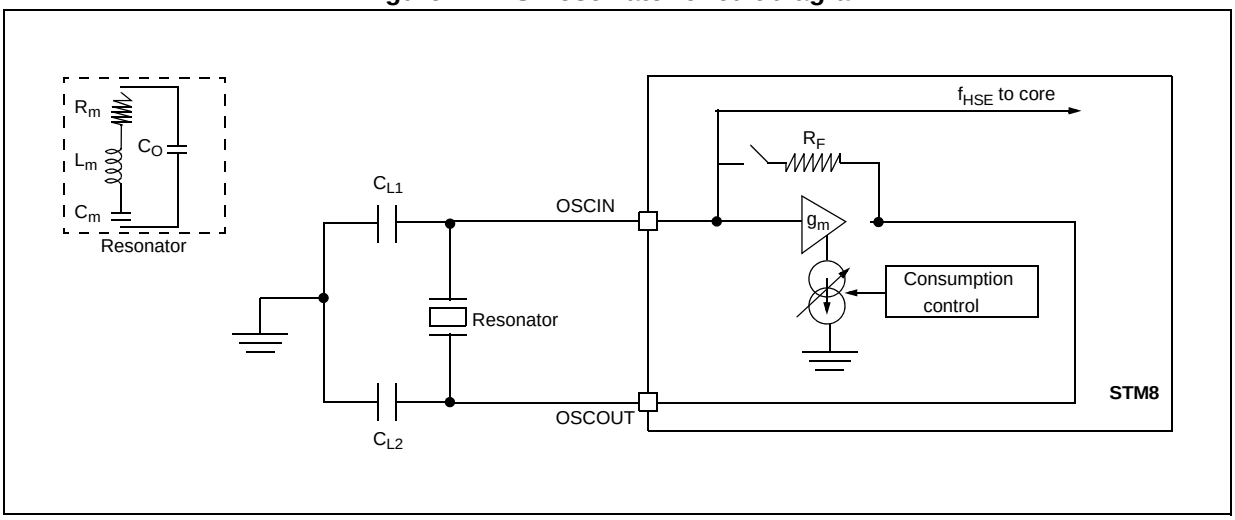
1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Table 32. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	External high speed oscillator frequency		1		24	MHz
R_F	Feedback resistor			220		kΩ
$C^{(1)}$	Recommended load capacitance (2)				20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 24 MHz			6 (startup) 2 (stabilized)(3)	mA
		C = 10 pF, f_{OSC} = 24 MHz			6 (startup) 1.5 (stabilized)(3)	
g_m	Oscillator transconductance		5			mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized		1		ms

1. C is approximately equivalent to 2 x crystal Cload.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Data based on characterization results, not tested in production.
4. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 24 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 17. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Notional resistance (see crystal specification)
L_m: Notional inductance (see crystal specification)
C_m: Notional capacitance (see crystal specification)
Co: Shunt capacitance (see crystal specification)
C_{L1}=C_{L2}=C: Grounded external capacitance
$g_m >> g_{mcrit}$

10.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A. f_{HSE}

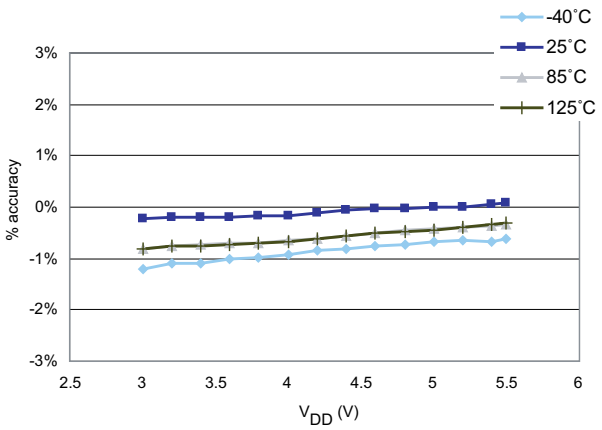
High speed internal RC oscillator (HSI)

Table 33. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			16		MHz
ACC_{HSI}	Accuracy of HSI oscillator	Trimmed by the CLK_HSITRIMR register for given V_{DD} and T_A conditions	-1.0(1)		1.0	%
	Accuracy of HSI oscillator (factory calibrated)	V_{DD} = 5 V, T_A = 25 °C	-1.5		1.5	
		V_{DD} = 5 V, 25 °C ≤ T_A ≤ 85 °C	-2.2		2.2	
		2.95 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C	-3.0(2)		3.0(2)	
$t_{su(HSI)}$	HSI oscillator wakeup time including calibration				1.0(1)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			170	250(2)	µA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production

Figure 18. Typical HSI frequency variation vs V_{DD} at 4 temperatures



10.3.5 Memory characteristics

RAM and hardware registers

Table 35. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Unit
V_{RM}	Data retention mode(1)	Halt mode (or reset)	V_{IT-max}(2)	V

1. Minimum supply voltage without losing data stored in RAM (in halt mode or under reset) or in hardware registers (only in halt mode). Guaranteed by design, not tested in production.
2. Refer to *Table 19 on page 57* for the value of V_{IT-max}.

Flash program memory/data EEPROM memory

General conditions: T_A = -40 to 125 °C.

Table 36. Flash program memory/data EEPROM memory

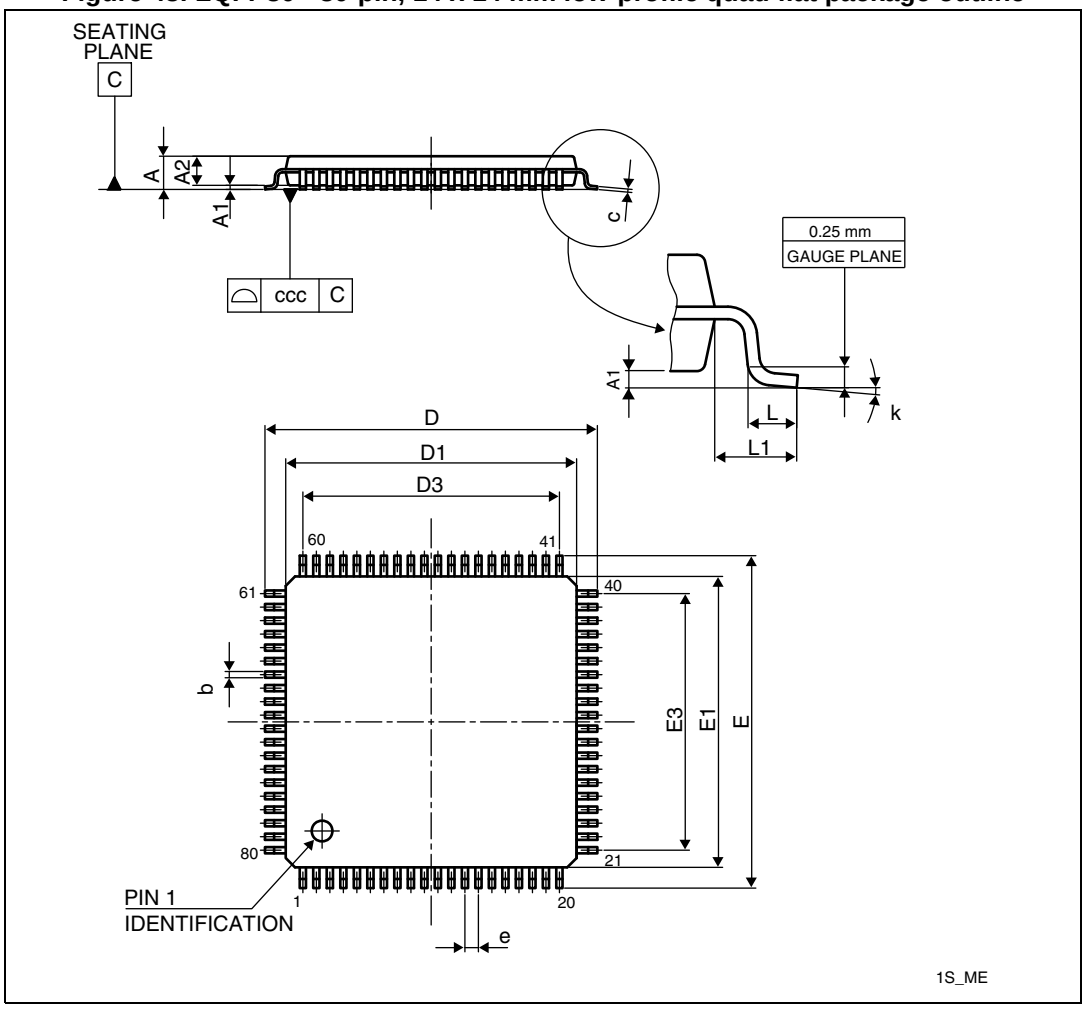
Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
V_{DD}	Operating voltage (all modes, execution/write/erase)	$f_{CPU} \leq$ 24 MHz	2.95		5.5	V
t_{prog}	Standard programming time (including erase) for byte/word/block (1 byte/4 bytes/128 bytes)			6	6.6	ms
	Fast programming time for 1 block (128 bytes)			3	3.3	ms
t_{erase}	Erase time for 1 block (128 bytes)			3	3.3	ms
N_{RW}	Erase/write cycles(2) (program memory)	T_A = 85 °C	10 k			cycles
	Erase/write cycles (data memory)(2)	T_A = 125 ° C	300 k	1M		
t_{RET}	Data retention (program memory) after 10 k erase/write cycles at T_A = 85 °C	T_{RET} = 55° C	20			years
	Data retention (data memory) after 10 k erase/write cycles at T_A = 85 °C	T_{RET} = 55° C	20			
	Data retention (data memory) after 300k erase/write cycles at T_A = 125 °C	T_{RET} = 85° C	1			
I_{DD}	Supply current (Flash programming or erasing for 1 to 128 bytes)			2		mA

1. Data based on characterization results, not tested in production.
2. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.

11.1 Package information

11.1.1 LQFP80 package information

Figure 43. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

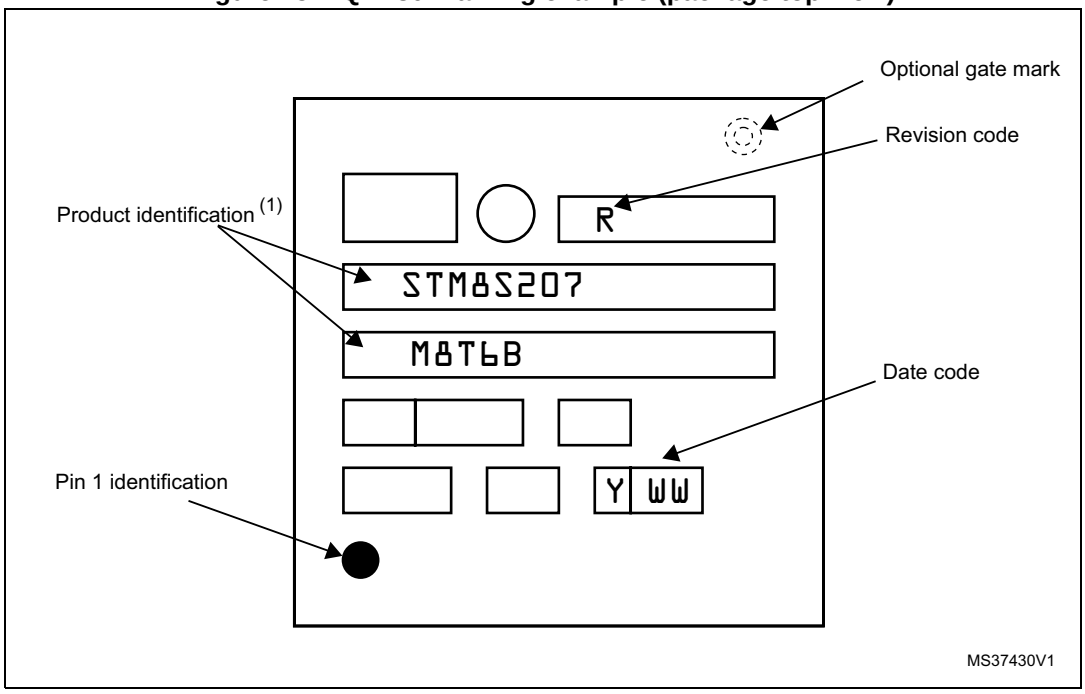
Table 51. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package mechanical data(1)

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.220	0.320	0.380	0.0087	0.0126	0.0150
c	0.090	-	0.200	0.0035	-	0.0079

Device marking

The following figure shows the marking for the LQFP80 package.

Figure 45. LQFP80 marking example (package top view)



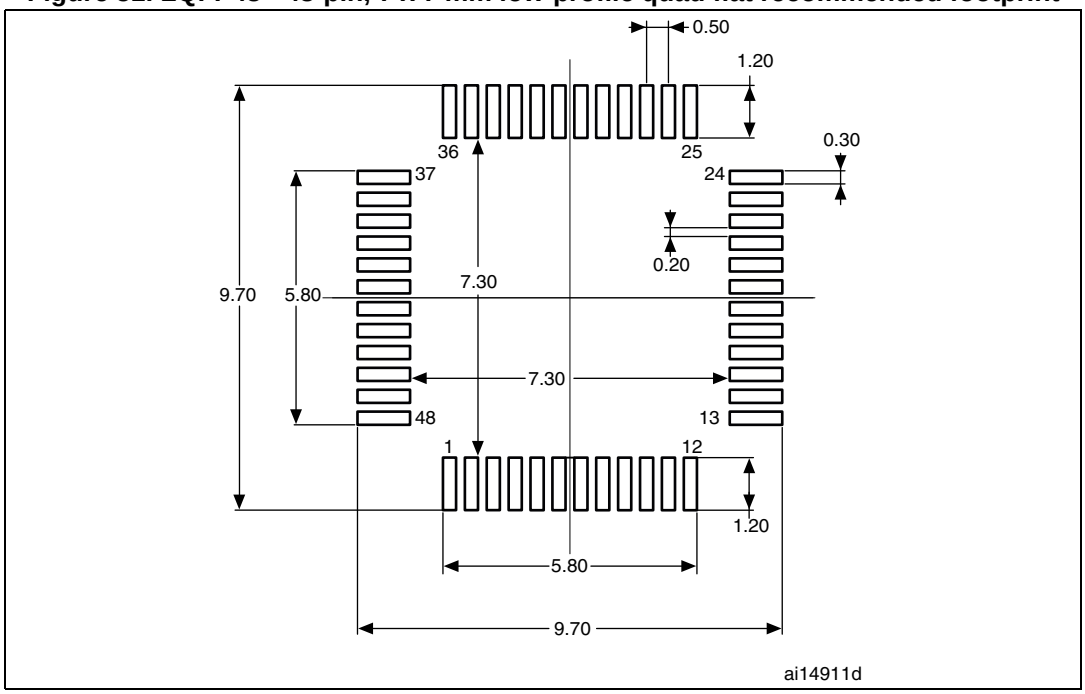
1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 54. LQFP48 - 48-pin, 7x 7 mm low-profile quad flat package mechanical (continued)

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal places.

Figure 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint



1. Dimensions are expressed in millimeters.

11.1.4 LQFP44 package information

Figure 53. LQFP44 - 44-pin, 10 x 10 mm low-profile quad flat package outline