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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	52
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s207r6t6tr

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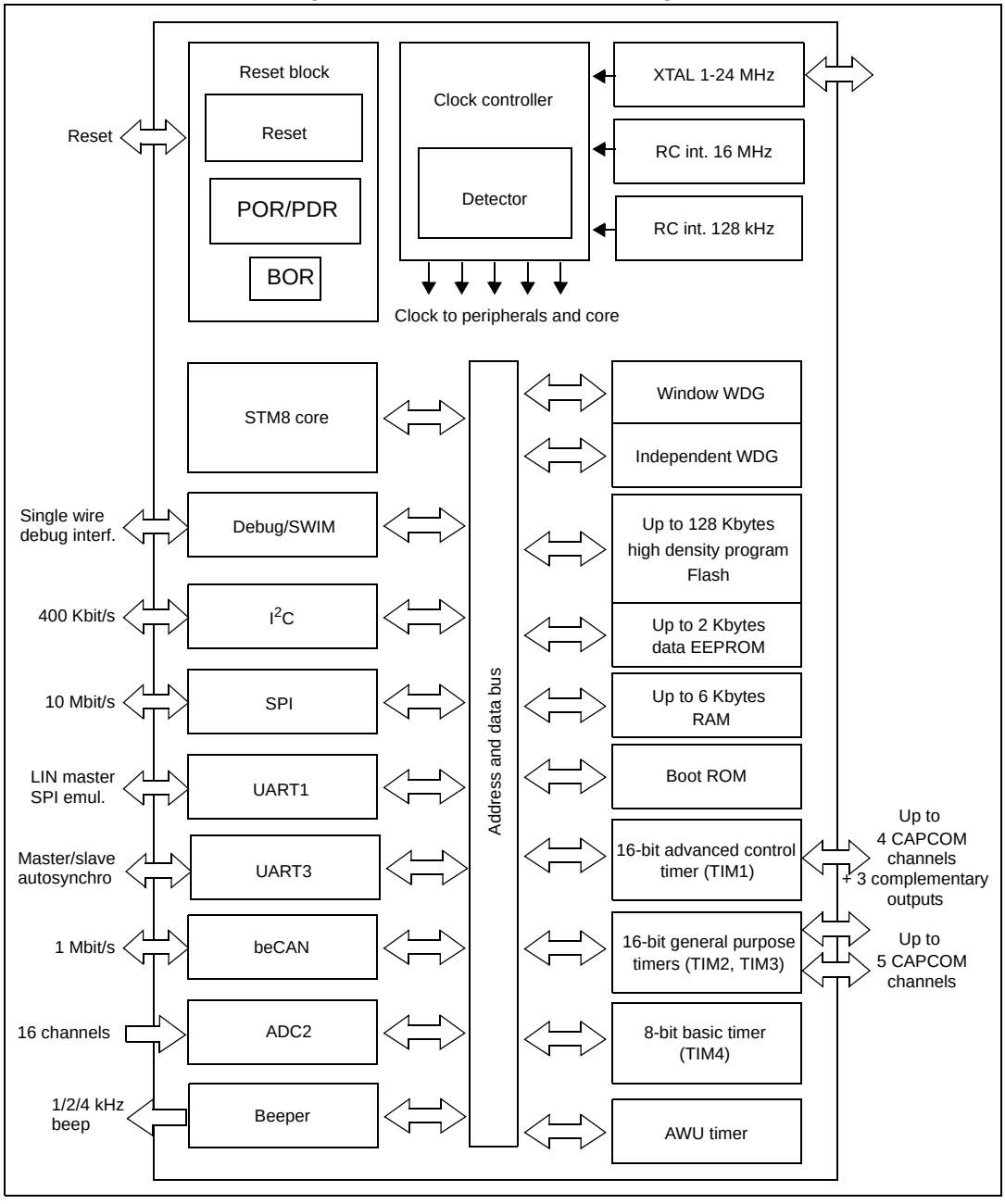
1 Introduction

This datasheet contains the description of the STM8S20xxx features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8S microcontroller memory, registers and peripherals, please refer to the STM8S microcontroller family reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8S Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

3 Block diagram

Figure 1. STM8S20xxx block diagram



1. Legend:
ADC: Analog-to-digital converter
beCAN: Controller area network
BOR: Brownout reset
I²C: Inter-integrated circuit multimaster interface
Independent WDG: Independent watchdog
POR/PDR: Power on reset / power down reset
SPI: Serial peripheral interface
SWIM: Single wire interface module
UART: Universal asynchronous receiver transmitter
Window WDG: Window watchdog

4.12 TIM4 - 8-bit basic timer

- 8-bit autoreload, adjustable prescaler ratio to any power of 2 from 1 to 128
- Clock source: CPU clock
- Interrupt source: 1 x overflow/update

Table 4. TIM timer features

Timer	Counter size (bits)	Prescaler	Counting mode	CAPCOM channels	Complem. outputs	Ext. trigger	Timer synchr-onization/ chaining
TIM1	16	Any integer from 1 to 65536	Up/down	4	3	Yes	No
TIM2	16	Any power of 2 from 1 to 32768	Up	3	0	No	
TIM3	16	Any power of 2 from 1 to 32768	Up	2	0	No	
TIM4	8	Any power of 2 from 1 to 128	Up	0	0	No	

4.13 Analog-to-digital converter (ADC2)

STM8S20xxx performance line products contain a 10-bit successive approximation A/D converter (ADC2) with up to 16 multiplexed input channels and the following main features:

- Input voltage range: 0 to V_{DDA}
- Dedicated voltage reference (VREF) pins available on 80 and 64-pin devices
- Conversion time: 14 clock cycles
- Single and continuous modes
- External trigger input
- Trigger from TIM1 TRGO
- End of conversion (EOC) interrupt

4.14 Communication interfaces

The following communication interfaces are implemented:

- UART1: Full feature UART, SPI emulation, LIN2.1 master capability, Smartcard mode, IrDA mode, single wire mode.
- UART3: Full feature UART, LIN2.1 master/slave capability
- SPI: Full and half-duplex, 10 Mbit/s
- I^2C: Up to 400 Kbit/s
- beCAN (rev. 2.0A,B) - 3 Tx mailboxes - up to 1 Mbit/s

Table 6. Pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	LQFP44	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
12	12	12	11	-	PA6/UART1_CK	I/O	**X**	X	X	HS	O3	X	X	**Port A6**	UART1 synchronous clock	
13	-	-	-	-	PH0	I/O	**X**	X		HS	O3	X	X	**Port H0**		
14	-	-	-	-	PH1	I/O	**X**	X		HS	O3	X	X	**Port H1**		
15	-	-	-	-	PH2	I/O	**X**	X			O1	X	X	**Port H2**		
16	-	-	-	-	PH3	I/O	**X**	X			O1	X	X	**Port H3**		
17	13	-	-	-	PF7/AIN15	I/O	**X**	X			O1	X	X	**Port F7**	Analog input 15	
18	14	-	-	-	PF6/AIN14	I/O	**X**	X			O1	X	X	**Port F6**	Analog input 14	
19	15	-	-	-	PF5/AIN13	I/O	**X**	X			O1	X	X	**Port F5**	Analog input 13	
20	16	-	-	8	PF4/AIN12	I/O	**X**	X			O1	X	X	**Port F4**	Analog input 12	
21	17	-	-	-	PF3/AIN11	I/O	**X**	X			O1	X	X	**Port F3**	Analog input 11	
22	18	-	-	-	V_{REF+}	S								ADC positive reference voltage		
23	19	13	12	9	V_{DDA}	S								Analog power supply		
24	20	14	13	10	V_{SSA}	S								Analog ground		
25	21	-	-	-	V_{REF-}	S								ADC negative reference voltage		
26	22	-	-	-	PF0/AIN10	I/O	**X**	X			O1	X	X	**Port F0**	Analog input 10	
27	23	15	14	-	PB7/AIN7	I/O	**X**	X	X		O1	X	X	**Port B7**	Analog input 7	
28	24	16	15	-	PB6/AIN6	I/O	**X**	X	X		O1	X	X	**Port B6**	Analog input 6	
29	25	17	16	11	PB5/AIN5	I/O	**X**	X	X		O1	X	X	**Port B5**	Analog input 5	I^2C_SDA [AFR6]
30	26	18	17	12	PB4/AIN4	I/O	**X**	X	X		O1	X	X	**Port B4**	Analog input 4	I^2C_SCL [AFR6]

Table 6. Pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	LQFP44	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
46	37	29	-	21	PC4/TIM1_CH4	I/O	**X**	X	X	HS	O3	X	X	**Port C4**	Timer 1 - channel 4	
47	38	30	27	22	PC5/SPI_SCK	I/O	**X**	X	X	HS	O3	X	X	**Port C5**	SPI clock	
48	39	31	28	-	V_{SSIO_2}	S								I/O ground		
49	40	32	29	-	V_{DDIO_2}	S								I/O power supply		
50	41	33	30	23	PC6/SPI_MOSI	I/O	**X**	X	X	HS	O3	X	X	**Port C6**	SPI master out/ slave in	
51	42	34	31	24	PC7/SPI_MISO	I/O	**X**	X	X	HS	O3	X	X	**Port C7**	SPI master in/ slave out	
52	43	35	32	-	PG0/CAN_TX(2)	I/O	**X**	X			O1	X	X	**Port G0**	beCAN transmit	
53	44	36	33	-	PG1/CAN_RX(2)	I/O	**X**	X			O1	X	X	**Port G1**	beCAN receive	
54	45	-	-	-	PG2	I/O	**X**	X			O1	X	X	**Port G2**		
55	46	-	-	-	PG3	I/O	**X**	X			O1	X	X	**Port G3**		
56	47	-	-	-	PG4	I/O	**X**	X			O1	X	X	**Port G4**		
57	48	-	-	-	PI0	I/O	**X**	X			O1	X	X	**Port I0**		
58	-	-	-	-	PI1	I/O	**X**	X			O1	X	X	**Port I1**		
59	-	-	-	-	PI2	I/O	**X**	X			O1	X	X	**Port I2**		
60	-	-	-	-	PI3	I/O	**X**	X			O1	X	X	**Port I3**		
61	-	-	-	-	PI4	I/O	**X**	X			O1	X	X	**Port I4**		
62	-	-	-	-	PI5	I/O	**X**	X			O1	X	X	**Port I5**		
63	49	-	-	-	PG5	I/O	**X**	X			O1	X	X	**Port G5**		
64	50	-	-	-	PG6	I/O	**X**	X			O1	X	X	**Port G6**		
65	51	-	-	-	PG7	I/O	**X**	X			O1	X	X	**Port G7**		
66	52	-	-	-	PE4	I/O	**X**	X	X		O1	X	X	**Port E4**		
67	53	37	-	-	PE3/TIM1_BKIN	I/O	**X**	X	X		O1	X	X	**Port E3**	Timer 1 - break input	
68	54	38	34	-	PE2/I^2C_SDA	I/O	**X**		X		O1	T(3)		**Port E2**	I^2C data	

remap) option bits. Refer to *Section 8: Option bytes on page 47*. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of the family reference manual, RM0016).

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5216	I²C	I2C_DR	I²C data register	0x00
0x00 5217		I2C_SR1	I²C status register 1	0x00
0x00 5218		I2C_SR2	I²C status register 2	0x00
0x00 5219		I2C_SR3	I²C status register 3	0x00
0x00 521A		I2C_ITR	I²C interrupt control register	0x00
0x00 521B		I2C_CCRL	I²C clock control register low	0x00
0x00 521C		I2C_CCRH	I²C clock control register high	0x00
0x00 521D		I2C_TRISER	I²C TRISE register	0x02
0x00 521E to 0x00 522F	Reserved area (18 bytes)			
0x00 5230	UART1	UART1_SR	UART1 status register	0xC0
0x00 5231		UART1_DR	UART1 data register	0xXX
0x00 5232		UART1_BRR1	UART1 baud rate register 1	0x00
0x00 5233		UART1_BRR2	UART1 baud rate register 2	0x00
0x00 5234		UART1_CR1	UART1 control register 1	0x00
0x00 5235		UART1_CR2	UART1 control register 2	0x00
0x00 5236		UART1_CR3	UART1 control register 3	0x00
0x00 5237		UART1_CR4	UART1 control register 4	0x00
0x00 5238		UART1_CR5	UART1 control register 5	0x00
0x00 5239		UART1_GTR	UART1 guard time register	0x00
0x00 523A		UART1_PSCR	UART1 prescaler register	0x00
0x00 523B to 0x00 523F	Reserved area (5 bytes)			
0x00 5240	UART3	UART3_SR	UART3 status register	C0h
0x00 5241		UART3_DR	UART3 data register	0xXX
0x00 5242		UART3_BRR1	UART3 baud rate register 1	0x00
0x00 5243		UART3_BRR2	UART3 baud rate register 2	0x00
0x00 5244		UART3_CR1	UART3 control register 1	0x00
0x00 5245		UART3_CR2	UART3 control register 2	0x00
0x00 5246		UART3_CR3	UART3 control register 3	0x00
0x00 5247		UART3_CR4	UART3 control register 4	0x00
0x00 5248		Reserved		
0x00 5249		UART3_CR6	UART3 control register 6	0x00
0x00 524A to 0x00 524F	Reserved area (6 bytes)			

9 Unique ID

The devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single bytes and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

Table 14. Unique ID registers (96 bits)

Address	Content description	Unique ID bits							
		7	6	5	4	3	2	1	0
0x48CD	X co-ordinate on the wafer	U_ID[7:0]							
0x48CE		U_ID[15:8]							
0x48CF	Y co-ordinate on the wafer	U_ID[23:16]							
0x48D0		U_ID[31:24]							
0x48D1	Wafer number	U_ID[39:32]							
0x48D2	Lot number	U_ID[47:40]							
0x48D3		U_ID[55:48]							
0x48D4		U_ID[63:56]							
0x48D5		U_ID[71:64]							
0x48D6		U_ID[79:72]							
0x48D7		U_ID[87:80]							
0x48D8		U_ID[95:88]							

Total current consumption in wait mode

Table 22. Total current consumption in wait mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 24 MHz, $T_A \leq$ 105 °C	HSE crystal osc. (24 MHz)	2.4		mA
			HSE user ext. clock (24 MHz)	1.8	4.7	
		$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	2.0		
			HSE user ext. clock (16 MHz)	1.4	4.4	
			HSI RC osc. (16 MHz)	1.2	1.6	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	1.0		
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.55		
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.5		

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Table 23. Total current consumption in wait mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 24 MHz, $T_A \leq$ 105 °C	HSE crystal osc. (24 MHz)	2.0		mA
			HSE user ext. clock (24 MHz)	1.8	4.7	
		$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.6		
			HSE user ext. clock (16 MHz)	1.4	4.4	
			HSI RC osc. (16 MHz)	1.2	1.6	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	1.0		
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.55		
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	LSI RC osc. (128 kHz)	0.5		

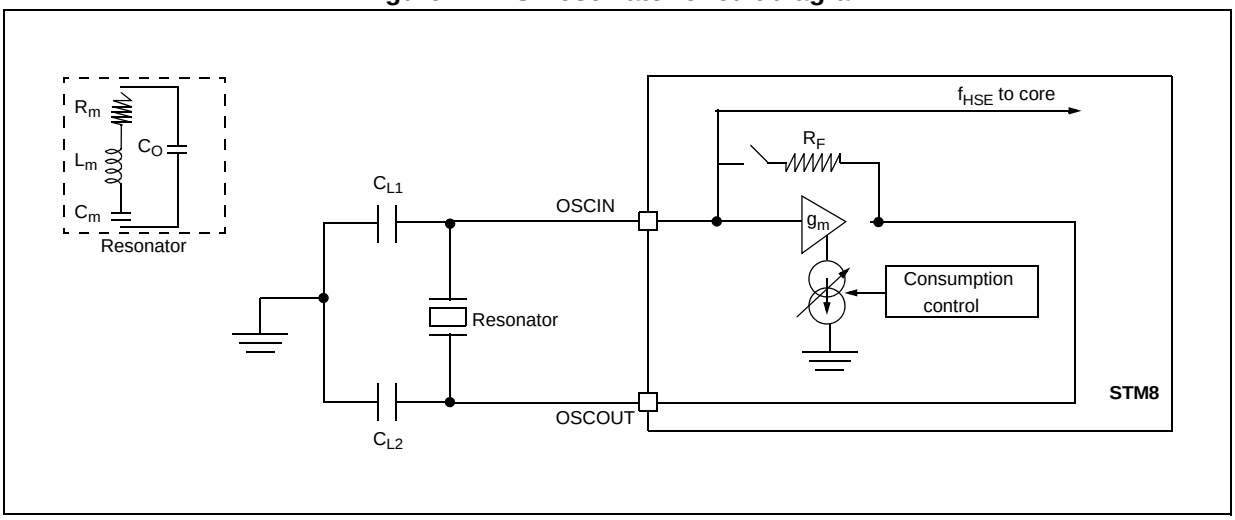
1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Table 32. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	External high speed oscillator frequency		1		24	MHz
R_F	Feedback resistor			220		kΩ
$C^{(1)}$	Recommended load capacitance (2)				20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 24 MHz			6 (startup) 2 (stabilized)(3)	mA
		C = 10 pF, f_{OSC} = 24 MHz			6 (startup) 1.5 (stabilized)(3)	
g_m	Oscillator transconductance		5			mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized		1		ms

1. C is approximately equivalent to 2 x crystal Cload.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Data based on characterization results, not tested in production.
4. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 24 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 17. HSE oscillator circuit diagram

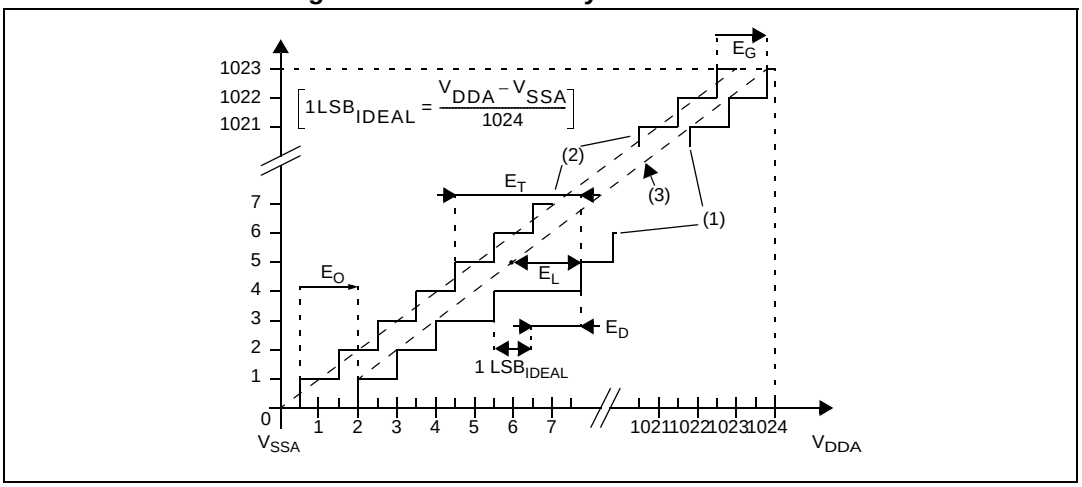


HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

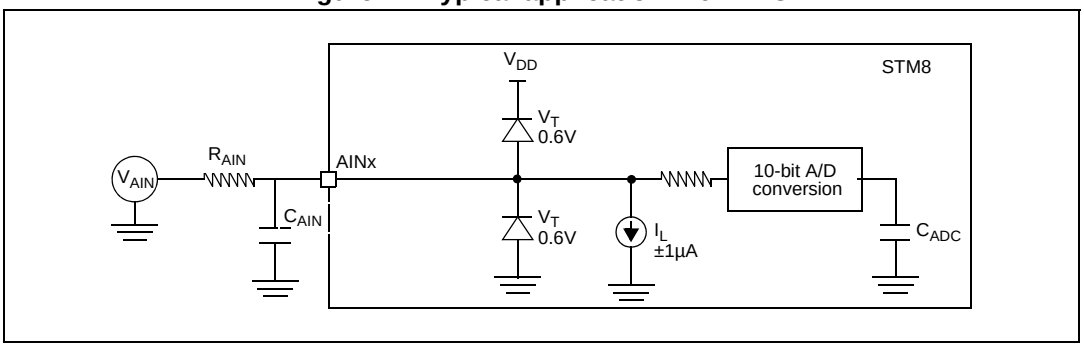
R_m: Notional resistance (see crystal specification)
L_m: Notional inductance (see crystal specification)
C_m: Notional capacitance (see crystal specification)
Co: Shunt capacitance (see crystal specification)
C_{L1}=C_{L2}=C: Grounded external capacitance
$g_m >> g_{mcrit}$

Figure 41. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. The ideal transfer curve
3. End point correlation line
   E_T = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset error: deviation between the first actual transition and the first ideal one.
   E_G = Gain error: deviation between the last ideal transition and the last actual one.
   E_D = Differential linearity error: maximum deviation between actual steps and the ideal one.
   E_L = Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

Figure 42. Typical application with ADC



Electromagnetic interference (EMI)

Emission tests conform to the SAE IEC 61967-2 standard for test software, board layout and pin loading.

Table 48. EMI data

Symbol	Parameter	Conditions					Unit
		General conditions	Monitored frequency band	Max f_{HSE}/f_{CPU} (1)			
				8 MHz/ 8 MHz	8 MHz/ 16 MHz	8 MHz/ 24 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V T_A = 25 °C LQFP80 package conforming to SAE IEC 61967-2	0.1MHz to 30 MHz	15	20	24	dBµV
			30 MHz to 130 MHz	18	21	16	
			130 MHz to 1 GHz	-1	1	4	
	SAE EMI level		SAE EMI level	2	2.5	2.5	

1. Data based on characterization results, not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 49. ESD absolute maximum ratings

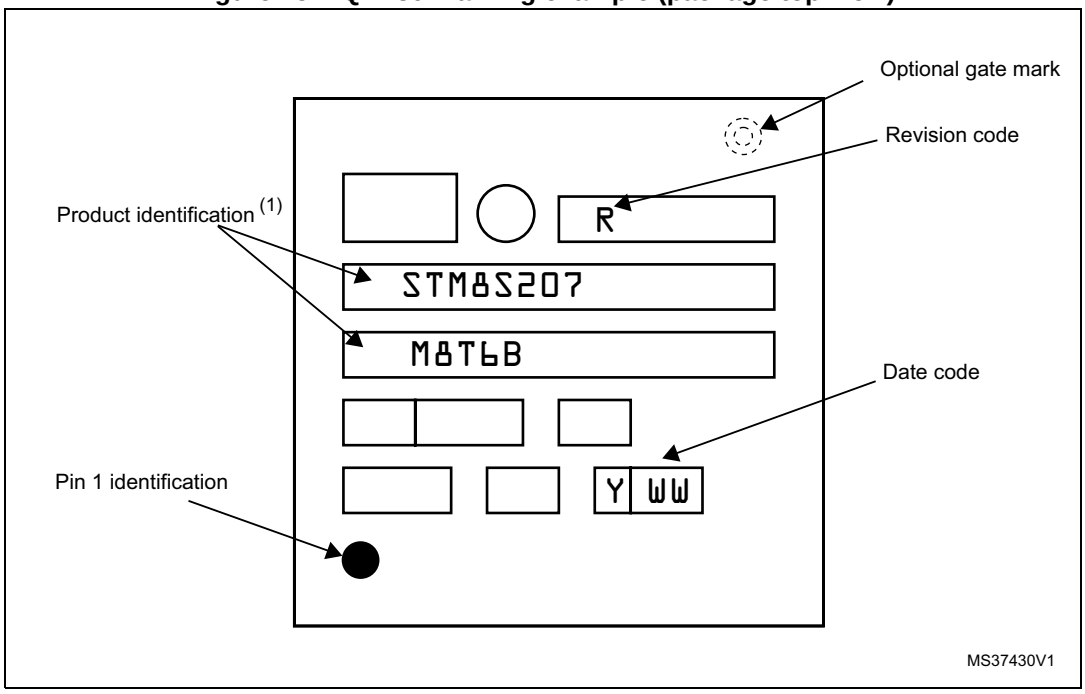
Symbol	Ratings	Conditions	Class	Maximum value (1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to JESD22-A114	A	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	T_A= 25°C, conforming to JESD22-C101	IV	1000	V

1. Data based on characterization results, not tested in production.

Device marking

The following figure shows the marking for the LQFP80 package.

Figure 45. LQFP80 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

11.1.2 LQFP64 package information

Figure 46. LQFP64 - 64-pin 14 mm x 14 mm low-profile quad flat package outline

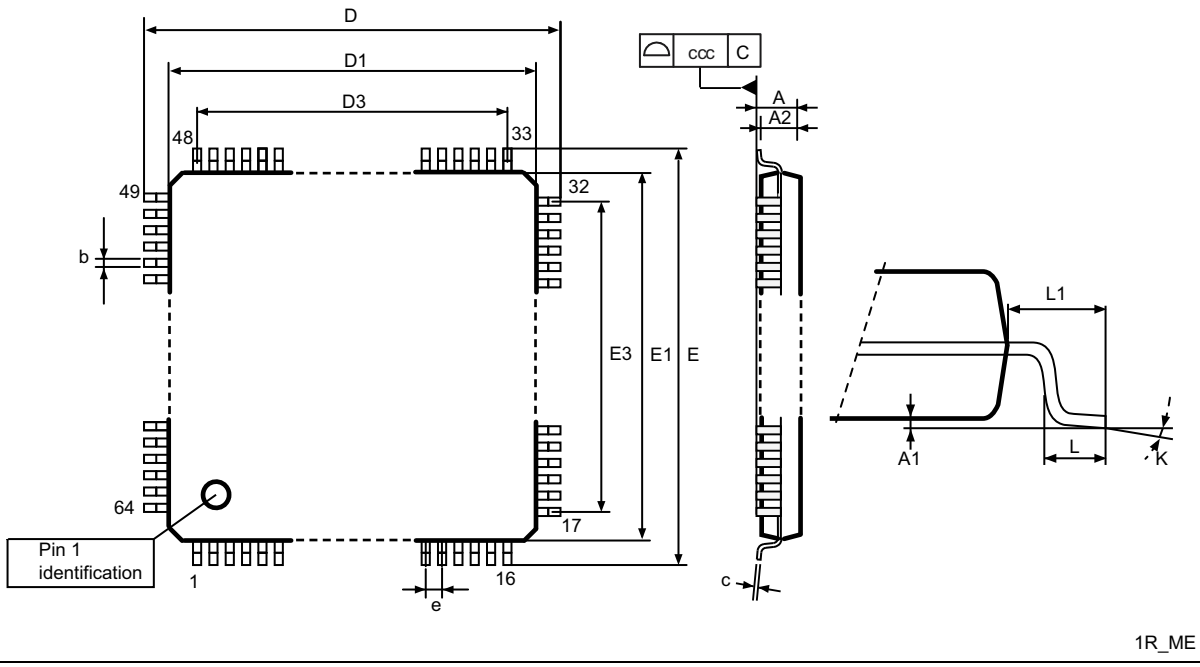


Table 52. LQFP64 - 64-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
C	0.090		0.200	0.0035		0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3		12.000			0.4724	
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3		12.000			0.4724	
e		0.800			0.0315	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	

11.1.3 LQFP48 package information

Figure 50. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline

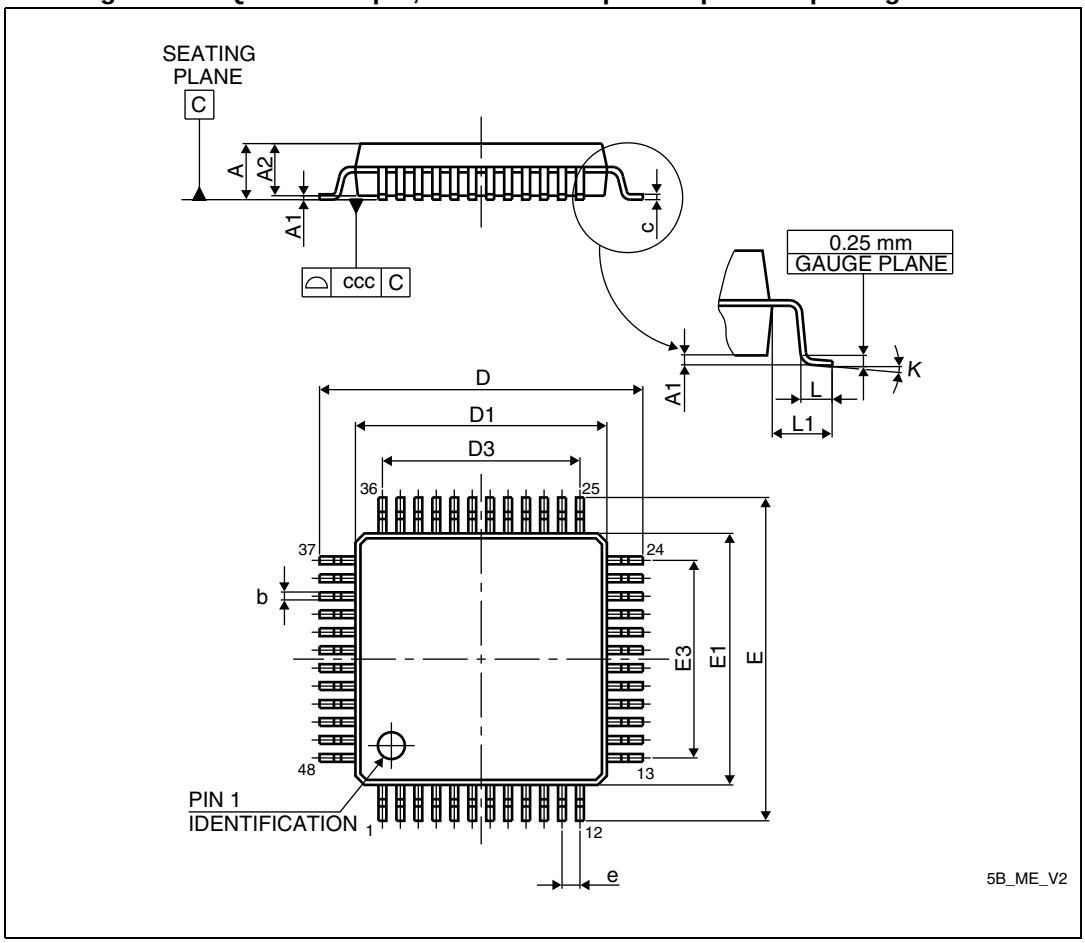


Table 54. LQFP48 - 48-pin, 7x 7 mm low-profile quad flat package mechanical

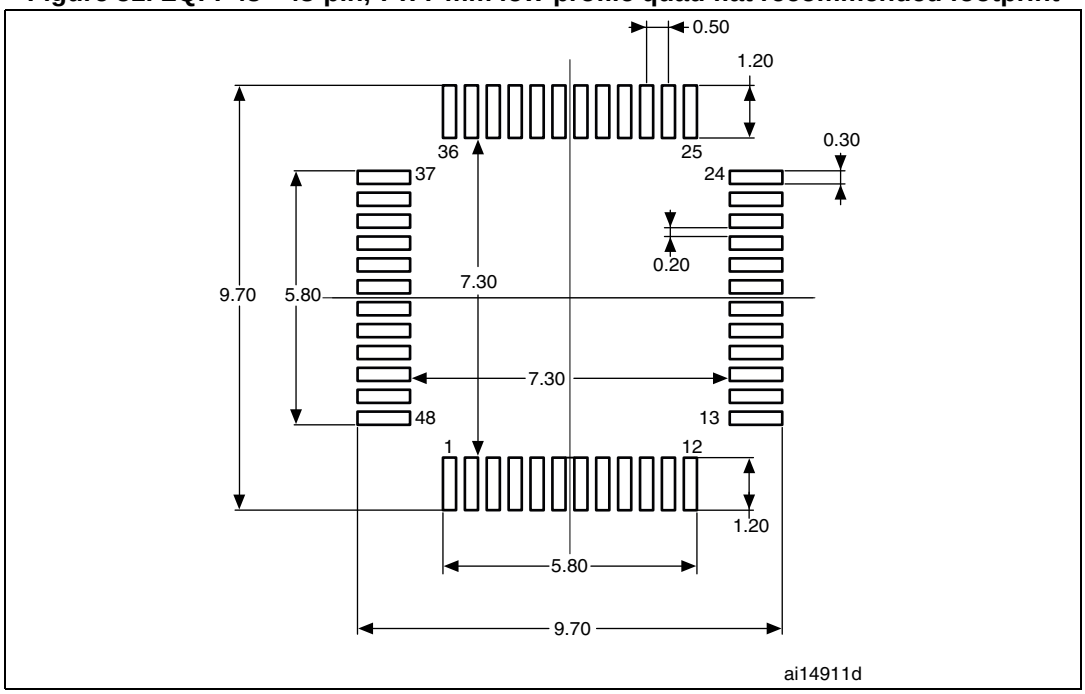
Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622

Table 54. LQFP48 - 48-pin, 7x 7 mm low-profile quad flat package mechanical (continued)

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal places.

Figure 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint



1. Dimensions are expressed in millimeters.

Table 55. LQFP44 - 44-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035		0.0079
D	11.800	12.000	12.200	0.4646	0.4724	0.4803
D1	9.800	10.000	10.200	0.3858	0.3937	0.4016
D3	-	8.000	-	-	0.3150	-
E	11.800	12.000	12.200	0.4646	0.4724	0.4803
E1	9.800	10.000	10.200	0.3858	0.3937	0.4016
E3	-	8.000	-	-	0.3150	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal places.

Table 58. Document revision history (continued)

Date	Revision	Changes
18-Feb-2015	13	Updated: – *Figure 43: LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package outline* – *Table 51: LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package mechanical data* – *Figure 51: LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package mechanical data* – *Figure 47: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline* – *Table 53: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data* – *Figure 50: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline* – *Table 54: LQFP48 - 48-pin, 7x 7 mm low-profile quad flat package mechanical* – *Figure 56: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline* – *Table 56: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data* Added: – *Figure 44: LQFP80 recommended footprint* – *Figure 45: LQFP80 marking example (package top view)* – *Figure 48: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint* – *Figure 49: LQFP64 marking example (package top view)* – *Figure 51: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint* – *Figure 52: LQFP48 marking example (package top view)* – *Figure 54: LQFP44 - 44-pin, 10 x 10 mm low-profile quad flat recommended footprint* – *Figure 55: LQFP44 marking example (package top view)* – *Figure 57: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat recommended footprint* – *Figure 58: LQFP32 marking example (package top view)*